IC Design

Homework # 3

(Due on 2020/12/18, 13:20. Verilog code and Report upload to CEIBA)

- ✧ Plagiarism is not allowed. 10% penalty for each day of delay.
- ✧ Any further questions, you can send e-mail to the TA (李嘉恆)or leave messages on the board of the class website.
- ✧ TA email: r08943006@ntu.edu.tw , EE2-329

Specifications

In this homework, you are asked to design a **gate-level combinational circuit** that sorts five given numbers. The inputs of this circuit are **five 6-bit unsigned** digital values, denoted as *i0, i1, i2, i3, i4*. The outputs of the circuit, denoted as *rank0(biggest), rank1, rank2, rank3, rank4(smallest),* are all **6-bit unsigned numbers**.

Below are some examples of the I/O:

Input					Output				
i0	*i1*	*i2*	*i3*	*i4*	Rank0	Rank1	Rank2	Rank3	Rank4
0x09	0x1c	0x1d	0x26	0x2f	0x2f	0x26	0x1d	0x1c	0x09
0x07	0x0a	0x35	0x2c	0x37	0x37	0x35	0x2c	0x0a	0x07
0x1d	0x24	0x3a	0x36	0x26	0x3a	0x36	0x26	0x24	0x1d

[**HINT**] Bubble sort may not be fast enough, so try to use other sorting methods that are more hardware friendly.

There are some important things that you should notice:

- ➢ Your design should base on the **standard cells in the lib.v**. All logic operations in your design **MUST consist of the standard cells** instead of using the operands such as “+”, ”-”, “&”, “|”, “>”, and “<”. **Note that the score of HW3 will be 0 if you use any of them.**
- ➢ Design your homework in the given “sorting.v” file. **You are NOT ALLOWED to change the filename and the header of the top module (i.e. the module name and the I/O ports)**.
- ➢ If your design contains more than one module, don’t create new file for them, just put those modules in “sorting.v.”
- ➢ The output waveform will be dumped to file “**sorting.fsdb.”** You can use nWave to examine it.
- ➢ **For each set of input data, the test bench will allow your circuit to calculate the sorter outputs within 20ns.** Once exceeding 20ns or detecting the correct

answer from your circuit, the test bench will soon provide the new data set to your design until all 10000 data sets have been simulated.

Grading

1. Gate-level design using Verilog (80%)

Your score will depend on both the correctness and performance of your design. We provide a "public" test bench with 10000 datasets. What follows is the grading policy:

Correctness & Performance	Score
Fail to pass the test bench.	40 * (1-err #/10000)
Functionally correct	40
Critical Path < 8ns	45
Critical Path < 7ns	50
Critical Path < 6ns	55
Critical Path < 5ns	60
Critical Path < 4ns	70
Critical Path < 3ns	80
Using operands, not standard cell logic	0
Plagiarism	0

Testbench will provide related information for grading:

```
Congratulations! Your critical path is below 5!

Simulation complete via $finish(1) at time 210 US + 0
./tb_sorting_v2.v:137                   $finish;
ncsim> exit
```

2. Report (20%)

You should also describe and discuss your design. Below are required items in your report.

- Circuit diagram (10%)

  Plot the circuit diagram of your design. You are encouraged to plot it hierarchically so that the reader can understand your design easily.

- Discussion (10%)

  Discuss about your design. For example, how do you sort these numbers, how do you improve your critical path.

Notification

- Following are the files you will need (available on the class website)
  HW3.zip includes
  - **HW3_2020.pdf** : this document.
  - **HW3_tutorial** Verilog introduction
  - **sorting.v**:
    Dummy design file. Program the design in this file.
    The header of the top module and the declaration of the I/O ports are predefined in this file and you cannot change them.
  - **lib.v**: standard cells.
  - **tb_ sorting.v**:
    Testbench for your design.
  - **tb_ sorting_pattern.v**:
    Testbench for debugging.
  - **i0.dat, i1.dat, i2.dat, i3.dat, i4.dat:**
    Input patterns for test bench. Put these files in the folder that contains **tb_ sorting.v** when doing simulation.
  - **golden0.dat, golden1.dat, golden2.dat, golden3.dat, golden4.dat:**
    Output patterns of correct answers for test bench. Put these files in the folder that contains **tb_ sorting.v** when doing simulation.

- The following files should be compressed and uploaded to CEIBA by due time.
  - Report (PDF format)
  - sorting.v
- File name rule : *HW3_(student id)_v#*
  Ex. HW3_b03901301_v1.zip
  Ex. HW3_b03901311_v2.zip

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HW3 Office hours: 12/14 19:00-21:00 @ 博理 213
12/17 12:00-14:00 @ 博理 215
If you have no time at office hours, you can email TA to discuss another time for appointment.