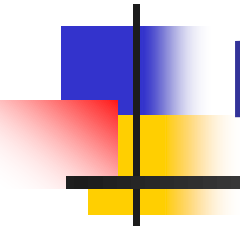
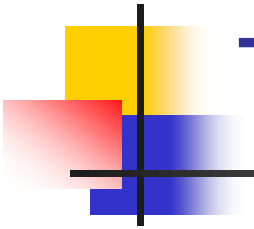


# Digital System Design

Instructor: Pei-Yun Tsai

Email: pytsai@ee.ncu.edu.tw

Spring 2022



# Target of the Course

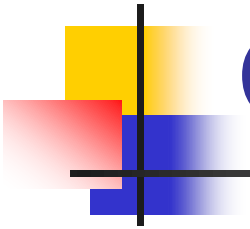
- Supplements to basic digital design course
- Study the Hardware Description Language (HDL) – Verilog/System Verilog
- Familiar with modeling digital designs by HDL
  - Case studies
  - Homework/Lab
- Familiar with hardware implementation on FPGA boards.

# Course (1/2)

- Credit: 3
- Office Hour:
  - Monday, 3:00PM-5:00PM
- eeClass system
  - Download lecture notes
  - Upload your codes
- Reference Book
  - Josoph Cavanagh, “Verilog HDL – Digital Design and Modeling,” CRC Press.
  - Samir Palnitkar, “Verilog HDL – A Guide to Digital Design and Synthesis,” Sunsoft Press.

# Course (2/2)

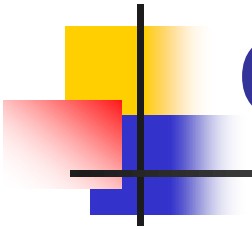
- Course Time (Location: E1-124)
  - Tuesday 13:00~14:50 (E1-124)
  - Thursday 11:00~11:50 (E1-124)
- Lab Time (Location: E1-223)
  - Thursday 10:00~11:50
  - Friday 13:00~14:50 (二者擇一)
- Prerequisites
  - Introduction to digital systems



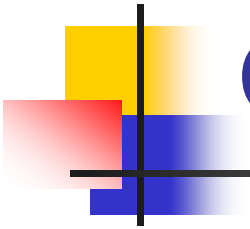
# Overview

- Introduction
- Language fundamentals -- Verilog HDL
- Modeling sequential elements
- Modeling combinational circuits
- Review of Synchronous sequential logic
- Modeling finite state machines
- Modeling digital systems
- Introduction to HDL synthesis
- Introduction to System Verilog

# Grading (1/2)

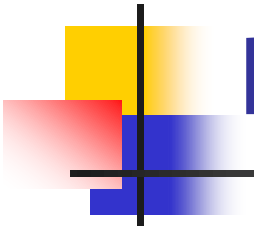


- Several labs … ☹
  - Presentation and demonstration are necessary
  - Possible topics: (subject to change)
    - Verilog simulation & implementation
    - Design combinational circuits
    - Design sequential circuits
    - Design finite state machine
    - Project status checking
- Homework/Lab
  - Basically assigned per week/every two weeks
  - May require a lot of time
- Total …. 45%



# Grading (2/2)

- One final project --- 20%
  - Design a “large” digital system with Verilog
  - Required to work on FPGA
  - Details will be announced after midterm
- One final exam--- 35%
  - A simple writing test of Verilog
  - Maybe on-line testing



# Rule

- “Cheating“ is very uncivilized behavior and is to be avoided at all cost
- Oral discussion is not considered as cheating
- Copying someone else’s work or part of a work is cheating
- If cheating is discovered
  - All students involved will receive no credit for the homework / project
  - They will possibly get an F grade for the course

# Syllabus

| Date | Contents | Date | 1ontents |
|---|---|---|---|
| 2/15, 2/17 | Introduction to Verilog | 4/19, 4/21 | Keyboard and Debounce (Homework 3) |
| 2/22, 2/24 | Introduction to Verilog | 4/26, 4/28 | Keyboard and Debounce (Lab 3) |
| 3/01, 3/03 | Introduction to Verilog (Homework 1) | 5/03, 5/05 | VGA Display Module (Lab 3) |
| 3/08, 3/10 | Modeling Sequential Circuits (Homework 2) | 5/10, 5/12 | VGA Display Module (Lab 4) |
| 3/15, 3/17 | Seven-Segment & LED Display (Lab 1) | 5/17, 5/19 | Modeling Digital System (Lab 5) |
| 3/22, 3/24 | Synthesis (Lab 1) | 5/24, 5/26 | Modeling Digital System (Lab 5) |
| 3/29, 3/31 | Modeling Combination Circuits (Lab 2) | 5/31, 6/02 | Final Exam/Final Project |
| 4/05, 4/07 | Modeling Finite State Machine (Lab 2) | 6/07, 6/09 | Final Project |
| 4/12, 4/14 | Modeling Finite State Machine (Homework 3) | 6/14, 6/16 | Final Project |

# Teaching Assistant

- At Room 232
  - 柯翔展 asd55288@gmail.com
  - 吳禹辰 chen19990410@gmail.com
  - 陳柏達 s1060632@mail.yzu.edu.tw
  - 何芝儀 lspss097273@gmail.com
  - 賴品叡 ray795461@gmail.com