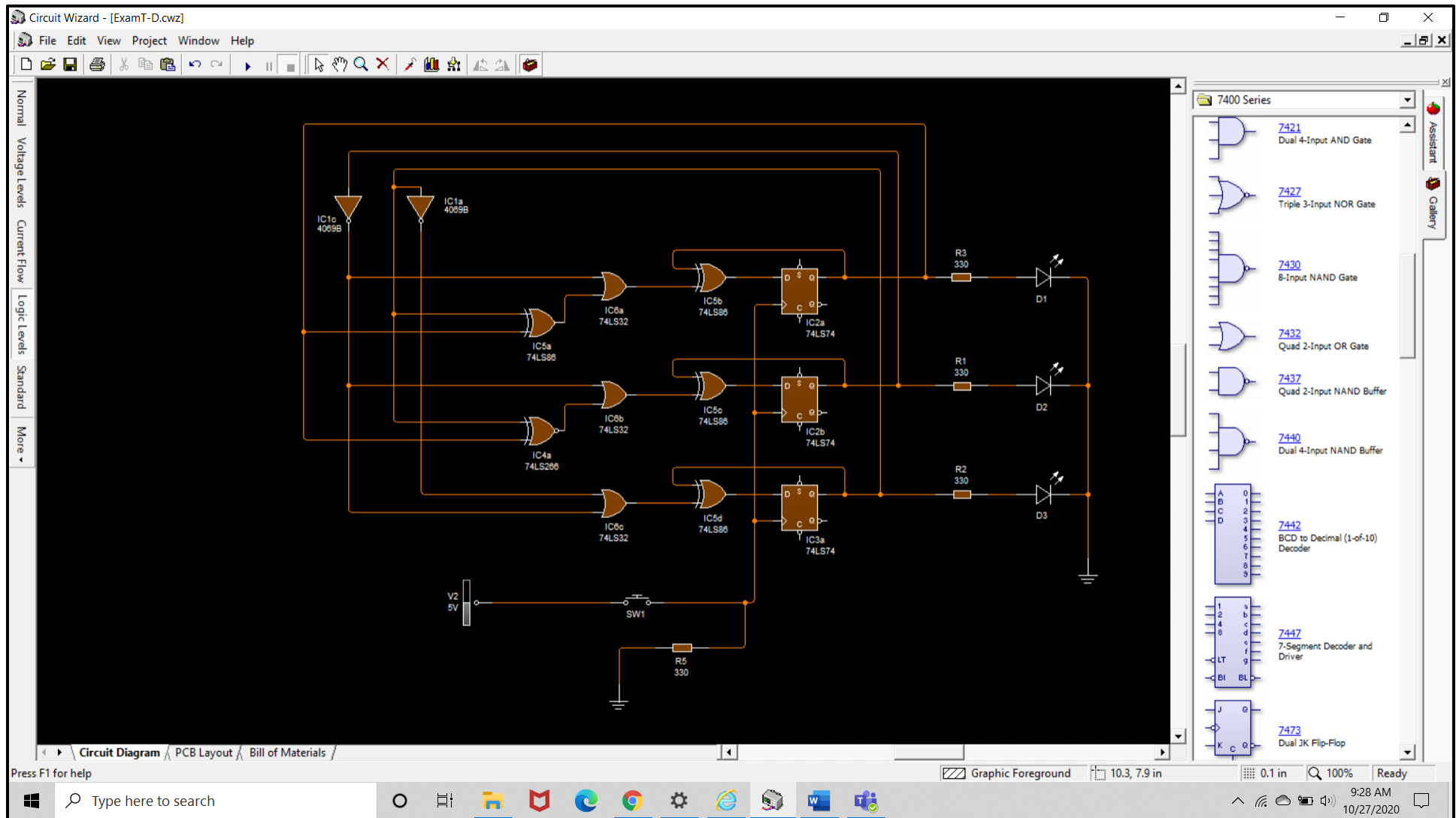
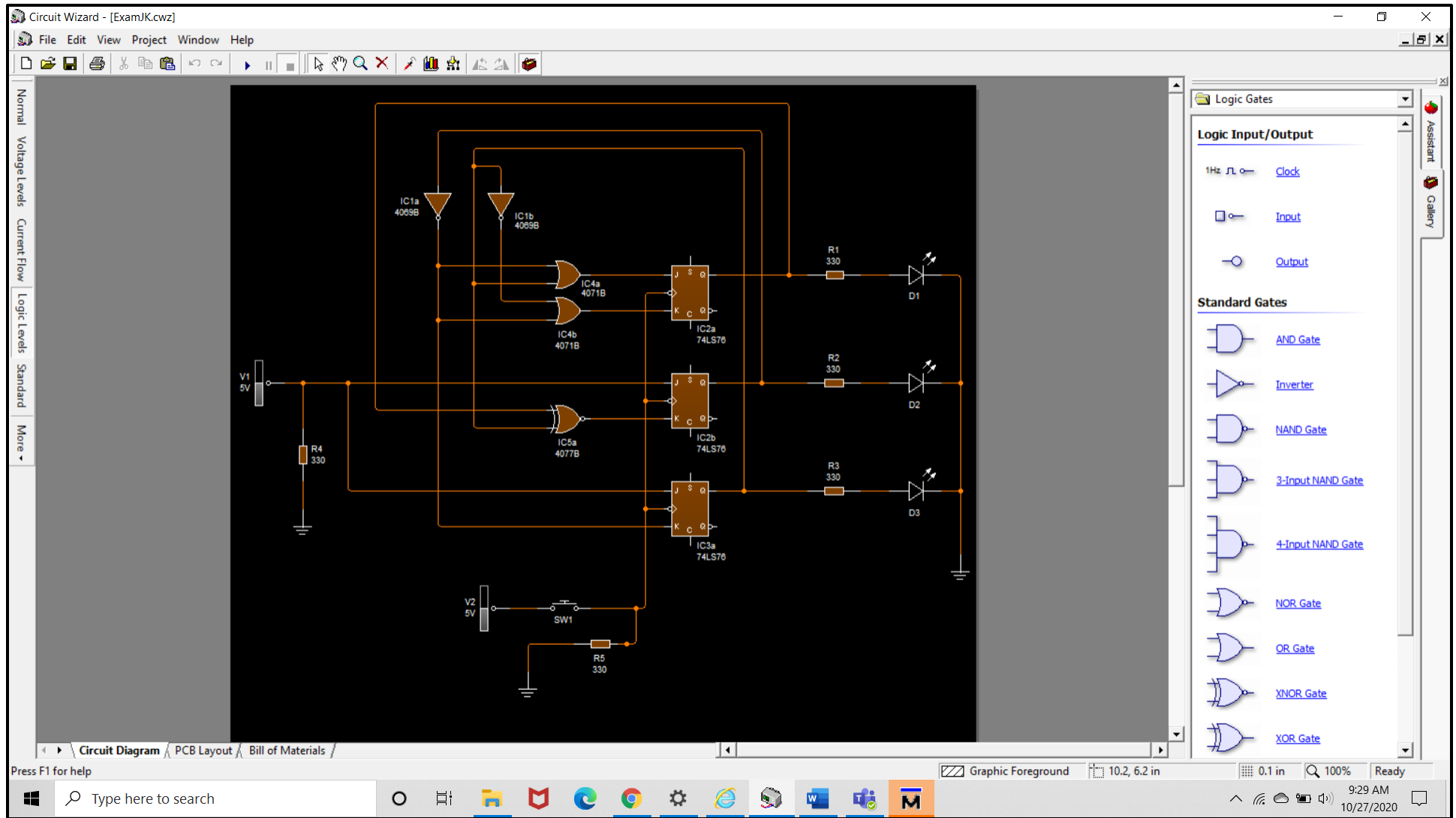


CIRCUIT DIAGRAM (Number 1)

A. T Flip-Flop



B. JK Flip Flop



Number 2

A. HALF SUBTRACTOR

1) System Module Code

The screenshot displays the ModelSim PE Student Edition 10.4a interface. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Source, Tools, Layout, Bookmarks, Window, and Help. The toolbar contains various icons for file operations, simulation, and layout. The main workspace is divided into three panes:

- Project Pane:** Shows the project structure for "C:/Modeltech_pe_edu_10.4a/examples/Half Subtractor". It lists two files: "half_subtractor.v" and "tb_half_sub.v", both with a status of "Verilog" and a "Modified" timestamp of "10/27/2020 09:39:29 am".
- Code Editor:** Displays the Verilog code for the "half_subtractor.v" module. The code is as follows:

```
1 module half_subtractor (X, Y, Difference, Borrow);  
2   input X, Y;  
3   output Difference, Borrow;  
4   wire wire1;  
5  
6   not Inv1 (wire1, X);  
7   xor G1 (Difference, X, Y);  
8   and G2 (Borrow, wire1, Y);  
9  
10  endmodule  
11
```
- Transcript Pane:** Shows the compilation results:

```
# Reading C:/Modeltech_pe_edu_10.4a/tcl/vsim/pref.tcl  
project open (C:/Modeltech_pe_edu_10.4a/examples/Half Subtractor)  
# Loading project Half Subtractor  
# Compile of half_subtractor.v was successful.  
# Compile of tb_half_sub.v was successful.  
# 2 compiles, 0 failed with no errors.  
ModelSim>
```

The bottom status bar indicates the current position in the code (Ln: 1 Col: 0), the project name (Project: Half Subtractor), and the design status (<No Design Loaded>).

2) Testbench Code

The screenshot displays the ModelSim PE Student Edition 10.4a interface. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Source, Tools, Layout, Bookmarks, Window, and Help. The toolbar contains various icons for file operations, simulation, and layout. The main workspace is divided into three panes:

- Project Explorer:** Shows the project structure for "C:/Modeltech_pe_edu_10.4a/examples/Half Subtractor". It lists two files: `half_subtractor.v` and `tb_half_sub.v`, both in Verilog format, with their respective modification dates.
- Code Editor:** Displays the testbench code for `tb_half_sub.v`. The code is as follows:

```
1 module tb_half_subtractor;
2   reg A, B;
3   wire Z0, Z1;
4   half_subtractor tbl (A, B, Z0, Z1);
5   initial
6   begin
7     A=1'b0; B=1'b0;
8     $display ("Simulating output for Half Subtractor");
9     $monitor ($time, " A=%b B=%b", A,B,Z0,Z1);
10    #1 A=1'b0 ; B=1'b1 ;
11    #1 A=1'b1 ; B=1'b1 ;
12    #2 $finish;
13  end
14 endmodule
15
```
- Transcript:** Shows the simulation log, indicating that the project was opened, loaded, and compiled successfully without errors.

```
# Reading C:/Modeltech_pe_edu_10.4a/tcl/vsim/pref.tcl
project open {C:/Modeltech_pe_edu_10.4a/examples/Half Subtractor}
# Loading project Half Subtractor
# Compile of half_subtractor.v was successful.
# Compile of tb_half_sub.v was successful.
# 2 compiles, 0 failed with no errors.

ModelSim>
```

The bottom status bar shows the current line and column (Ln: 1 Col: 0), the project name (Project: Half Subtractor), and the design context (<No Design Loaded>).

3) Timing Diagram

ModelSim PE Student Edition 10.4a

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

ColumnLayout Default

Search:

sim - Default

Instance	Design unit	Design unit type	Top Category
tb_half_su...	tb_half_su...	Module	DU Instance
tb1	half_subtra...	Module	DU Instance
#INITI...	tb_half_su...	Process	-
#vsim_cap...	Capacity	Statistics	

Objects

Name	Value	Kind	Now
A	1'h1	Regi...	Internal
B	1'h1	Regi...	Internal
Z0	1'h0	Net	Internal
Z1	1'h0	Net	Internal

Wave - Default

Name	Value
/tb_half_subtractor/A	1'h1
/tb_half_subtractor/B	1'h1
/tb_half_subtractor/Z0	1'h0
/tb_half_subtractor/Z1	1'h0

Now 4 ns
Cursor 1 0 ns

0 ns 2 ns 4 ns 6 ns 8 ns

Library Project sim

Transcript

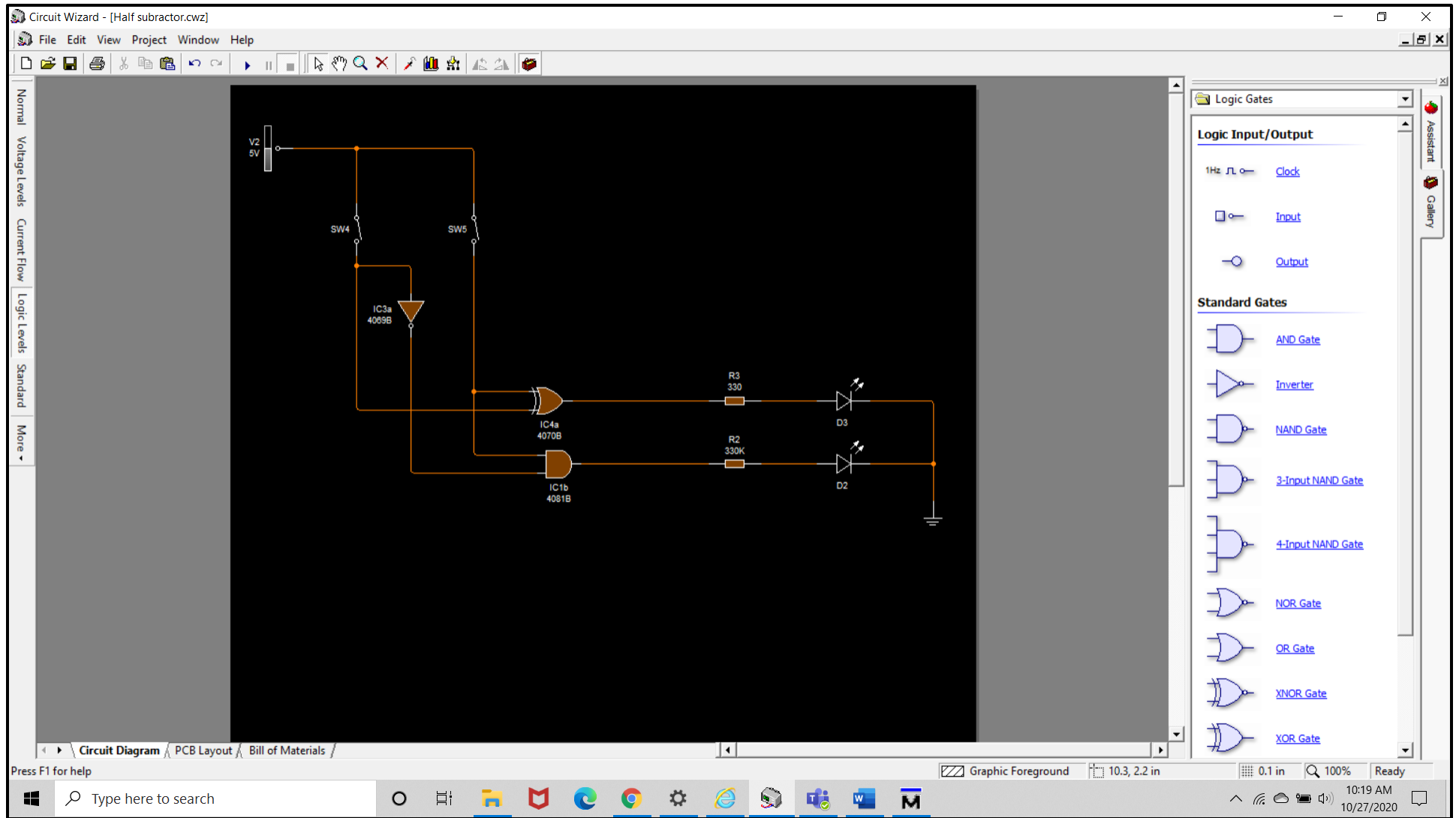
```
add wave -position end sim:/tb_half_subtractor/Z1
VSIM 7> run
# Simulating output for Half Subtractor
# 0 A=0 B=000
# 1 A=0 B=111
# 2 A=1 B=100
# ** Note: $finish : C:/Modeltech_pe_edu_10.4a/examples/tb_half_sub.v(12)
# Time: 4 ns Iteration: 0 Instance: /tb_half_subtractor
# 1
# Break in Module tb_half_subtractor at C:/Modeltech_pe_edu_10.4a/examples/tb_half_sub.v line 12
VSIM 8>
```

0 ns to 8 ns Project: Half Subtractor Now: 4 ns Delta: 0 sim:/tb_half_subtractor/#INITIAL#5

Type here to search

9:44 AM 10/27/2020

4) Circuit Diagram



FULL ADDER

1) System Module Code

The screenshot displays the ModelSim PE Student Edition 10.4a interface. The main window shows the Verilog code for a Full Adder module. The code is as follows:

```
1 module full_adder (A, B, C_in, Sum, C_out);
2   input A, B, C_in;
3   output Sum, C_out;
4   wire wire1, wire2, wire3;
5
6   xor G1 (wire1, A, B);
7   xor G2 (Sum, wire1, C_in);
8   and G3 (wire2, C_in, wire1);
9   and G4 (wire3, A, B);
10  or G5 (C_out, wire2, wire3);
11
12 endmodule
13
```

The left pane shows the project structure with files `full_adder.v` and `tb_full_adder.v`. The bottom pane shows the transcript of the compilation process:

```
# Reading C:/Modeltech_pe_edu_10.4a/tcl/vsim/pref.tcl
project open {C:/Modeltech_pe_edu_10.4a/examples/Full Adder}
# Loading project Full Adder
# Compile of full_adder.v was successful.
# Compile of tb_full_adder.v was successful.
# 2 compiles, 0 failed with no errors.

ModelSim>
```

The status bar at the bottom indicates the project is "Full Adder" and the design is not loaded. The Windows taskbar is visible at the bottom of the screen.

2) Testbench Code

The screenshot displays the ModelSim PE Student Edition 10.4a interface. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Source, Tools, Layout, Bookmarks, Window, and Help. The toolbar contains various icons for file operations, simulation, and layout. The main workspace is divided into three panes:

- Project Explorer:** Shows the project structure for "C:/Modeltech_pe_edu_10.4a/examples/Full Adder". It lists two files: "full_adder.v" and "tb_full_adder.v", both with a status of "Verilog" and a modified date of "10/26/2020 0".
- Code Editor:** Displays the testbench code for "tb_full_adder.v". The code is as follows:

```
1 module tb_full_adder;
2   reg A, B, C;
3   wire Z0, Z1;
4   full_adder tbf1 (A, B, C, Z0, Z1);
5   initial
6   begin
7     A=1'b0 ; B=1'b0 ; C=1'b0;
8     $display ("Simulating output for Full Adder");
9     $monitor ($time,,, " A=%b B=%b C=%b", A, B, C, Z0, Z1);
10    #2 A=1'b0 ; B=1'b0 ; C=1'b1;
11    #1 A=1'b0 ; B=1'b1 ; C=1'b0;
12    #1 A=1'b1 ; B=1'b1 ; C=1'b1;
13    #1 A=1'b1 ; B=1'b1 ; C=1'b0;
14    #1 A=1'b1 ; B=1'b0 ; C=1'b0;
15    #1 A=1'b1 ; B=1'b1 ; C=1'b1;
16    #2 $finish;
17  end
18 endmodule
```
- Transcript:** Shows the simulation log, indicating that the project was opened, the files were loaded, and the compilation was successful. It also shows the ModelSim prompt.

The bottom status bar indicates the current line and column (Ln: 1 Col: 0), the project name (Project : Full Adder), and the design context (<No Design Loaded>).

3) Timing Diagram

ModelSim PE Student Edition 10.4a

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

ColumnLayout AllColumns

Search:

sim - Default

Instance	Design unit	Design unit type	Top Category
tb_full_ad...	tb_full_adder	Module	DU Instance
tb1	full_adder	Module	DU Instance
#INITI...	tb_full_adder	Process	-
#vsim_cap...		Capacity	Statistics

Objects

Name	Value	Kind	Scope
A	1'h0	Regi...	Internal
B	1'h0	Regi...	Internal
C	1'h0	Regi...	Internal
Z0	1'h0	Net	Internal
Z1	1'h0	Net	Internal

Wave - Default

Msgs
/tb_full_adder/A
/tb_full_adder/B
/tb_full_adder/C
/tb_full_adder/Z0
/tb_full_adder/Z1

Now 9 ns

Cursor 1 0 ns

0 ns 2 ns 4 ns 6 ns 8 ns 10 ns 12 ns 14 ns 16 ns

Wave tb_full_adder.v full_adder.v

Transcript

```
# 2 A=0 B=0 C=110
# 3 A=0 B=1 C=010
# 4 A=1 B=1 C=110
# 5 A=1 B=1 C=000
# 6 A=1 B=0 C=010
# 7 A=1 B=1 C=110
# ** Note: $finish : C:/Modeltech_pe_edu_10.4a/examples/tb_full_adder.v(16)
# Time: 9 ns Iteration: 0 Instance: /tb_full_adder
# 1
# Break in Module tb_full_adder at C:/Modeltech_pe_edu_10.4a/examples/tb_full_adder.v line 16
VSIM 9>
```

0 ns to 16 ns Project: Full Adder Now: 9 ns Delta: 0 sim:/tb_full_adder/#INITIAL#5

Type here to search

8:37 AM 10/27/2020

4) Circuit Diagram

