

MICROWAVE PHOTONIC INTERFERENCE
CANCELLATION: RF ANALYSIS, III-V AND SILICON
INTEGRATION, DEVELOPMENT OF BALANCED AND
HYBRID ARCHITECTURES

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Abstract

Dedicated to my family

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Appendix A

Packaging Process

This appendix highlights the packaging approach, recipes, and procedures developed to interface with photonic integrated circuits within the Princeton University's Lightwave Lab from 2017 to 2023.

Authors: Eric C. Blow, Bert Harrop, Simon Bilodeau, Thomas Ferreira de Lima

A.1 Introduction

Packaging, whilst often overlooked, plays a critical role in the overall performance of integrated circuits. A next-generation processor requires equally state-of-the-art interfacing or performance is unnecessarily degraded. PICs enable ultra-wide instantaneous bandwidths of 10 GHz and frequency tunability from MHz to 100 GHz. This unprecedented bandwidth performance generates a novel electrical interfacing requirement [1, 2]. Historically in the Lightwave Laboratory, RF electrical I/O on PICs were probed, while this is sufficient for low number of I/O (≤ 6 ; 3 sides of GSGSG RF probes) and for lab bench experiments, the technique does not support commercialization or growing chip complexities. A fully packaged solution increased functionality through interfacing with co-packaged CMOS and control electronics.

Traditional wirebonding techniques can support high-speed connections up to 100 GHz. This performance is achieved by keeping wirebond lengths short and pairing the bonds with

impedance-matched transmission lines, resulting in narrowband gain at the operating frequency. Wedge wire bonding can be optimized to achieve 30 GHz instantaneous bandwidth (IBW), strip wire bonding can increase IBW to 50 GHz, but beyond that requires the transition to flip-chip bonding [3, 4].

In addition to the bandwidth consideration of electrical packaging PICS, the growing complexity of neuromorphic PICs required an increase in the amount and density of electrical I/O. Immediately after demonstrations of a small PNN with 2 neurons, the size of the PNN was limited due to packaging. Electrical probing limited the electrical I/O to 48 connections (16 DC probes over 3 sides of the PIC, 1 side reserved for optical I/O). A simple approximation for electrical I/O required is shown in eqn. /refeqn:IOcount. Two connections, ground and signal, per weight and neuron bias. For an all-to-all connected PNN, the number of weights scale with the number of neurons squared, and lastly each neuron requires a bias. Therefore, probing could only support a PNN with four neurons.

$$\text{Number of I/O} = 2[\text{Weights} + \text{Neuron Bias}] = 2[(\text{Neurons}^2) + \text{Neurons}]. \quad (\text{A.1})$$

Transitioning from probing to wedge wire bonding, scales available I/O from number of 3*probe size to a function of the perimeter length and therefore enables larger networks. For an electrical pad of width $100\mu\text{m}$ and a pitch of $150\mu\text{m}$, a standard 3mm by 6mm PIC size could support 100 electrical I/O and therefore a PNN size of 6. With perimeter wire bonding, multiple rows can be implemented if they are interlaced and separated by height. We developed a three-row recipe that increased the electrical I/O count to 300 and therefore a PNN size of 11. Multiplexing signals and common grounds could increase the number of neurons by a few. However, to exceed this number requires using the entire chip surface for electrical I/O instead of simply the perimeter. The PNN complexity scales with the area of the chip, but the electrical I/O with wire bonding scales with the perimeter. The discrepancy in these scaling laws leads to inefficiencies. Therefore,

to increase the size of PNNs further requires the transition to flip-chip bonding or co-integrated CMOS control.

During this , the Lightwave Laboratory transitioned our packaging approach from probing PICs to a fully wire-bonded approach which supports 20 GHz RF connections, 300 of DC control I/O, and epoxied optical coupling.

A.2 Packaging Approach

(Refer to Chapter 7: Silicon MPC for a detailed example)

Figure A.1 below summarizes the packaging approach for interfacing with the silicon microwave photonic canceller (MPC). The goals of the packaging approach were to have RF and DC electrical interfaces with two cancellers on-chip simultaneously. Physically secure the chip in a planar orientation while having sidewall access for optical edge coupling. Lastly, PICs require temperature control.

The MPC PIC has 45 electrical DC connections for two separate cancellers, 2 RF outputs which support DC-GSG-DC probes, and 2 RF inputs which support GSGSG probes. The on-chip electrical DC pad array consists of two rows of 23 and 22 aluminum pads, $100\mu m$ wide by $200\mu m$ long, pitched $150\mu m$. The MPC PIC has 19 relevant optical edge couplers but only requires a maximum of 10 to be interfaced simultaneously.

The MPC PIC is first interfaced with a custom-fabricated glass expander with an identical DC pad array to that which is on the PIC. This helps to keep the wire bonds as short as possible and parallel to one another. The expander pad array is then fanned out to a lower density single row pad array. This array is matched to a custom-made chip carrier which can be soldered to a printed circuit board. The chip carrier is then diced on one side in order to support optical edge coupling.

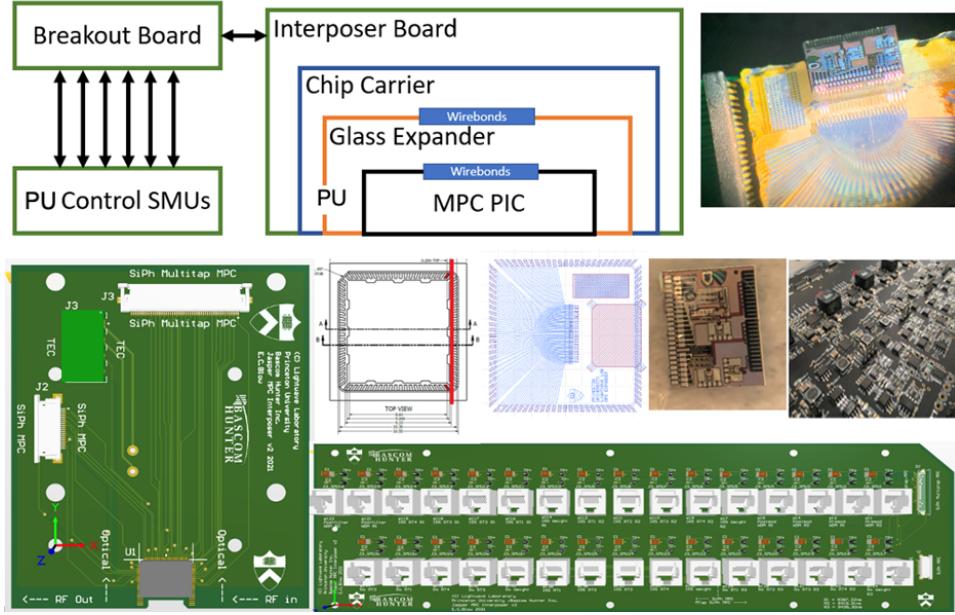


Figure A.1: Diagram of packaging approach for silicon microwave photonic canceller

A.3 Fabrication of Glass Expander

Author and Recipe Developer: Simon Bilodeau

The fabrication of an expander chip is required to transition from the high density electrical I/O of the PIC to the lower density electrical I/O of a chip carrier. This enables higher density I/O, shorter wirebonds, and multiple rows of wirebonds. Currently, these chips are only utilized passive routing for DC connections. Although, it would be advantageous to surface mount capacitors on this packaging layer for improved RF performance. The following recipe was designed for 4" silica wafer with aluminum traces. Shown in Figure A.2 below, is an example of a glass expander design used for a microwave photonic canceller.

1. Write the 4" or 5" chrome hard mask **negative** using a direct write lithography tool.
2. Develop, etch chrome, and strip resist in TMAH tank.
3. Perform a solvent clean on the wafer with acetone and isopropanol followed by an oxygen plasma clean (5 min, 500 W O₂ ashing).
4. Perform a 5000A aluminum deposition.

5. Spin AZ1518 resist (4000 rpm, 40 seconds) followed by a 1 min soft bake at 95°C.
6. Expose wafer with standard dose and time for AZ1518.
7. Develop in AZ 300 MIF for 40s and inspect result under the microscope.
8. Run a plasma descum (5 min, 200 W O₂ ashing) [Recommended but optional].
9. Aluminum Etch Type A at 50°C for a few minutes until change is visible.

This procedure is updated from the recipe presented by the authors in Thomas Ferrier de Lima’s “Neuromorphic Computing with Silicon Photonics” (2022) [5]. The recipe was modified by change from an aluminum deposition of positive mask and lift-off to aluminum deposition of negative mask and aluminum etch. This transition resulted in a faster process, higher quality traces, and higher yields.

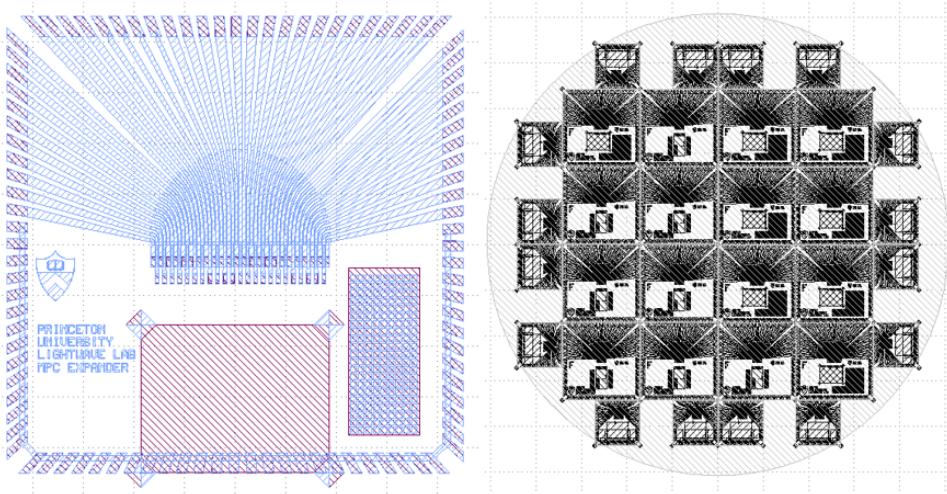


Figure A.2: Expander designs for fabricated 4” silica wafer

A.4 ADT Dicing Expander

After the customized expander wafer is fabricated within MNFL Cleanroom, the glass or silicon expander wafer must be diced to remove the experiment-specific expander. This process of dicing a 4-inch wafer is standard and requires a few steps, stated below.

1. Mount wafer with the ADT metal ring and $90 \mu m$ tape.
2. Measure the height of the tape and confirm $90 \mu m$.
3. Flip mounted wafer and apply a second layer of tape to top of wafer. This is done to prevent the expanders from being scratched in the dicing process or afterwards while stored.
4. Define the appropriate recipe for the ADT Dicing saw.
 - (a) Recipe: Si_Dice or Glass_Dice
5. Adjust Recipe with the actual height of the tape using the Mitutoyo Height Gauge minus 10 microns and also define the 0 degree and 90 degree dicing index.
6. Insert Correct Blade:
 - (a) 2045 Blade for silicon
 - (b) ADT Resin Blade for glass
7. System Init*
8. Calibrate blade*
9. Calibrate Y-offset*
10. Partial cuts plus manual alignment to dice wafer*. On the ADT Dicing, be careful using full wafer cut; There is no confirmation, and the entire wafer will cut after index definition.

*Use Tool Manual for additional detailed instruction.

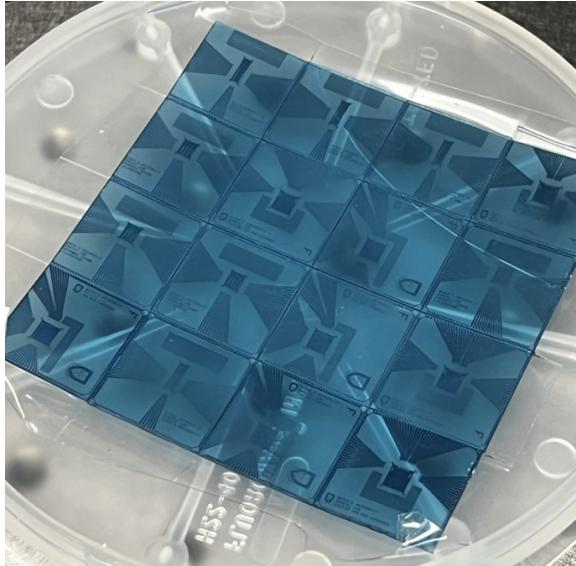


Figure A.3: Diced glass expander used for photonic integrated circuit packaging

A.5 Silicon Photonic Integrated Circuit Die Dicing – Z-Cut

In integrated photonic prototyping, research groups will leverage multi-project wafer (MPW) runs. The foundry will offer many customers an 8-inch wafer to share, resulting in a user getting 10s of copies of a standardized sized die (commonly 3mm by 8mm). Research groups can utilize this space more effectively by further dividing the chip area into groups of experiments. The division of a single PICs into sub-PICs is highly beneficial for two reasons. Firstly, an increased copy of available chips per experiment, without further dicing of the PIC such as 32 copies of a PIC with 4 experiments would result in 8 copies per experiment. This is due to an inability to package all experiments simultaneously. Secondly, as shown in the figure below, the sub-grouping of experiments significantly increases the available chip parameter for electrical and optical I/O.

Performing such a dice on a small sample using a wafer dicing saw requires custom techniques and recipes as to not damage or dislodge the sample. The Z-cut recipe was developed to bring the dicing down in the Z direction over top of the sample. Rather than dicing from the side such as a traditional dicing saw recipe. The recipe is designed to cut with a much slower movement to reduce horizontal forces. For large samples the recipe allows for travel in the positive x-direction (right) after the initial cut is made.

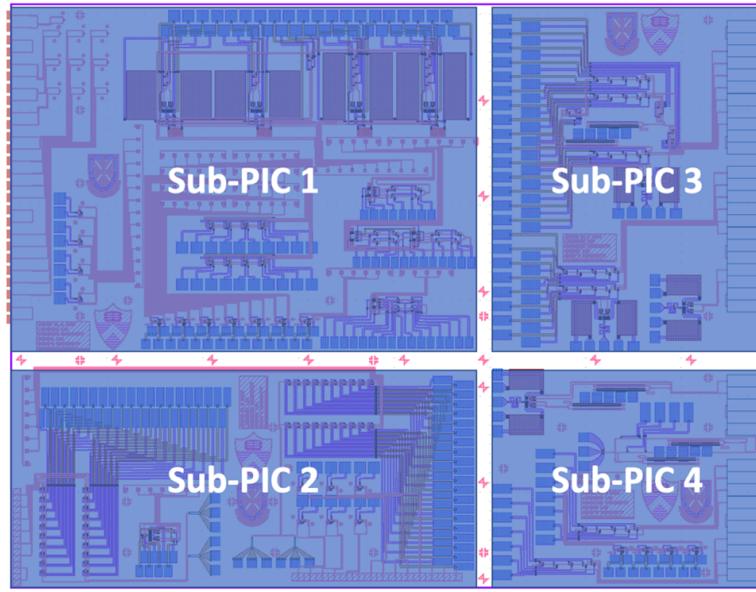


Figure A.4: Lightwave Lab’s 6 mm by 10 mm Photonic Integrated Circuit (PIC) sub-grouped into four sub-PICs. The $100 \mu m$ dicing lanes are indicated by alignment markers.

This is an updated procedure to the one developed by the authors presented in Thomas Ferrier de Lima’s “Neuromorphic Computing with Silicon Photonics” (2022)[5].

A.5.1 Carrier Wafer Preparation

Optional: Prepare a carrier wafer with guidelines to make finding the sample using the ADT significantly easier.

1. Take a relatively clean bulk silicon carrier wafer and use a tex wipe wet with acetone to remove any debris or previous wax from top and back.
2. Mount the wafer with the tape and metal ring.
3. Measure the surface of the carrier wafer and set the cutting depth of the recipe to $20 \mu m$ before the surface of the wafer.
4. Load the carrier wafer into the ADT dicing saw and define the recipe as the standard Si dicing recipe, e.g. Si_{Test} .

5. Follow the ADT manual to perform the following $20 \mu\text{m}$ dice.
6. Avoid dicing too deeply, beyond $20 \mu\text{m}$ can scribe the wafer and encourage breaking along the lattice dislocation line.
7. Remove sample and clean excess tape residue with acetone.

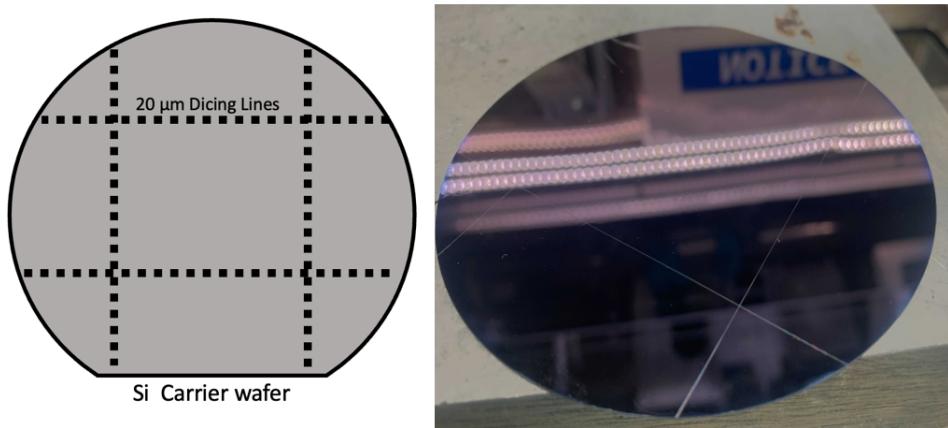


Figure A.5: Diagram of guidelines on Si carrier wafer (left) Example of Si carrier wafer with etched guidelines (right)

Sample Preparation

1. Take a prepared carrier wafer and acetone wipe the wafer. Fold acetone wipe to only clean with a clean side of the wipe.
2. Roughly clean back with acetone wipe using the same technique before mounting as carrier wafer will dislodge while dicing if dirty.
3. Heat carrier wafer at 165°F (74°C).
4. Use razor to chisel small shards of crystalline wax from tube
5. If Z-cutting multiple samples orient them so there is no chance of the dicing blade hitting more than one sample at a time.

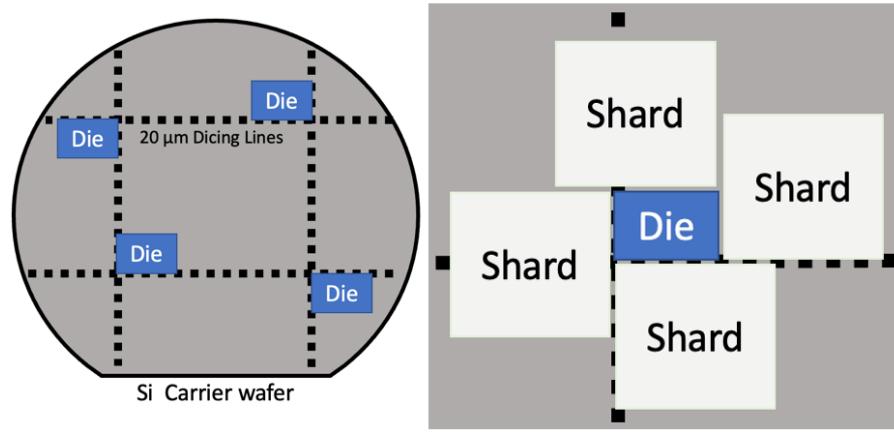


Figure A.6: Illustration on how to place multiple samples for Z-cut (left) and how to support a die with space Si or Glass shards (right).

6. Put one large shard where the PIC will be located, where all four support shards are located, and the corners where support shards interface with the chip. Place carrier wafer on 80°C hot plate. Mid-range melting point of 165°F (74°C).



Figure A.7: Placing crystalline wax shards where sample and supports should be located (left) Image of mounted sample (right)

7. Ensure chips are loaded onto carrier with same orientation locked into place with 3-4 sides of silicon shards, shown below.
 - (a) If there are edge couplers, you can avoid supporting them with a fourth shard to protect the edge couplers from mechanical damage. There is a risk tradeoff between too poorly supporting the chip or damaging the interface.

8. Precisely clean back, 1 wipe per surface of the acetone-soaked Tex wipe to avoid dislodgement.

9. Measure Z in different places to make sure it's flat with the Mitutoyo Height Gauge.

(a) Example of Measuring before cut:

i. Tape height = 120-180 μm

ii. Tape + Carrier height = 700-800 μm

iii. Tape + Carrier + Chip = 2500 – 2700 μm

iv. Cut down to 600 μm (100 μm below your carrier height)

10. Roll tape on the carrier without the wafer.

11. Slowly apply carrier wafer to tape.

(a) Place wafer underneath, making sure there are no gaps. Start with one edge of the wafer and stick the tape gradually and gently with your thumb across the wafer, avoiding bubbles.

Changes to recipe:

1. Previously used beeswax

(a) Problem: beeswax is weaker than crystalline wax.

2. Previously used wax shards on top of sample

(a) Problem 1: Too little wax sample is not secure, and sample can be dislodged.

(b) Problem 2: Too much wax is hard to see through and therefore hard to align.

(c) Problem 3: Too much wax causes a high wax profile which wears heavily on blade.

i. i. Previously, height was reduced by using an acetone-soaked wipe Even though successful, there is a need for further reduction. The risk of wax height is due to

the 30,000 RPM saw melting the wax on top as cutting and then the wax can get onto the side of blade.

Z-cut Dice

1. Load the carrier into the ADT*.
2. Select the appropriate blade.
 - (a) Blade 2045 for Silicon PICs
 - (b) $60 \mu m$ cut width
3. Recipe for Z-cut: *ZcutCMOS* (set cut depth and wafer thickness).
4. Change recipe to include your calculated cut depth on both cut angles
5. Decide if you need to increase the cut distance. This may be necessary for dicing larger chips.
6. Perform Y-offset.*
7. Perform partial wafer alignment (skip second angle).*
8. Partial wafer cut. Access this option via manual, cut, partial. Use animation mode. After selecting it, assuming the wafer alignment is done, proceed with next-next-next-finish-finish.*
9. After the cut, the ADT tries to unload wafer. Cancel to abort and move to the next cut instead.*

Cleaning

1. Heat chip to $80^\circ C$ and remove sample with tweezers.
2. Slide sample into acetone bath for 60 seconds.
3. Slide onto Tex wipes to clean with Isopropyl Alcohol (IPA).

4. Repeat cleaning if there is still crystalline wax debris.

5. Dry with Nitrogen Gun.

*Use Tool Manual for additional detailed instruction

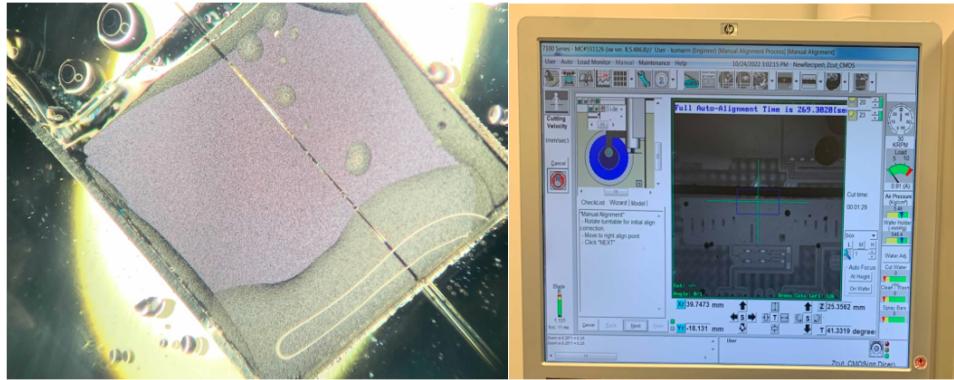


Figure A.8: Diced practice sample with improved recipe (left) and ADT dicing saw display after successful z-cut is completed (right).

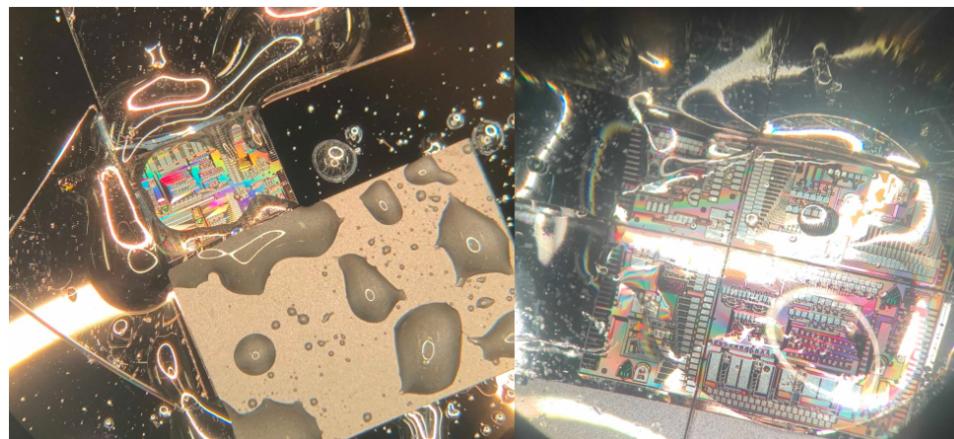


Figure A.9: Previously diced samples. Only covering edges with wax increased risk of sample dislodgement from the carrier (left). Samples with too much wax on the sample caused wear to the blade and was hard to align, even after significant removal with acetone Tex wipe (right).

A.6 Tresky Pick and Place (P&P)

A.6.1 Direct to chip carrier (Low I/O Count):

Direct pick and place (p&P) to Chip carrier without expander chip. This technique is fast and effective for small-scale experiments with low I/O count (less than 15). The I/O count is limited in this technique because the DC pad array on-chip and the chip carrier have a mismatched pitch. Therefore, the angles generated by the wirebonds will eventually become too great and wirebonds can often short. Additionally, this is only recommended for DC connections due to increased wire bond length relative to packaging with the glass expander or a custom carrier. This increased wire bond length results in a higher inductance which would cause high attenuation if these were used for AC signal.

1. Select DIP package which matches the needs of PIC.
2. Secure DIP to grated holder with the amber cleanroom electrical tape due to the high melting temperature.
3. Vacuum metal grated holder to Tresky flip chip bonder main stage.
4. Program 28 Pick and Place (P&P)
5. Parameters
 - (a) Force:
 - i. Pick: 30g
 - ii. Place: 250g
 - (b) Time:
 - i. Pick: 250 ms
 - ii. Place: 250 ms
 - iii. Scrub: 0 ms

- iv. Del. S: 0 ms
 - (c) Height:
 - i. Program dynamically due to height of dip and chip
 - (d) Puff time: disable
 - (e) Puff offset: disable
 - (f) Speed:
 - i. Pick down: 1 mm/s
 - ii. Pick up: 5 mm/s
 - iii. Place down: 1 mm/s (as slow as possible)
 - iv. Clearance: 40 mm/s
 - (g) QH Place force (applies force while heating and curing epoxy)
6. Define heat profile based on silver epoxy specification sheet.
- (a) Using H20E EPO-TEK Silver conductive epoxy Product No. 16014
 - (b) 120°C for 15 min.
 - (c) Make sure TEC unit is enabled or Tresky will stall out and require reboot.
7. Define height parameters using microscope and shortcut Tresky buttons.
8. Dry run with dummy Sample, Pick and Place with Quick Heat off to check heights and forces but not have to wait for heating cycling.
9. Remove metal grated holder with dip package from Tresky.
10. Apply blue tape to entire surface of dip and cut a rectangle hole approximately the same size as the chip being packaged .
11. Mix the two-part epoxy on a glass slide and using a small cotton swab apply a thin layer over the blue tape.

12. Remove the blue tape and left behind is the square epoxy.
13. Remount the metal grating holder to the Tresky flip chip bonding
14. Turn Quick Heat On and run the Pick and Place programming, aligning, and then curing the sliver epoxy.
 - (a) Align the sample to the DIP package with reflection of the samples. Aim for the mid-point between the nozzle and the reflection. This point is where the chip edge will meet the chip.

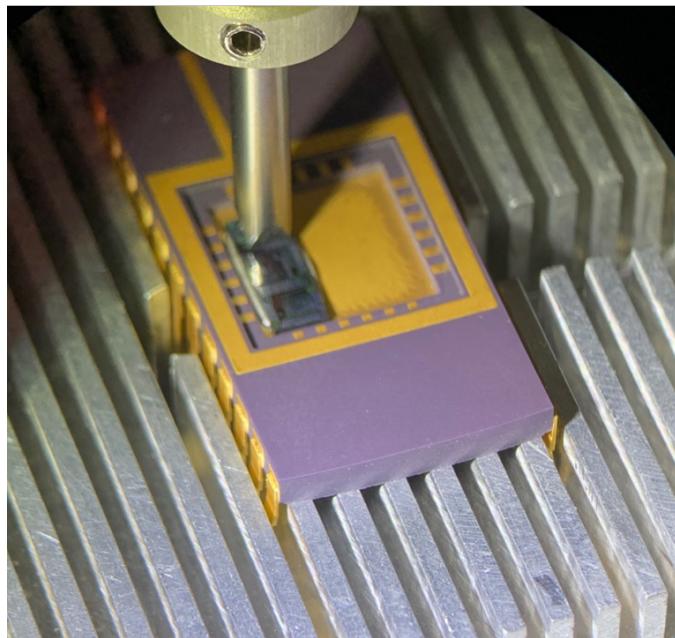


Figure A.10: DIP carrier mounted to metal grating holder. Tape corners for added stability

A.6.2 PIC, Expander, Chip Carrier stack (High I/O Count):

Discussion: There is a risk trade-off between the soldering chip carrier to the PCB board before wirebonding or afterwards. My recommendation is to bond first for small I/O prototyping and to solder to first for large scale I/O.

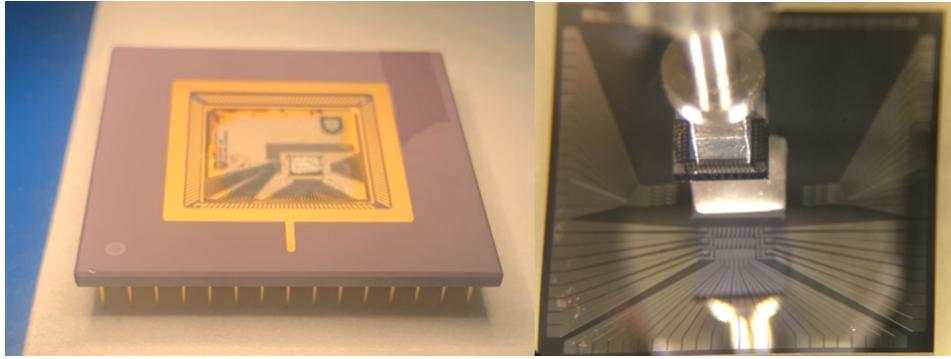


Figure A.11: Sample with silver epoxy applied (left) and sample with PIC being placed by Tresky P&P (right)

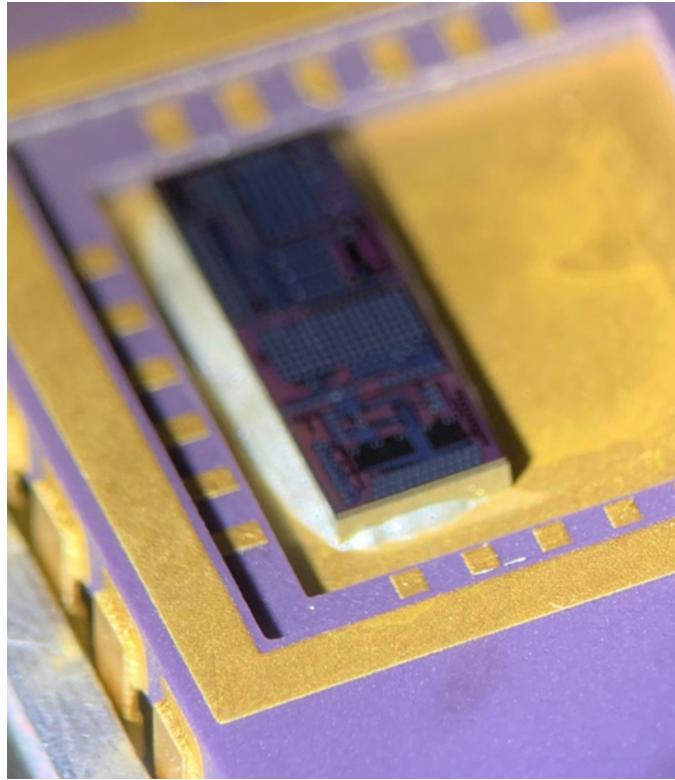


Figure A.12: PIC epoxied directly to DIP chip carrier.

If one was to first solder the chip carrier, there would be no risk of damaging the bonds while soldering. This process requires heat and mechanical manipulation, which could result in accidental damage to the bonds. There would also be the risk of damaging the FR4 PCB board during the curing process. Upon detailed observation, discoloration and smoking took place initially but stabilized after 15 seconds. Neither damage nor degradation of performance was observed.

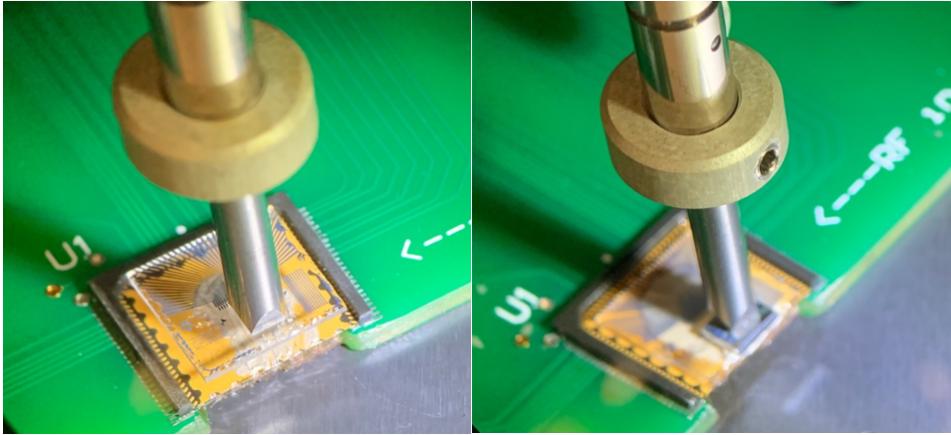


Figure A.13: Glass expander being placed and epoxied to custom chip carrier (left), PIC being placed and epoxied to glass expander (right).

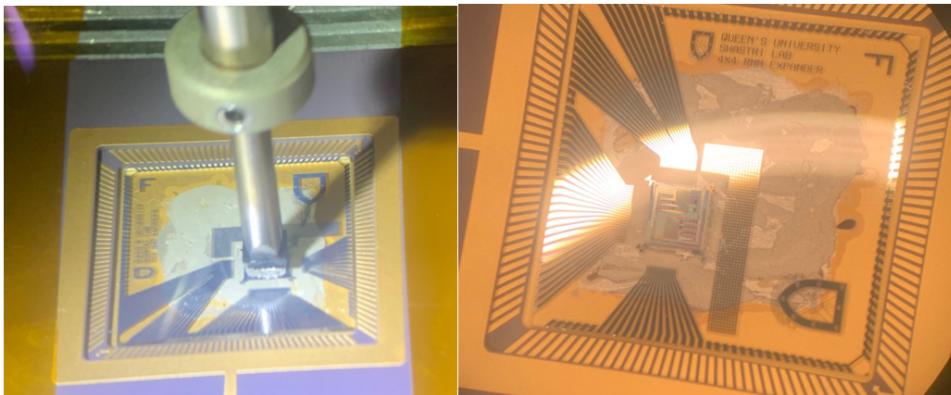


Figure A.14: Chip Carrier, Glass Expander, PIC epoxying procedure.

The primary problem with soldering first on the small I/O DIP packages is twofold. Firstly, it is difficult to achieve the security and planarization required for wirebonding in a standard through-hole or pluggable standardized chip carrier package. Additionally, not only must the carrier be planar, but also the board must be. If the board is planned significantly in advance and there are mounting holds which match the Tresky and Questar mounts to stabilize the board and chip carrier, soldering first is recommended. The sample must be absolutely secure and planar or the bonding yield will be very poor (< 80%). For prototyping small I/O counts, using the metal grating and soldering afterwards is an easier and more flexible approach. For large I/O counts, plan ahead and incorporate mounting holds and solder first.

A.7 Questar Automatic Wedge Wire Bonder

Wire bonding is a tedious but critical part of the packaging procedure. The PICs, glass expanders, and chip carriers were electrically interfaced with $25 \mu m$ wedge wire bonds. The challenge within this research was two-fold. Firstly, the authors needed to achieve a high yield to successfully bond 300+ wire bonds without failure. This was due to a high number of electrical I/O and small pad sizes on the PIC which only allowed for one bonding attempt. Second, given the limited chip perimeter, the authors developed a three-row recipe to three-fold increase the amount of possible electrical I/O. There was a critical need to scale the size of the photonic neural network. The yield of the wire bonding is dependent on:

1. Requirement: Planarization of the PIC and glass expander.
 - (a) Solution: the use of the Tresky for Pick and Place.
2. Requirement: Firm mounting of sample to Questar.
 - (a) Solution: Design custom PCBs with drill holes matching the mounting of the Questar.
3. Requirement: Parallel Wirebonds
 - (a) Solution: Design glass expanders in Princeton Cleanroom with matching pad arrays to that which are on the PIC.
4. Requirement: Clean surfaces and quality metalization.
 - (a) Solution: Cleaning pads before bonding and optimized glass expander recipe (see Appendix A3)

By applying these solutions, the authors developed a packaging recipe with a percent yield of more than 99%. To achieve the three rows of wire bonds for the high density photonic neural network, the authors fabricated dummy replicas of the PICs and optimized the physical parameters of the wire bonds by trial and error. The result of the recipe development is stored in memory on

the Tresky and provided in the Table 1 below. Lastly, the authors determined the inclusion of a pad array “graveyard” on the glass expander was critically important. These additional free pads can be used for calibration, ensuring proper bonding operation after a failed bond, and removal of the wire bond tail caused by re-threading.

Sample and Equipment Preparation:

1. Clean pads with acetone, if possible, and/or at least IPA to remove any potential organic debris
2. Firmly and securely mount the sample to the Questar Wire Bonder.
 - (a) This can be done with metal grates if a small through-hole I/O chip carrier is used.
 - (b) Ideally, the designer planned for wire bonding and the sample is on a custom PCB with 4 holes created which match the mounting brackets of the Questar.
 - i. Screw hole: 9 AWG (2.9 metric)
 - ii. Horizontal separation: 4 cm
 - iii. Vertical separation: 4.5 cm
3. Unthread the wire from the wedge tool and calibrate for x-y position and ultrasonics, following the manual.
 - (a) This calibration should be done on the pad array graveyard on glass expander.
4. Select the PIC row or expander to chip carrier recipe.
5. Begin bonding in accordance with the equipment manual.
6. Check pad footprint width to ensure it meets the 1.5x wire bond width which ensures appropriate levels.
 - (a) If too wide lower ultrasonic power, if too narrow increase ultrasonic power

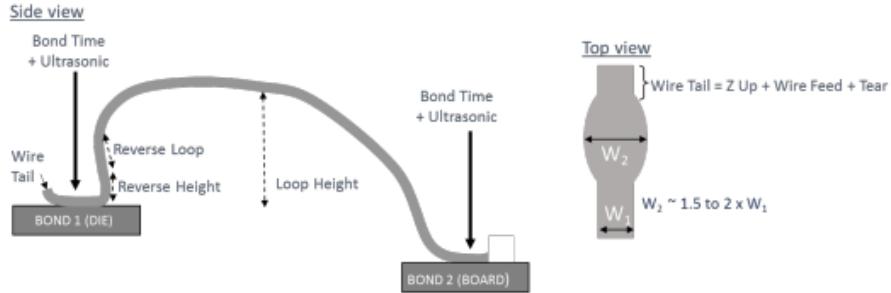


Figure A.15: Wedge wire bond parameter definitions and expected range. Source: Princeton MNFL

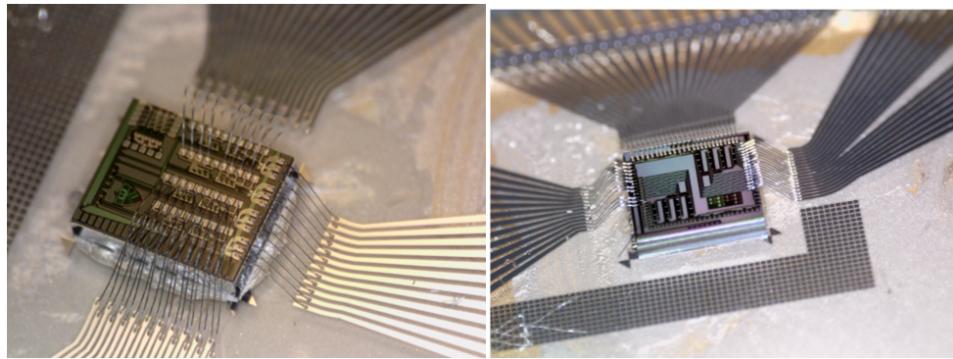


Figure A.16: Two fully packaged photonic integrated circuits demonstrating high density electrical I/O. Optical I/O is not shown.

Table A.1: **Questar Wire bond Recipes: Expander to Chip Carrier**

Parameter	Value for glass expander
Bond 1 CV Height	35 mils
Bond 1 Overtravel	1 mils
Bond 1 Bond Time	60 ms
Bond 1 Ultrasonics	50 power
Loop Reverse Height	10 mils
Loop Reverse Loop	10 mils
Loop Height	35 mils
Bond 2 CV Height	35 mils
Bond 2 Overtravel	1 mils
Bond 2 Bond Time	55 ms
Bond 2 Ultrasonics	54
Z up	2.1 mils
Wire Feed	2.8 mils
tear	1.5 mils

Table A.2: Questar Wire bond Recipes: PIC Row 1

Parameter	Value for AMF	Value for IME
Bond 1 CV Height	35 mils	35 mils
Bond 1 Overtravel	1 mils	1 mils
Bond 1 Bond Time	50 ms	50 ms
Bond 1 Ultrasonics	49 power	50 power
Loop Reverse Height	10 mils	10 mils
Loop Reverse Loop	10 mils	10 mils
Loop Height	36 mils	36 mils
Bond 2 CV Height	35 mils	35 mils
Bond 2 Overtravel	1.2 mils	1.2 mils
Bond 2 Bond Time	60 ms	60 ms
Bond 2 Ultrasonics	55 power	55 power
Z up	2.6 mils	2.6 mils
Wire Feed	2.6 mils	2.6 mils
tear	1.5 mils	1.5 mils

Table A.3: Questar Wire bond Recipes: PIC Row 2

Parameter	Value for AMF	Value for IME
Bond 1 CV Height	35 mils	35 mils
Bond 1 Overtravel	1 mils	1 mil
Bond 1 Bond Time	62 ms	62 ms
Bond 1 Ultrasonics	49 power	56 Power
Loop Reverse Height	12 mils	12 mils
Loop Reverse Loop	20 mils	20 mils
Loop Height	40 mils	40 mils
Bond 2 CV Height	35 mils	35 mils
Bond 2 Overtravel	1.2 mils	1.2 mils
Bond 2 Bond Time	65 ms	65 ms
Bond 2 Ultrasonics	55 power	59 power
Z up	2.3 mils	2.3 mils
Wire Feed	3 mils	3.2 mils
tear	1.5 mils	1.5 mils

Table A.4: Questar Wire bond Recipes: PIC Row 3

Parameter	Value for AMF	Value for IME
Bond 1 CV Height	35 mils	35 mils
Bond 1 Overtravel	1 mil	1 mil
Bond 1 Bond Time	60 ms	60 ms
Bond 1 Ultrasonics	49 power	40 power
Loop Reverse Height	35 mils	35 mils
Loop Reverse Loop	33 mils	33 mils
Loop Height	58 mils	58 mils
Bond 2 CV Height	35 mils	35 mils
Bond 2 Overtravel	1 mil	1 mils
Bond 2 Bond Time	63 ms	63 ms
Bond 2 Ultrasonics	55 power	40 power
Z up	2.3 mils	2.3 mils
Wire Feed	3 mils	3 mils
tear	1.5 mils	1.5 mils

Table A.5: Questar Wire bond Recipes: Static Parameters

Static Parameters	Value for AMF	Value for IME
	Expander to Chip Carrier	
Bond 1 and 2 CV Height	35 mils	35 mils
Bond 1 and 2 Contact Velocity	100 mils/sec	100 mils/sec
Loop Stretch	0 mils	0 mils
Rise to Loop	0 mils	0 mils
Clamp Close	CV Height 2	CV Height 2
Reset Height	35 mils	35 mils

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Bibliography

- [1] L. Ranno, P. Gupta, K. Gradkowski, R. Bernson, D. Weninger, S. Serna, A. M. Agarwal, L. C. Kimerling, J. Hu, and P. O'Brien, “Integrated photonics packaging: Challenges and opportunities,” *ACS Photonics*, vol. 9, no. 11, pp. 3467–3485, 2022.
- [2] L. Zimmermann, G. B. Preve, T. Tekin, T. Rosin, and K. Landles, “Packaging and assembly for integrated photonics—a review of the epixpack photonics packaging platform,” *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 17, no. 3, pp. 645–651, 2010.
- [3] W. Heinrich, M. Hossain, S. Sinha, F.-J. Schmükle, R. Doerner, V. Krozer, and N. Weimann, “Connecting chips with more than 100 ghz bandwidth,” *IEEE Journal of Microwaves*, vol. 1, no. 1, pp. 364–373, 2021.
- [4] A. Hassona, Z. S. He, V. Vassilev, C. Mariotti, S. E. Gunnarsson, F. Dielacher, and H. Zirath, “Demonstration of+ 100-ghz interconnects in ewlb packaging technology,” *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 7, pp. 1406–1414, 2019.
- [5] T. Ferrier de Lima, “Neuromorphic computing with silicon photonics,” *Princeton University*, 2022.