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## **PROFESSIONAL**

Sony Electronics Inc.

Rochester, NY

Staff Mixed Signal IC Design Engineer

July 2018 - Present

- Involved in the Dynamic Voltage Scaling (DVS) power management architecture for next-gen image sensors
- Responsible for architecture and design of a sub-uW unconditionally stable capacitorless LDO supporting up to 10mA of load current in 40nm to support DVS efforts
- Responsible for the design of circuits to interface with a pixel array on a low-power CMOS imaging product Synaptics Inc.

  Rochester, NY

Sr. Mixed Signal IC Design Engineer

February 2014 - July 2018

- Experience implementing various capacitive sensing front-ends for touch and fingerprint applications, with a focus in low-noise and low-power architectures
- Designed and implemented a small area and noise-optimized capacitive fingerprint AFE to enable a 50% in die cost without impacting performance in 55nm
- Designed an innovative continuous-time demodulation topology for SNR improvement in fingerprint AFEs
- Analyzed the impact of non-linearities in competing fingerprint AFE architectures to determine interference susceptibility, and proposed solutions to mitigate this risk
- Designed a noise-optimized switched capacitor demodulator and filter for high-volume touch AFEs
- Designed a passive mixer with built-in DAC capable of arbitrary waveform mixing
- Architected and implemented a sub-µW power management architecture to reduce system power by 30% utilizing a long (100s of ms) sample-and-hold bandgap architecture
- Designed a nW-level time-to-digital (TDC) temperature sensor capable of sub-1℃ resolution
- Designed and evaluated a low-jitter 1Gbps receiver front-end for MIPI DSI
- Led efforts to evaluate, track, and debug new silicon for risk evaluation of metal or all-layer spin
- Experience working closely and effectively with multidisciplinary teams to ensure smooth silicon design all the way through to production
- Focus on fundamental understanding of circuits for architectural comparisons is a strength

Synaptics Inc. Rochester, NY

Analog Design and Silicon Validation Contractor

June 2013 - February 2014

Performed extensive verification and validation on LDOs, VCOM drivers, LCD level shifters, and MIPI DSI

## **EDUCATION**

## **Rochester Institute of Technology**

Rochester, NY

M.S. and B.S. in Electrical Engineering, August 2013

GPA: 4.0

**Thesis** 

Stability Analysis of Switched DC-DC Boost Converters for Integrated Circuits

• Investigated small-signal modeling and stability requirements for boost converters, as well as a variety of OTA-based controller topologies, in order to aid in the measurement of boost converter stability on multiple ASICs. Also investigated the use of optimization algorithms as a way to improve controller design.

## PATENTS AND PUBLICATIONS

- US 9,780,736 Temperature compensated offset cancellation for high-speed amplifiers Grant Oct. 3, 2017
- US 9,817,428 Current-mode Bandgap Reference Grant Nov. 14, 2017
- US 10,394,386 Interference Detection Grant Aug. 27, 2019
- US 15/685,937 Mixer Circuit Pending Feb. 28, 2019
- US 15/885,769 Oscillator Temperature Coefficient Adjustment Pending Jan. 31, 2018