

PROFESSIONAL

Sony Electronics Inc.

Rochester, NY

Staff Mixed Signal IC Design Engineer

July 2018 - Present

- Involved in the Dynamic Frequency and Voltage Scaling (DFVS) power management architecture for next-gen stacked-chip CMOS image sensors in 40nm
 - Led effort to introduce and implement a new low-jitter 600 MHz oscillator architecture with 50% power saving over existing PLL-based implementations, and also eliminating the need for external oscillator references
 - Performed architecture study on potential LDO designs to use for next-generation ULP CMOS imaging products
 - Architected and designed a 5-uW unconditionally-stable capacitorless-LDO supporting up to 10mA of load current
 - Implemented an innovative scheme to handle undershoot during voltage-domain crossover
- Responsible for the design of circuits to interface with a pixel array for a stacked-chip low-power CMOS imaging product in 40nm
 - Required generation of an accurate pixel model to gauge sensitivity to adjacent column coupling, as well as transient performance during image capture
 - Used unique multiplexing scheme to be able to intelligently bin adjacent columns for power reduction during motion detection capture
 - Specified testing scheme to ensure each multiplexer per column was void of defects with negligible contribution to total test time

Synaptics Inc.

Rochester, NY

Sr. Mixed Signal IC Design Engineer

February 2014 - July 2018

- Worked on architecture, design, and bring-up of a low-area, noise optimized AFE for capacitive fingerprint sensing in 55nm achieving 50% cost reduction over existing solutions
 - Transistor-level design of a low-noise current conveyor with innovative mixing topology meant to improve SNR with minimal overhead (US 15/685,937)
 - Performed interference susceptibility analysis on existing and proposed architectures and designed an innovative mitigation technique that took advantage of existing system design for improved performance (US 10,394,386)
 - Responsible for initial prototyping of architecture in silicon, prior to introduction into a part
 - Led effort to evaluate, track, and debug A0 silicon to enable rapid evaluation of needs for metal or all-layer spins
 - Designed subsystems for first market introduction of Touch and Display Driver Integrated Circuits (TDDI). Initial prototypes in 130nm, mass-produced parts in 55nm.
 - Designed noise-optimized discrete-time demodulator and filter for mass-produced capacitive touch front-ends
 - Designed an innovative bandgap topology to enable a more efficient power management strategy for the chip (US 9,817,428)
 - Led the introduction of a 1Gbps MIPI DSI receiver architecture, utilizing continuous-time linear equalization, to replace existing solution and proposed an integrated offset calibration scheme (US 9,780,736)
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- Proposed, architected, and implemented a prototype sub-uW power management architecture for next-generation fingerprint sensors to aid in >30% power reduction over existing solutions (55nm)
 - Work involved brand-new designs for bias generation circuits, oscillators, and long sample-and-hold bandgap references (>1ms hold time)
 - Designed a nW-level time-to-digital (TDC) temperature sensor capable of sub-1°C resolution as measured in silicon
 - Designed an innovative adaptive bias mechanism for POR circuits to enable fast reaction time while only taking up a few nW of total power budget (US 16/378,853)
- Experience working closely and effectively with multidisciplinary teams to ensure smooth silicon design all the way through to production (involved in seven unique tape-outs while at Synaptics)

Synaptics Inc.

Rochester, NY

Analog Design and Silicon Validation Contractor

June 2013 - February 2014

- Performed extensive verification and validation on LDOs, VCOM drivers, LCD level shifters, and MIPI DSI

Intel Corporation

Hudson, MA

Circuit Design Co-op

March 2012 - August 2012

EDUCATION

Rochester Institute of Technology

Rochester, NY

M.S. and B.S. in Electrical Engineering, August 2013

Thesis

Stability Analysis of Switched DC-DC Boost Converters for Integrated Circuits

- Investigated small-signal modeling and stability requirements for boost converters, as well as a variety of OTA-based controller topologies, in order to aid in the measurement of boost converter stability on multiple ASICs. Also investigated the use of optimization algorithms as a way to improve controller design.
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PATENTS AND PUBLICATIONS

- US 9,780,736 - Temperature compensated offset cancellation for high-speed amplifiers - Grant Oct. 3, 2017
 - Authors: Kevin Fronczak, Murat Ozbas, Yongang Chen
- US 9,817,428 - Current-mode Bandgap Reference - Grant Nov. 14, 2017
 - Authors: Kevin Fronczak, Eric Bohannon
- US 10,394,386 - Interference Detection - Grant Aug. 27, 2019
 - Authors: Kevin Fronczak, Eric Bohannon
- US 10,530,296 - Oscillator Temperature Coefficient Adjustment - Grant Jan. 7, 2020
 - Authors: Andrew Jabrucki, Eric Bohannon, Kevin Fronczak
- US 15/685,937 - Mixer Circuit - Pending Aug. 24, 2017
 - Authors: Kevin Fronczak, Eric Bohannon
- US 16/378,853 - Adaptive Bias Circuit for Power Event Detection Comparator - Pending Apr. 20, 2018
 - Authors: Kevin Fronczak, Mark Pude