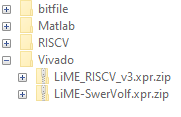
**LiME (Logic-in-Memory Emulator) with RISCV**

**Files structure:**  


* Vivado – HDL projects folder
  + Lime\_RISCV\_v3 – main project
  + LiME-SwerVolf – project for generating RISCV core
* RISCV – software for RISCV MCU
* Matlab – MATLAB GUI
* Bitfile – compiled bitfile

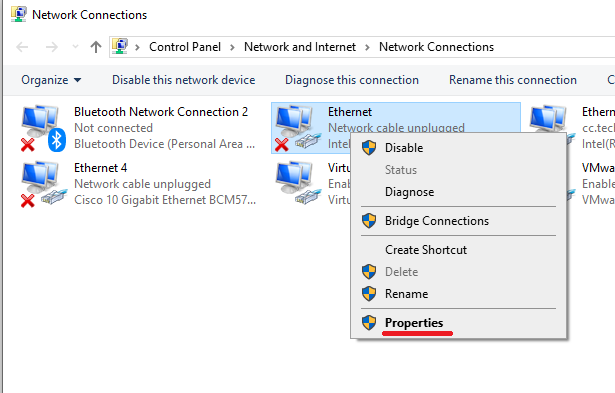
**Running the system:**  
1) Connect JTAG (micro USB) cable between PC and ZC706 board

2) Connect UART (nimi USB) cable between PC and ZC706 board

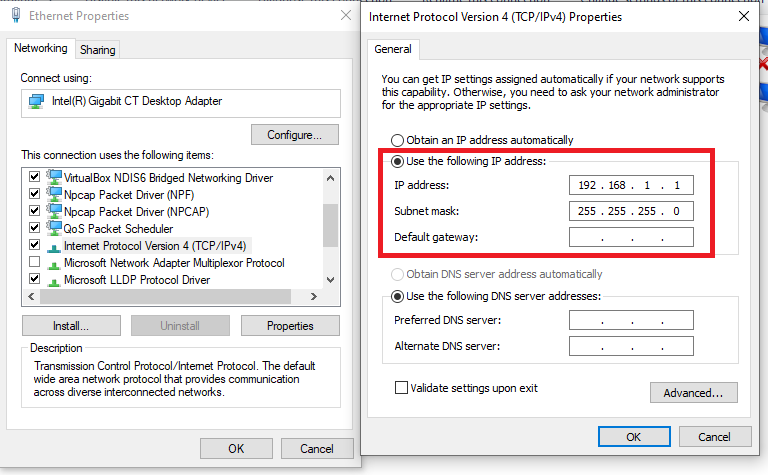
3) Connect Ethernet cable between PC and ZC706 board

4) Define static IP address on PC Ethernet port connected to ZC706:

* Go to Control Panel -> Network and Sharing Center -> Change adapter settings
* Right click on adapter -> Properties



* Click on TCP/IPv4
* Mark “Use the following IP address” and enter IP address = 192.168.1.1, Subnet Mask = 255.255.255.0

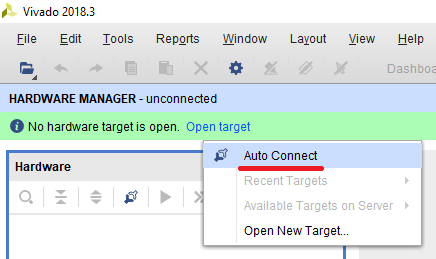


* Press OK

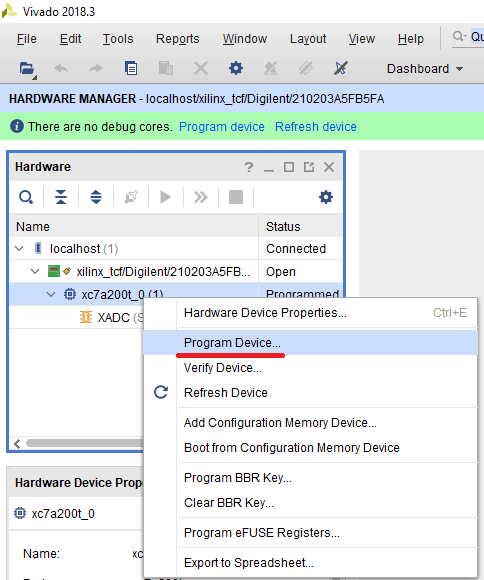
5) Power on ZC706 board

6) Program ZC706 with bitfile:

* Open Vivado Hardware Manager
* Click Open Target -> Auto Connect

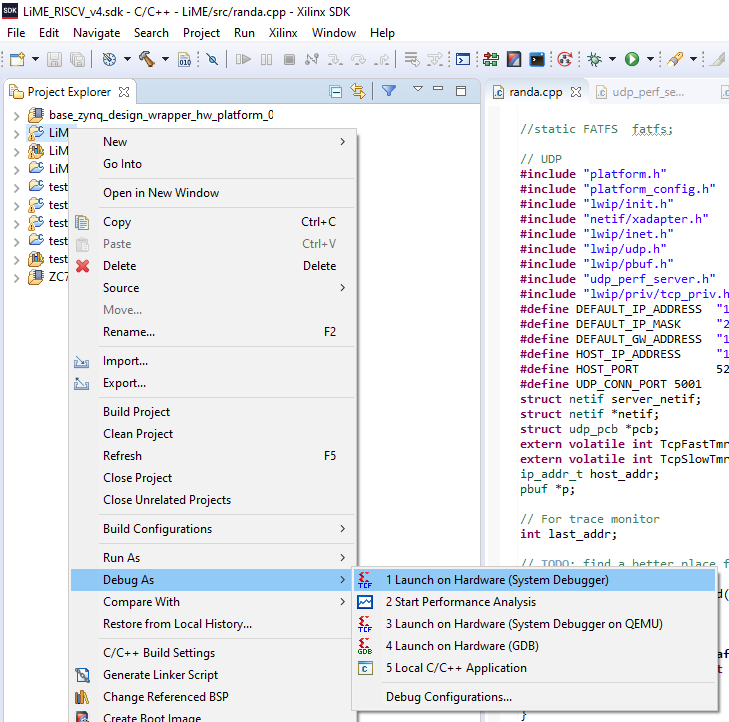


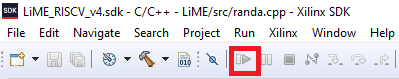
* Right click on FPGA icon -> Program Device and provide bitfile from bitfile directory



7) Run ZYNC processor:

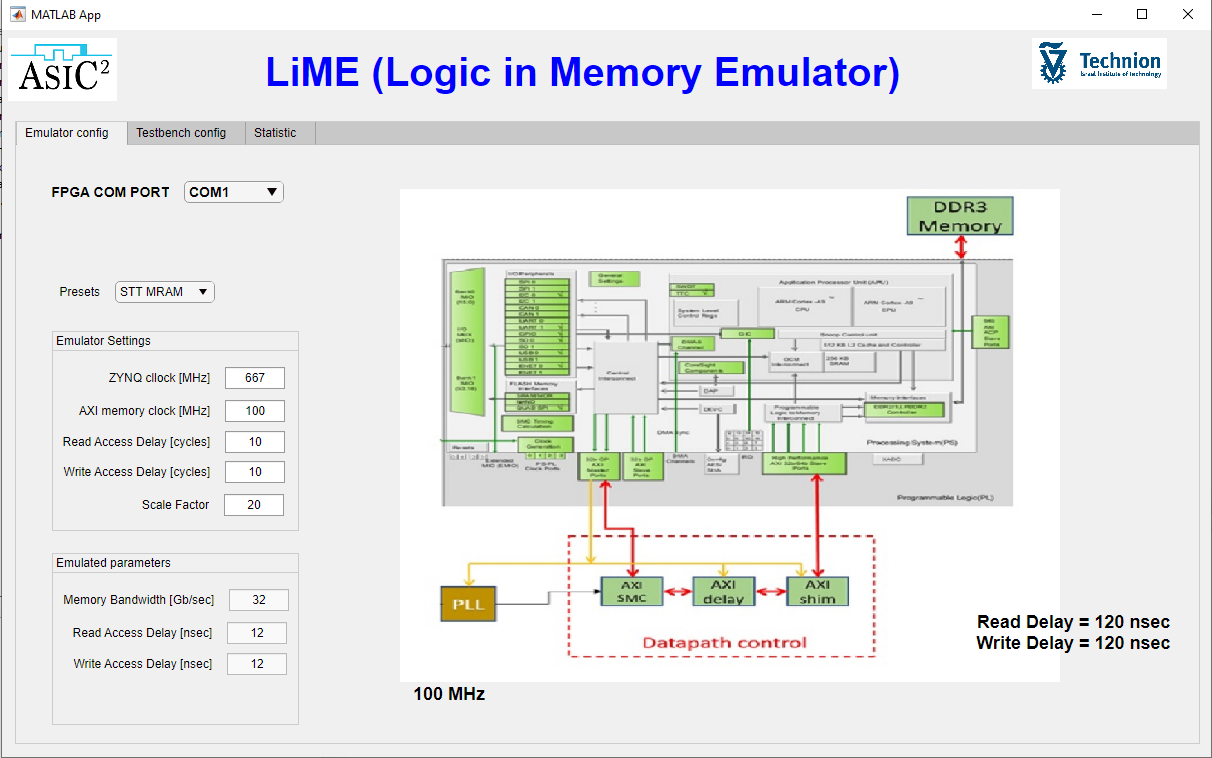
* Open LiME project in Xilinx SDK
* Right click on LiME -> Debug as -> Launch on Hardware

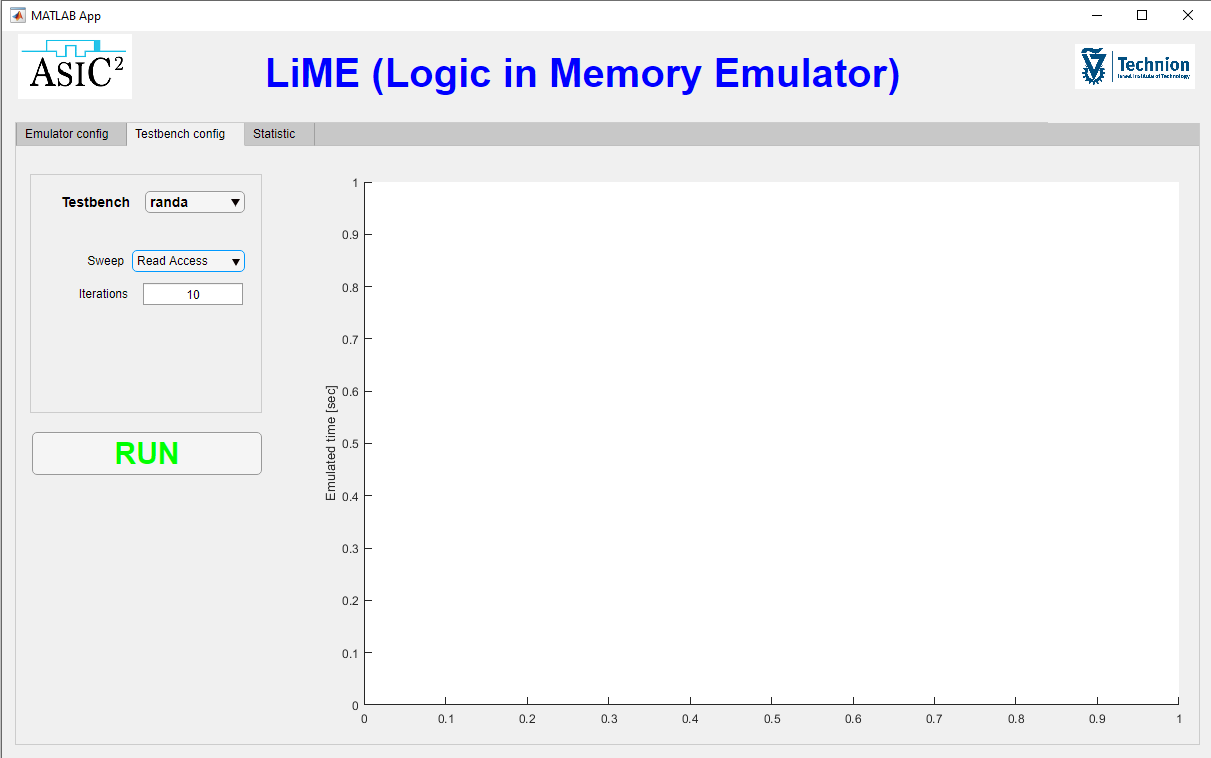


* Press Play button  
  

6) From MATLAB run LiME.mlapp GUI

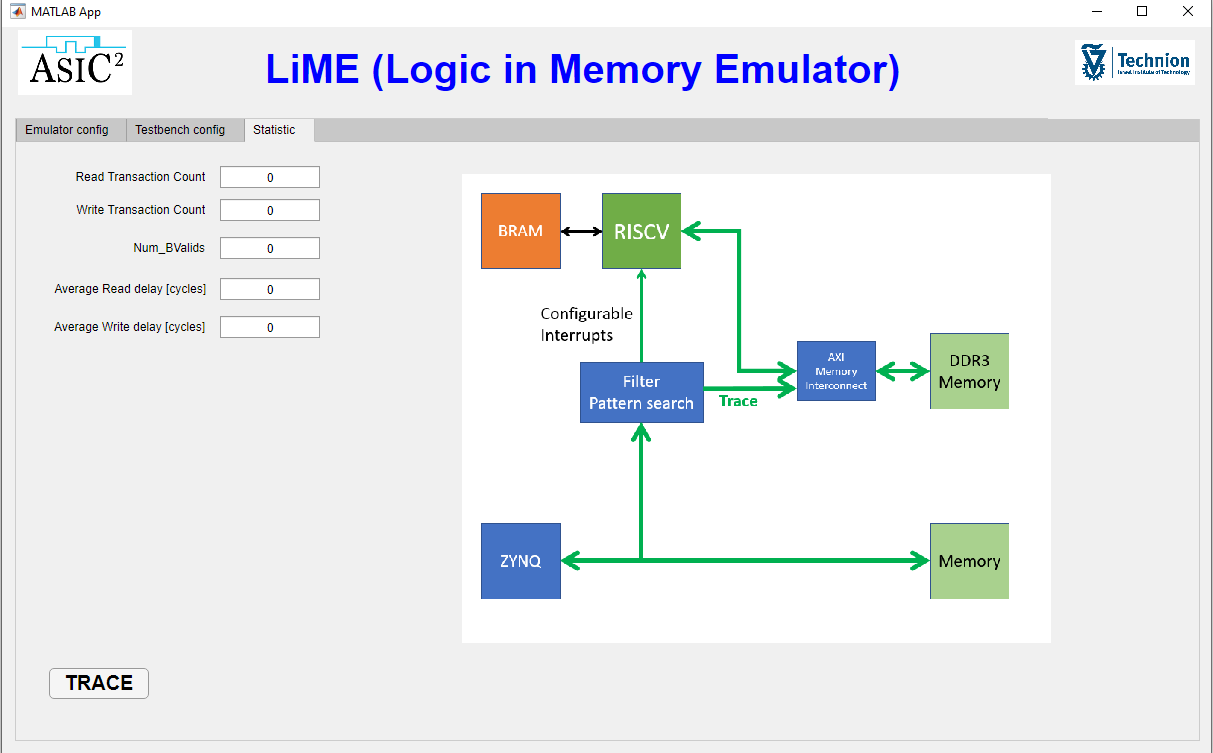
7) Select setting for emulation on “Emulator config” tab



8) Select setting for testbench on “Testbench config” tab  


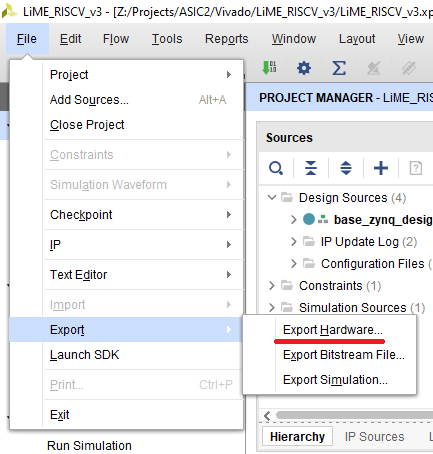
9) Press RUN button, wait for testbench to finish and observe the results

10) On Static tab you can see basic statistic of transactions on memory bus during

  
  
11) Pressing “TRACE” button will open transactions log

**Building the project**

1. Open project in Vivado by double click on \*.xpr file
2. Press “Generate Bitstream” to compile the design
3. Export generated hardware by File -> Export -> Export Hardware



1. Launch SDK by clicking File -> Launch SDK  
   