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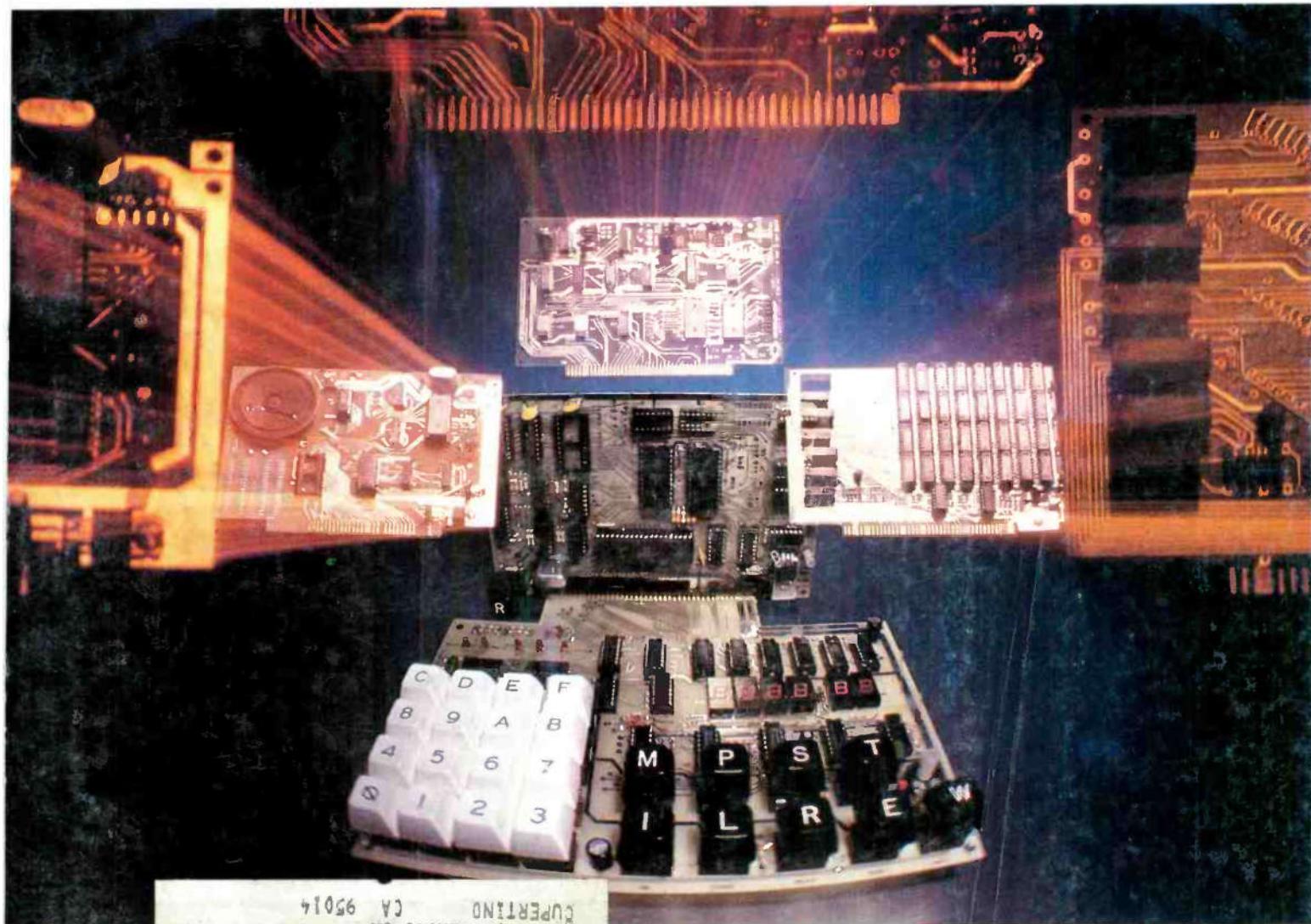
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NOVEMBER 1980/95¢

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PART II

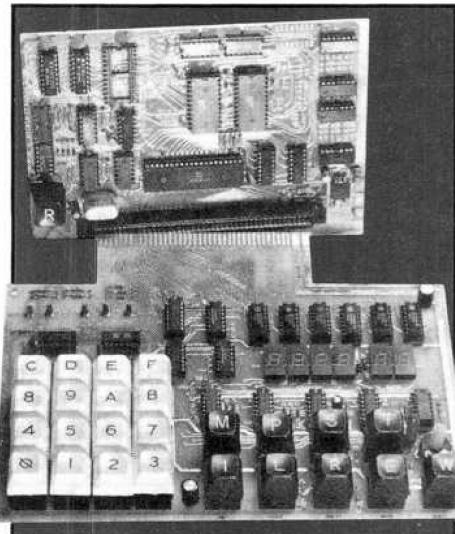
NOW YOU CAN BUILD MICROPROCESSOR PROJECTS USING AN INEXPENSIVE PRODUCT DEVELOPMENT SYSTEM!

BY GEORGE MEYERLE

IN May 1980, our first article on designing with microprocessors, "It's a Whole New Ballgame," showed how, with an understanding of just a few instructions and very modest hardware, one could build a microprocessor-based combination lock. However, to implement more generalized microprocessor product design with confidence, additional skills in programming and with hardware are required. Development of these skills will be the theme of this and future articles.

This article describes the use of input and output ports and how the microprocessor interfaces with peripheral hardware such as random access memory (RAM) and read-only memory (ROM). We will go on to the construction of an 1802 microprocessor product development system. This is an inexpensive system (professional models cost thousands of dollars) that allows the processor to be programmed, tested, and debugged for a particular application. The unique property of this system is that it is contained on two separable circuit boards: the product board and the programming board. The former becomes part of the finished project—whatever that may be; the latter is used to program other product boards.

The product or application board we will describe includes a CPU (central processing unit), a crystal-controlled system clock, 1024 bytes of RAM, 2048 bytes of ROM, one 8-bit input port, one 8-bit output port, address latches and decoding, buffered CPU flag inputs, Q output, INTERRUPT/DMA (direct memory access) request input, a POWER ON CLEAR circuit, and battery backup.



The product board is shown at top, and the programming board below.

The board uses bus connectors to plug in the programming board as well as additional product expansion cards or boards such as additional I/O, memory, A/D, graphics keyboard, cassette I/O, etc. The programming board that we will describe includes a hex keyboard to input programs, six 7-segment displays that show the status of the address and data busses, a variable-speed single-step system used to step through the program, LEDs on the MODE and STATE CODE lines of the CPU to indicate what the processor is doing, and a series of switches to completely control the action of the CPU. Functions include RESET, RUN/EXECUTE, WAIT, LOAD, INPUT and MEMORY PROTECT. (This programming card is not necessary if you already own an Elf

II; the product board plugs into an Elf II and can be programmed directly.)

Product Board Operation. The central component of the product board is the microprocessor (CPU), which controls the activities of all the peripherals. For the time being, we will not be concerned with what happens inside the CPU, only with external effects and signals. The following is a description of events and signals present at the CPU during various operations. (See Fig. 1.)

Clock. The clock signal required by the processor is generated by an external oscillator. It is used by the CPU to produce internal and external timing signals needed to control the peripherals as well as to transfer signals and data internally between parts of the CPU.

CPU Mode Control. Two processor mode-control pins completely control the CPU action. They are labelled WAIT and CLEAR. The line (vinculum) over the name indicates that a low-logic level (0 volts) at that point will cause the stated effect. To change the CPU mode, we simply have to present the CLEAR and WAIT lines with the logic levels shown in Fig. 2. When we want to put the processor in the RESET mode (CLEAR low, WAIT high) certain internal registers are set to predictable states. It will suffice for the moment to realize that the program counter is set to 0. This insures that when the mode is changed from RESET to RUN or LOAD, the first address issued by the CPU will be 0000. When the CPU is put into the LOAD mode (must be preceded by RESET), it is possible to load a program into memory via the direct-memory access line of the CPU. The

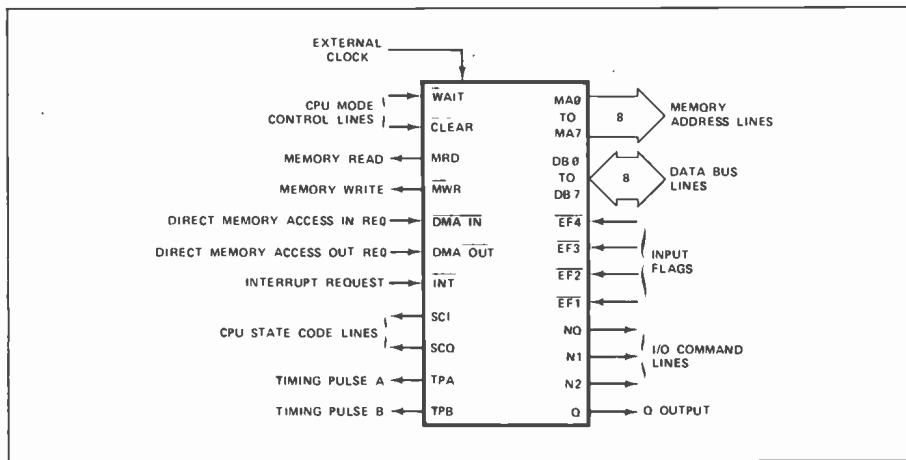


Fig. 1. Events and signals present at the CPU during various functions.

program is loaded directly into memory from the hex keypad during this mode. When the CPU is in the WAIT or PAUSE mode, the internal timing generator does not function. The clock continues to run but it is ignored. Note that the data, address, and other control lines may not have valid data or status in the WAIT mode.

The RUN mode (both CLEAR and WAIT high) may be entered from a PAUSE or RESET mode. Remember that the first machine cycle following a reset to RUN is followed by a memory fetch at address 0000. This is extremely important and simplifies the hardware interface.

State Code Lines. When in RUN, the CPU can perform only one of four types of operations. They are: INSTRUCTION FETCH, also called S0 (an abbreviation for "state"), EXECUTE, S1, a DIRECT MEMORY ACCESS, S2 or INTERRUPT, S3. Ignoring DMA and interrupt for the moment, we can say that the CPU is simply either fetching instructions or executing them. A FETCH requires one machine cycle (each machine cycle is made up of eight clock pulses). EXECUTE requires one or two machine cycles, two required only during long-branch operations.

The State-Code lines labelled SC1 and SC0 are used to tell the peripherals which type of operation is being performed by the processor. (See Fig. 3.) Note that during FETCH, both SC1 and SC0 are low; during EXECUTE, SC1 is low and SC0 is high.

Timing Pulses. (In addition to the state code lines, there are TIMING PULSE A and B (TPA, TPB). These signal the peripherals when the address, data and I/O COMMAND lines are valid and other internal operations are completed.

MEMORY READ and MEMORY WRITE LINES. These, designated MRD and MWR, are both active with logic low. MRD is present when the processor wants data from the memory. MRD must occur during a FETCH when the processor is reading memory for its next instruction. It must also occur during an OUTPUT exec-

CLEAR	WAIT	MODE
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

Fig. 2. Logic needed to change CPU Mode.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

Fig. 3. State code lines define operation

ution when the data is being transferred from the memory to an output port, as well as during BRANCH, and other memory read operations. MWR is present only when the processor is writing data into memory. Data may originate in the CPU or from an input port.

Input Flags. The input flag lines, EF1, EF2, EF3, EF4 are tested by the microprocessor and often used as single-signal input ports. The flag lines are tested during an EXECUTE. Remember that these lines are *active low*.

Q-Line. The Q-line output can be set high or low by a program instruction. The status of the Q-line can be tested by conditional BRANCH instructions. Q is a single-signal output port and can control relays or other devices.

MEMORY ADDRESS Lines. These eight lines are multiplexed. The high-order eight bits of the 16-bit address are present first; at the end of the TPA the low-order bits are presented. If the system memory is larger than 256 bytes, additional hardware is needed to record (latch) the high-order bits so that all 16 are presented simultaneously to the memory. The trailing edge of the TPA can be used to signal the latch when the high-order addresses are valid.

DATA BUS Lines. These eight-bit-bidirectional lines transfer data between the memory, CPU, and I/O devices.

(Continued on page 64)

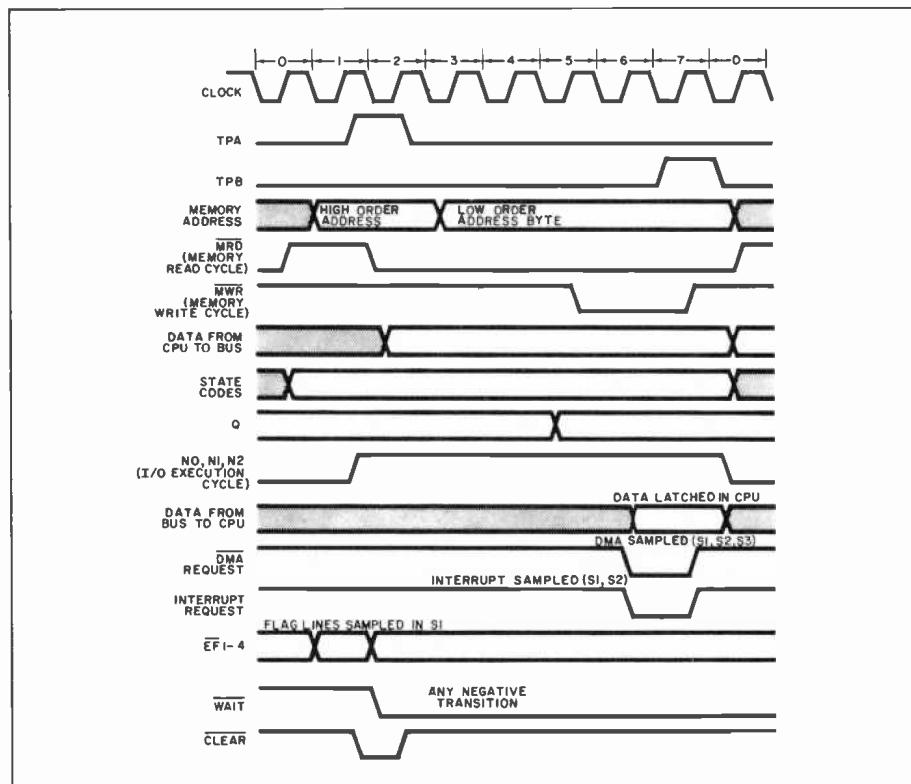


Fig. 4. The timing diagram is used to show signal relationships.
Shaded areas indicate undefined state when multiple transition may occur.

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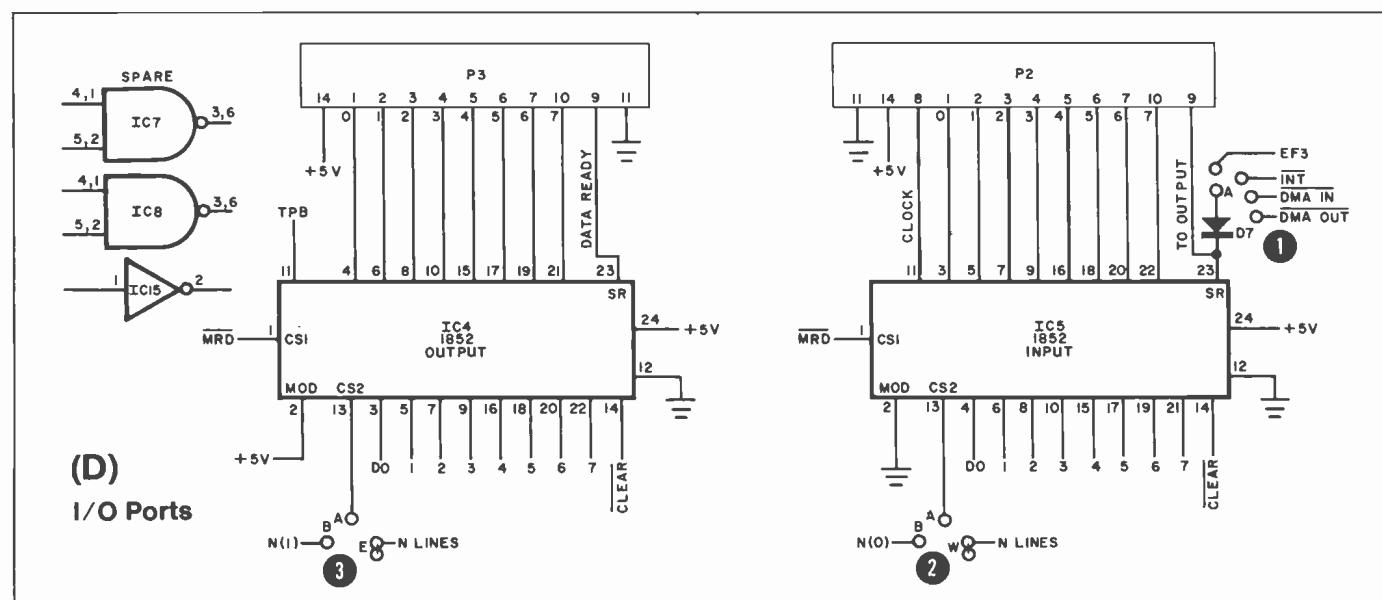
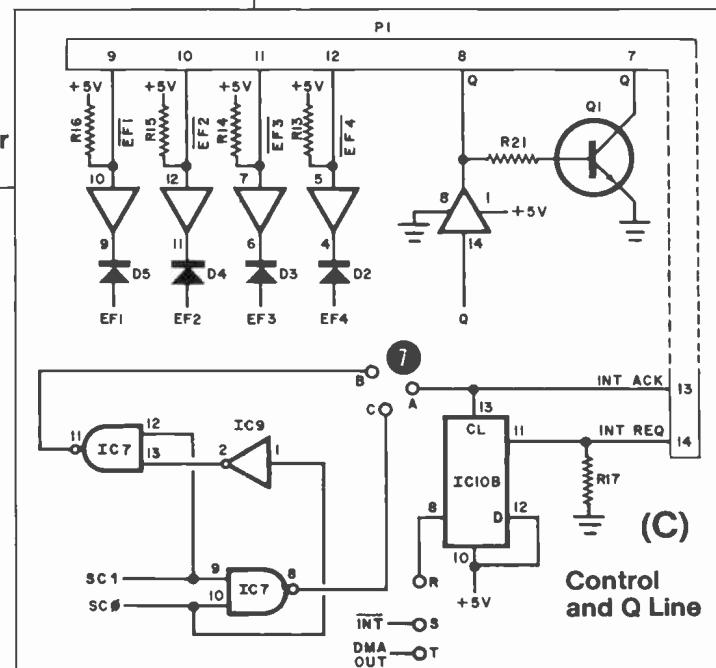
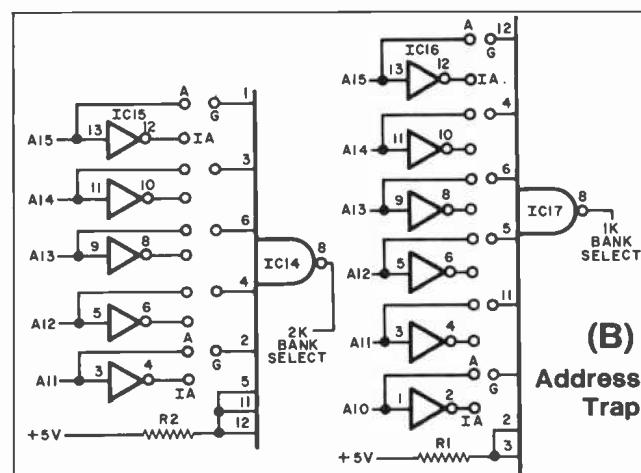
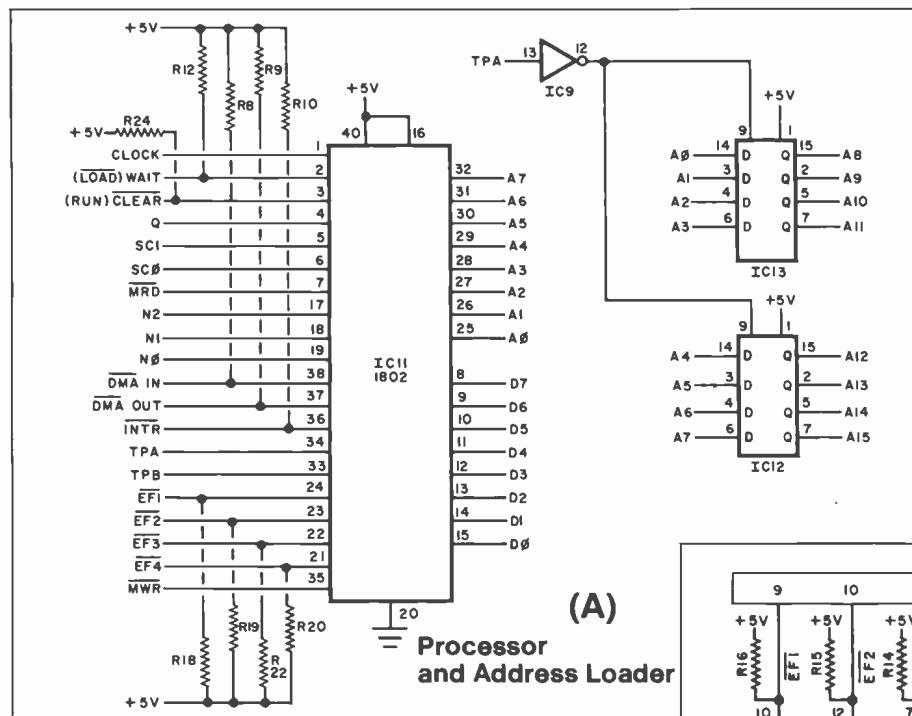


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NOVEMBER 1980

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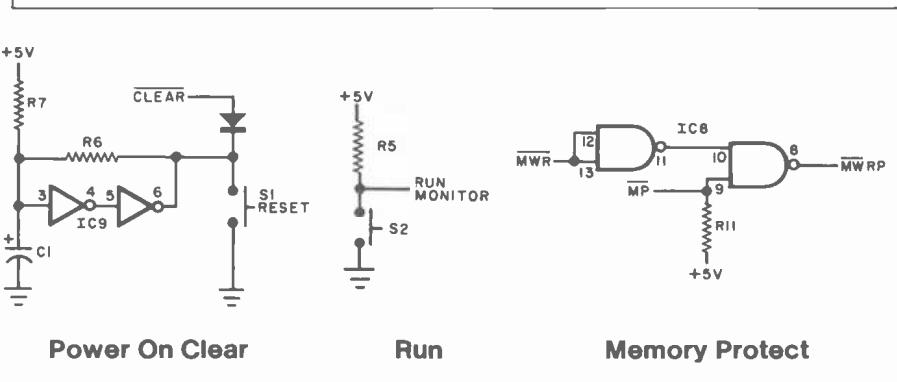
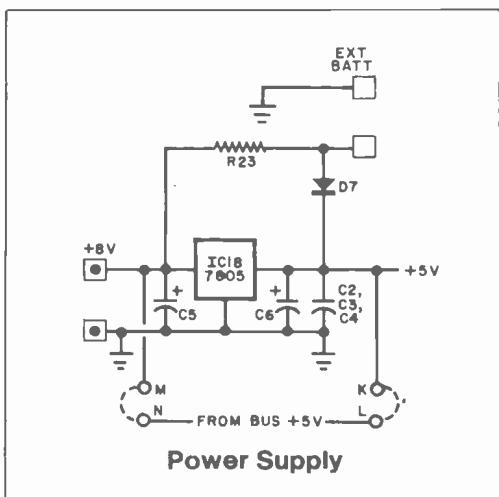
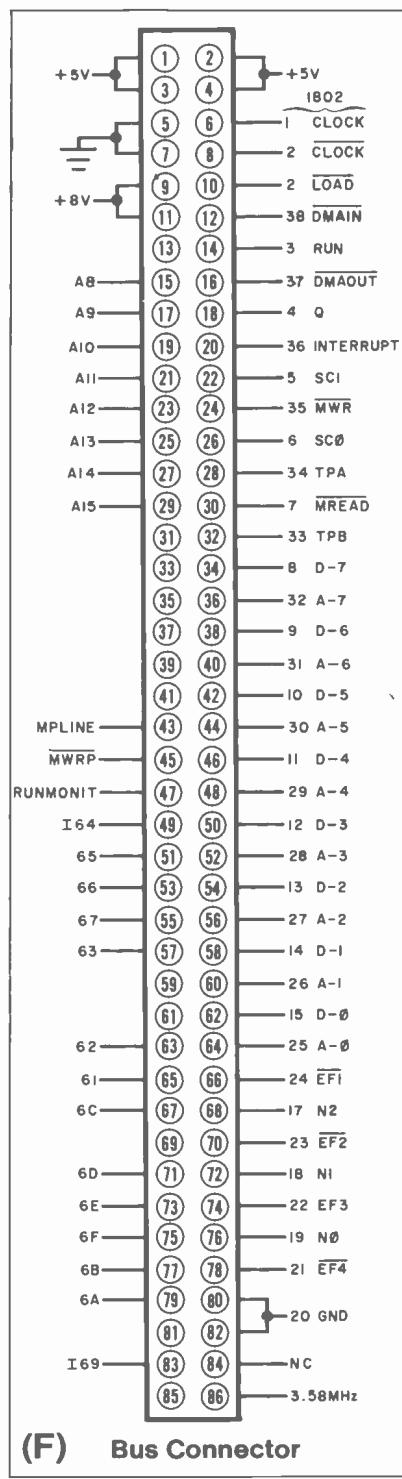
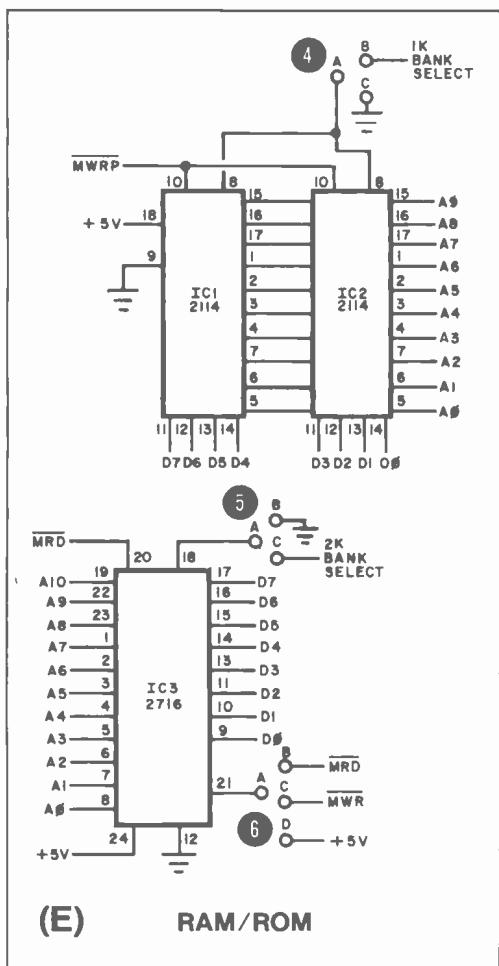


The TPB indicates to the external devices that the data bus is prepared for the transfer.

I/O COMMAND Lines. The input/output command lines, referred to as the N lines, are activated by a program instruction to signal input and output devices, either requesting data from them during an input instruction or sending data to them during an output instruction. The three lines can be decoded into seven separate output signals so that all 14 input/output instructions can be used.

A general timing diagram is shown in Fig. 4. It is not complete, but should give an idea of when transfers occur between the CPU and peripherals. Understanding this timing will enable us to use the

Fig. 5. The various parts of the circuit on the Product Board are shown schematically above and on the opposite page. Numbers in circles indicate jumper pads.



correct hardware I/O signalling devices. Note the eight clock pulses, 0-7, and the synchronization between them and the signals on the CPU lines. STATE CODES become valid just before the leading edge of TPA and continue valid until the trailing edge of TPB. External hardware is responsible for reading CPU signals during valid periods only. Each machine cycle outputs a 16-bit address of which the high-order eight bits are valid at the trailing edge of TPA and are followed by the low-order eight bits which are valid

PARTS LIST— PRODUCT BOARD

C1—2.2- μ F, 16-V electrolytic
 C2,C3,C4—0.01- μ F, 50-V disc ceramic capacitor
 C5,C6—10- μ F, 16-V electrolytic
 D1 through D6—1N4148 switching diode
 D7—1N4001 rectifier
 IC1,IC2—2114 random-access memory
 IC3—2716 ROM
 IC4,IC5—1852 I/O port
 IC6—CD4050 hex noninverting buffer
 IC7,IC8—74LS00 quad 2-input NAND gate
 IC9,IC15,IC16—74LS04 hex inverter
 IC10—74LS74 dual D flip-flop
 IC11—1802 CPU
 IC12,IC13—74LS174 hex D flip-flop
 IC14,IC17—74LS30 eight-input NAND gate
 IC18—7805 5-volt regulator
 Q1—2N4384 transistor
 The following, unless otherwise specified, are 1/4-watt, 10% tolerance, fixed carbon-composition resistors.
 R1,R2,R5,R11,R17—4.7k Ω
 R3,R4—1k Ω
 R6,R7—100 k Ω
 R8,R9,R10,R12,R13,R14,R15,R16,R18,
 R19,R20,R22,R24—22k Ω
 R21—2.2k Ω
 R23—47 Ω , 1/2 W
 XTAL1—3.579-MHz quartz crystal
 Misc.—Suitably etched and drilled, double-sided printed circuit board with plated-through holes and gold-plated edge-connector contacts; one normally open, momentary-contact pushbutton switch; IC sockets (one 40-pin, three 24-pin, two 18-pin, ten 14-pin) or Molex Solder-cons; three 14-pin DIP headers; heat sink for IC18 measuring 1" X 1/2" X 1/8" or similar; hookup wire; solder; etc.

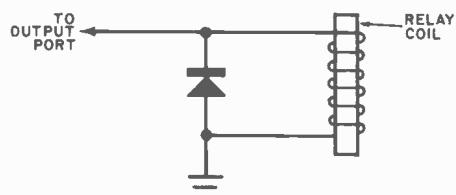


Fig. 6. How to determine load resistances on output ports. In circuit above, minimum relay coil resistance is 2.1 kΩ. The relay is active when the output is high. In the lower circuit, minimum relay resistance is 820Ω. The relay is active when the output is low.

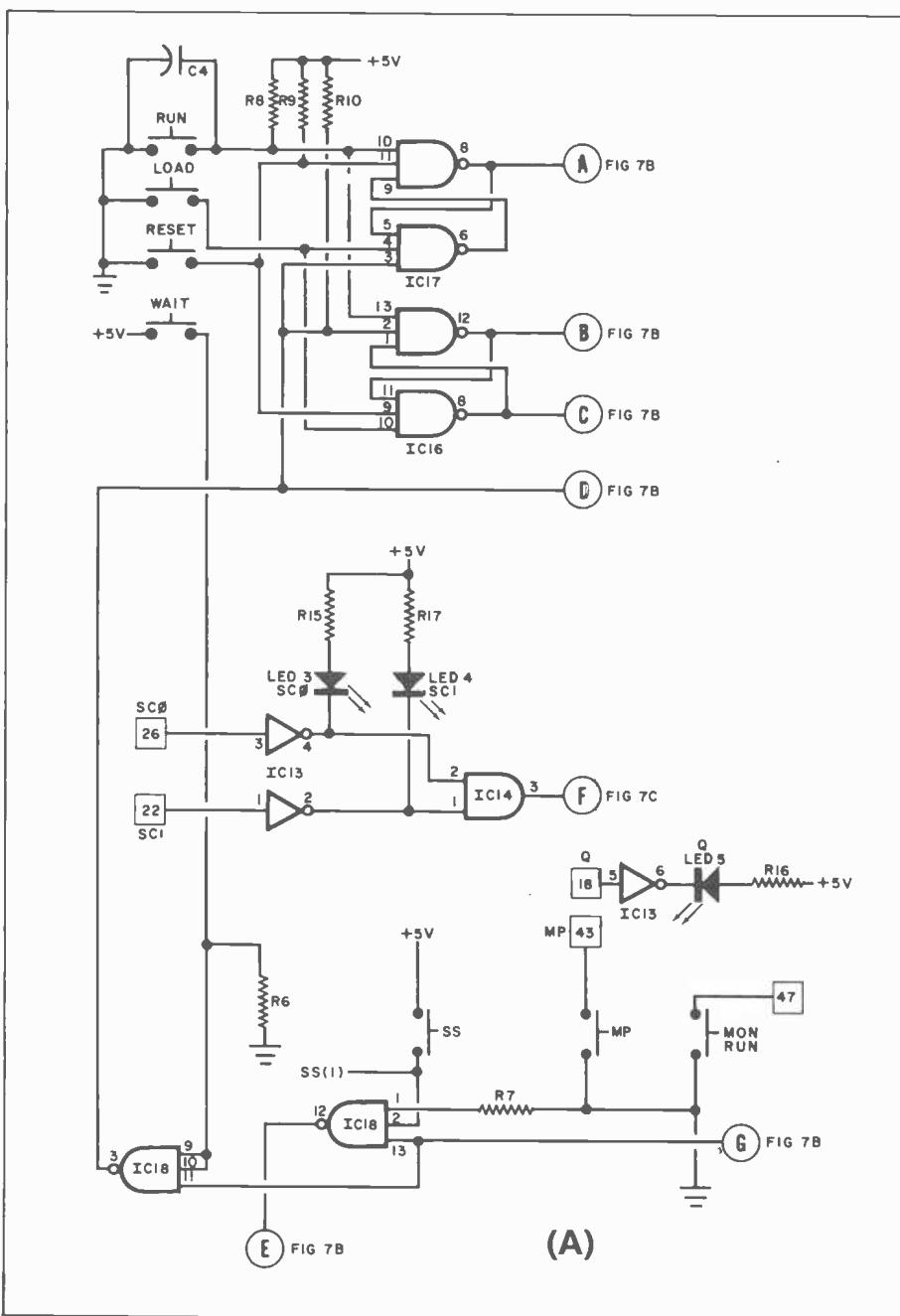
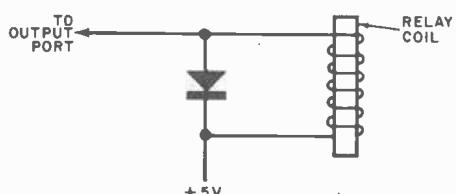


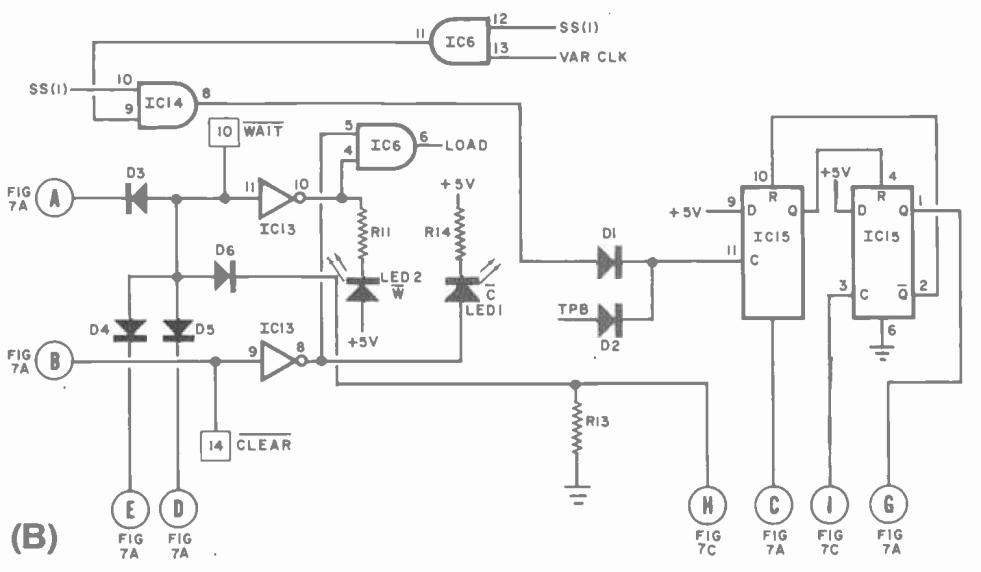
Fig. 7. Programming board circuits (A through F) are shown here and opposite

through the trailing edge of TPA. When the CPU reads from the data bus, data is latched into the CPU during TPA. I/O COMMAND lines N0, N1, and N2 are valid from the beginning of TPA to the end of TPA. The CPU tests the flag lines during an S1 cycle; the CPU responds to control signals WAIT and CLEAR during TPA, and samples DMA and INTERRUPT during TPA. Some conditions are valid only during certain types of machine cycles. For example, DMA is sampled only during machine cycles S1, S2, or S3.

Interfacing Memory. Having studied the signals present at the CPU, let's look at the schematic of the product board shown as Figs 5A through 5G. Data, in this case the high-order address bits, are latched into the Q outputs of the flip-flop during a low-to-high transition on the clock input. This low-to-high signal is produced through inversion of TPA

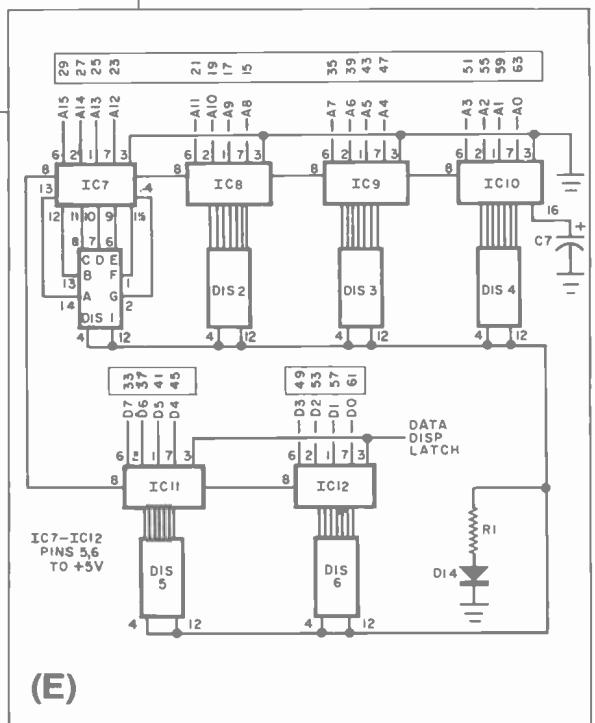
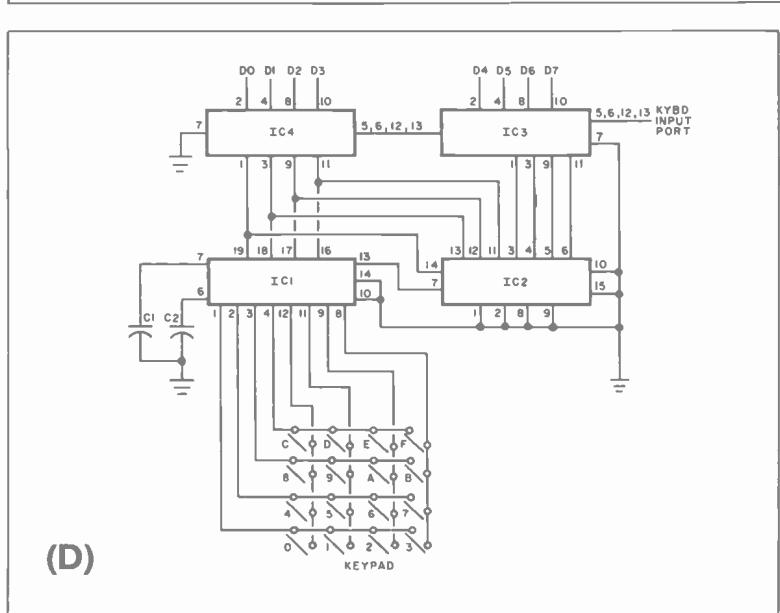
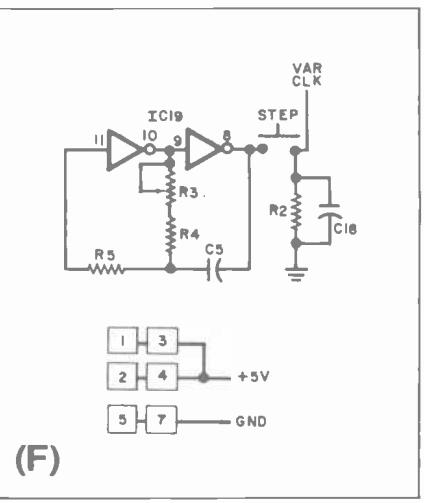
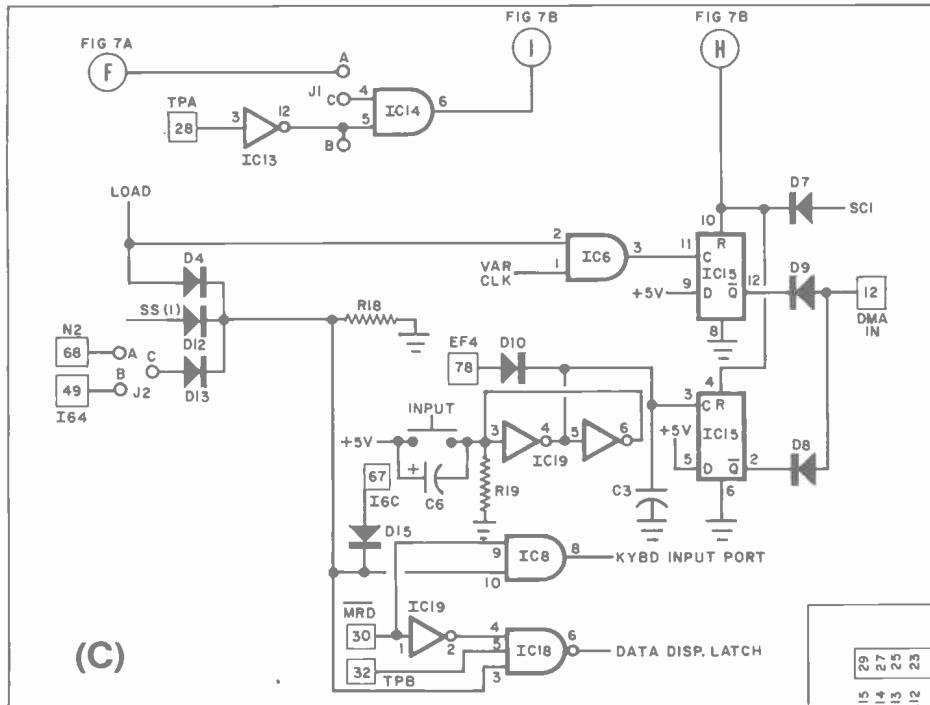
PARTS LIST— PROGRAMMING BOARD

C1,C5—1-μF, 16-V electrolytic
C2,C3—0.15-μF Mylar capacitor
C4—2.2-μF, 16-V electrolytic
C6,C7—22-μF, 16-V electrolytic
C8—0.1-μF disc ceramic capacitor
D1 through D13,D15—1N4148 switching diode
D14—1N4001 rectifier
DIS1 through DIS6—Common-cathode, seven-segment LED display
IC1—74C923 CMOS 20-key encoder
IC2—74C173 CMOS TRI-STATE quad D flip-flop
IC3,IC4—CD4016 quad bilateral switch
IC5,IC15—CD4013 dual D flip-flop
IC6,IC14—74LS08 quad 2-input AND gate
IC7 through IC12—MD 4368 hexadecimal-to-seven-segment decoder
IC13,IC19—74LS04 hex inverter
IC16,IC17,IC18—74LS10 triple 3-input NAND gate
LED1 through LED5—Red light-emitting diode (HP5082 or equivalent)
The following, unless otherwise specified, are 1/4-watt, 10% tolerance, fixed carbon composition resistors.
R1—15 Ω, 1/2 W
R2,R6,R7 through R10,R18,R19—4.7kΩ
R3—1-MΩ, linear-taper trimmer potentiometer
R4—22kΩ
R5—1 MΩ
R11,R14 through R17—470 Ω
R12—200 Ω
R13—47kΩ
Misc.—Suitably etched and drilled, double-sided printed circuit board with plated-through holes and gold-plated edge-connector contacts; 86-contact edge connector with gold-plated contacts; 22 normally open, momentary-contact pushbutton switches (this includes those comprising the hexadecimal keypad); two spdt toggle switches; IC sockets (seven 16-pin, eleven 14-pin) or Molex Soldercons; suitable hardware; hookup wire; solder; etc.



by IC9. The high-order address lines A8 to A15 are therefore present at the Q outputs of IC12 and IC13. Now, with the full 16-bit address present on the memory address bus, we can look at how the RAM IC1 and IC2 and ROM IC3 are actually addressed. RAM IC1 and IC2 contain 1,024 different memory cells or addresses; while ROM IC3 contains 2,048 different cells. The CPU is capable of addressing 65,536 different cells or addresses. To uniquely position our blocks of memory in the 65,536 address field, we must decode the upper address lines. If we want to address a RAM (IC1 or IC2 for example), we need 10 address lines, A0 through A9 ($2^{10} = 1024$). Note that on the 2114s, pin 8 is a chip-select line, active when low. The pin, when active, connects the memory cells to the data bus.

The 1,024 block could be addressed in any of 64 different blocks in the 65,536



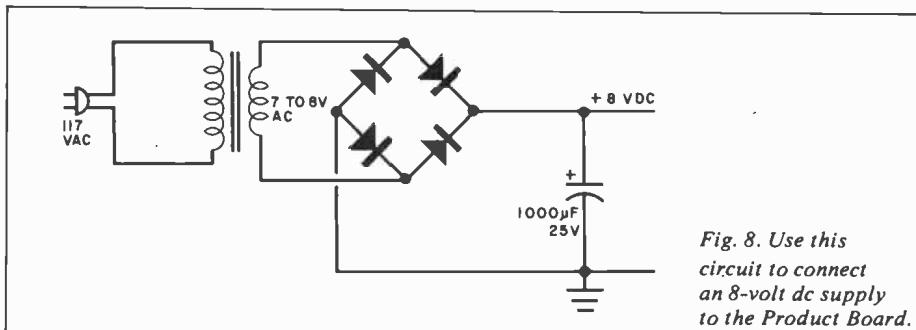


Fig. 8. Use this circuit to connect an 8-volt dc supply to the Product Board.

address field. Address lines A10 through A15 are decoded to select a specific field. If all the inputs to eight-input NAND gate IC17 are high, the output on pin 8 will be low and the RAM memory will be selected. The six address lines can be connected to the inputs of the NAND gate either directly or through hex inverter IC16. The use of inverters at selected address lines allows 64 (2^6) different possible locations for the block of memory.

To determine which address lines require an inverter, write the binary equivalent of the first address in the block of memory. Label the high-order six digits A15 through A10. An inverter must be used at all locations with a 0 binary digit. To locate the memory block at F000 (hex), we would use an inverter on address 11 and connect A12 through A15 directly to the NAND gate. If only one memory block is used and it is to be located at 0000, the chip-select CS line can be grounded and IC's 14, 15, 16, and 17 can be removed.

The same principle is used in the 2K bank-select, using IC14 and IC15 to locate the position in the memory field for IC3.

To finish our discussion on the memory, let's look at the MEMORY READ and MEMORY WRITE lines. IC1 and IC2 deposit their data on the bus whenever the CS line is low so there is no need to have the CPU READ signal connected. The MWR (P) is connected to pin 10. When the CHIP SELECT and MWR lines are low, the information on the data bus is copied into the memory cell address. Data flows from IC3 to the data bus only when both the CS and MRD lines are low. Although the position of IC3 is principally intended to be filled by a 2716 EPROM (which requires that pin 21 be tied high), a 2K RAM can be used instead by connecting its pin 21 to MWR. If you plan to use a 2K RAM at IC3, check the specs carefully for signal requirements. Finally the MEMORY WRITE line, pin 10 (IC1 and IC2), is labelled MWR (P). The P means that the memory can be protected against accidental written data by grounding pin 9 of IC8, which prevents MWR from reaching the memory. This line, MP, is also connected to pin 43 on the 86-pin bus.

into the port when CS₁ is low during a MEMORY READ and CS₂ is high during an output instruction, and when TPB is high. Data is immediately transferred to the output lines and is available at plug P3. A SERVICE REQUEST pulse is generated by the port after MRD line goes high. This pulse can signal the receiving device that new data is available.

The output lines can be connected to low-current relays or other digital devices. The 1852 will deliver up to 2.3 mA when the output is high or will sink up to 6 mA when the output is low. See Fig. 6 to determine the maximum and minimum resistances that may appear as loads on this port. Input and output commands can be changed by connecting pin 13 to a decoded N line (decoder must be on an expansion board). The output instruction for this board is 61 and the input is 6B. A final detail regarding the I/O ports is pin 14 CLEAR. A low on this line resets the port's registers and the SERVICE REQUEST output.

INTERRUPT/DMA Interface. As shown in the CPU timing diagram, DMA and INTERRUPT lines are only sampled for a short interval by the CPU. Therefore we must hold the request low until the CPU acknowledges that it has been received. This is done by flip-flop IC10B. A negative-to-positive pulse at pin 11 (clock) sets pin 8 low. Pin 8 can be connected to either the INT or DMA OUT line on the CPU. If an interrupt is chosen, pin 8 of IC7 will go low because the STATE CODE lines SC0 and SC1 will both be high. (See Fig. 4.) This will reset IC10B and signal the device requesting the interrupt that the CPU has responded. Jumper 7, A to C, must be connected. If IC10B pin 8 is connected to DMA OUT, IC7 pin 11 will go low when the STATE CODE lines indicate that DMA is in progress, again resetting the flip-flop and acknowledging the DMA request via jumper 7, A to B. These examples illustrate the importance of understanding timing diagrams.

Interfacing I/O Ports. Integrated circuit IC5 has pin 1 tied low and acts as an input port. It has eight input lines that can be connected to external equipment via plug P2. These inputs, typically, would be connected to the status switches on a robot, alarm system, etc. When the data is valid and to be read, IC5's CLOCK line (pin 11) is externally made high. This latches the data into the input side of the port. A high-to-low transition of the CLOCK line causes the input data to be latched into the input port's output register and simultaneously sets the SERVICE REQUEST line, pin 23, low. At this point, the output drivers of IC5 are disabled and the data is not yet on the bus. The SERVICE REQUEST line of IC5, pin 23, can be connected to the CPU flag EF3, INTERRUPT, or DMA. If you use EF3, your program must interrogate EF3 and issue an instruction that results in the transfer of data from the port to a memory location designated by the program, as well as to the D register in the CPU. Actual data transfer takes place when IC5's CS₁ and CS₂ both go high. This enables the output drivers and puts the data on the bus. At the same time, SERVICE REQUEST is reset. Voltage at the inputs must be in the range of -0.5 to 5.5 volts dc. This is true of all the gates and inputs that we will discuss.

Output port IC4 is identical to input port IC5. Tying pin 2 high converts the chip to its output mode. Data is latched

To Output Port				
0000	OUT 1	61	Output next byte	
0002		FF	All 1's	
0003	IDL	00	Idle	

Fig. 9. Use the program at left to output a byte and the one below to input a byte.

To Input Port				
0000	LD1	F8 00 B1	Load 00 in high order Reg. 1	
0003	LD1	F8 10 A1	Load 10 in low order Reg. 1	
0004	Set X	E1	Set X to	
0005	IN3	6B	Input data	
0006	Out 4	64	Display it on program board	
0007	IDL	00	Idle	

POWER ON/CLEAR Circuit. This automatically resets the CPU in the event of a power failure. Its usefulness depends on the retention of data in memory despite power loss, which means that the memory or program memory must be in ROM. When the CLEAR line on the CPU is held low with the WAIT line high, the CPU is reset. This condition is met on a power up because the CLEAR line is held low by IC9 until C1 charges. This delay lets the onboard crystal oscillator stabilize before program execution begins.

The crystal clock generator (2 gates of IC9) generates a 3.578-MHz square wave. The D-type flip-flop IC10A is used to divide the frequency by two. The 1802 clock input is connected to pin 5 of IC10A. A CLOCK signal is provided to drive a color video system in an expanded setup.

Buffers and Power Supply. Input and output buffers in IC6 isolate the external flags and Q lines from the CPU. Buffers are far less costly than CPUs and can serve as protection against voltage transients and short circuits that may occur in the outside world. Additionally, they are capable of sourcing and sinking larger currents than can CPU lines.

The power-supply regulator Q2 will deliver up to 500 mA dc. The programming board also gets its power from this source. The power requirement of the product board, fully loaded, is 110 mA. An optional NiCd battery pack can be added (four 1.5-volt cells) to power the product board for about 2 hours in the event of a power failure.

Programming Board. The purpose of the programming board is to load a program into the memory on the product board and then test the program and hardware. It can be disconnected from the product board when the programming and testing are complete. The programming board (Figs. 7A through 7F) is connected (via the 86 pin bus) to the CLEAR and WAIT lines on the CPU; therefore it can place the CPU in any of its four modes, displaying the mode selected on LED1 and LED2. Two LEDs (LED3 and LED4) on the STATE CODE lines identify the type of CPU machine cycle in progress.

The hex value of the entire 16-bit address line is displayed on 7-segment displays DIS1 through DIS4. Two 7-segment displays (DIS5 and DIS6) perform the same function for the data bus. Data bus displays are also configured as an output port responding to a 64-output instruction. A hex keyboard is connected to the data bus via two 4116 gates. IC1 converts the hex value of the key press to its 4-bit binary equivalent. When a second key is pressed, the value

(Continued on page 74)

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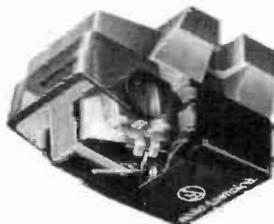
There are perhaps a dozen reasons why the new AT155LC does so well tracking even the most explosive new digital records. An advanced new Line Contact stylus, our exclusive Vector-Aligned™ magnetic system, and new high-efficiency coil and core designs to mention just a few.

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of the first key is stored in *IC2*. This puts a full 8-bit number on the input side of the 4016 gates *IC3* and *IC4*. If the CPU is in the LOAD mode, pressing the INPUT button will load the binary value of the two keys previously pressed into the program memory. This is accomplished by pin 2 of *IC5* pulling the DMA IN line low, causing the contents of the data bus to be directly loaded into the memory location specified by the register 0 in the CPU. The CPU will acknowledge the DMA by issuing a high on SCI. This is used to reset flip-flop *IC5*. The INPUT switch is also connected to the EF4 line.

The hex keyboard also can be used to input data during a program. It is configured to respond to a 6C instruction. The RUN, LOAD and RESET buttons are connected to three NAND gates of *IC17*. These gates are flip-flops that apply the appropriate logic levels to the CLEAR and WAIT lines which control the CPU mode. The WAIT switch will cause the CPU to pause. It is arranged so that the pause will only occur between TPA and TPB to insure that valid data and addresses are displayed when the WAIT is issued. The single-step mode allows the operator to execute the program one step at a time, observing the STATE CODES, Q line, data and address lines, as well as the action taken by external relays and components, etc. Jumper *J1* can select the stopping point during the single-step mode. If *J1* is connected A to C, then the program will stop only in a FETCH cycle. If *J1* is connected B to C, the stopping point will be each machine cycle at the trailing edge of TPB. You may want to try this initially to get a better understanding of the CPU operation. However, eventually you will probably connect *J1* to HALT only in the FETCH mode.

Remember to consult the timing diagrams to interpret the contents and meaning of the ADDRESS and DATA bus signals.

Slow-Step Clock. Formed from *IC19*, the speed of the stepping or toggling clock is controlled by *R3*. Hold the STEP toggle button depressed, and adjust *R3* for the clock speed desired.

Test Procedure. To test the combination of the product and programming boards, install the six 1K bank-select jumpers (IA to G). This will locate the 1K memory at 0000 hex. Connect the input ports so that jumper 1 connects from terminal A to EF3 and jumper 2 between A and B, selecting instruction 61. Connect the output port jumper 3 A to B, the 1K memory-select jumper 4 A to B. Jumpers 5, 6 and 7 are not required at this time. Install the following jumpers on the programming board: *J1* A to C, *J2* B to C. Now connect an

8-volt dc supply between the 8-volt input and ground on the product board. Use the circuit shown in Fig. 8. Apply the power with no ICs installed. Check the output of the 7805 regulator *Q2* on the product board. The voltage should be +5 volts, ±5%. If not, correct the problem before proceeding.

Remove the power, install the ICs, and plug the programming board into the product board. If you are using an Elf II to program the product board, remove the 1802, 2102's and the 1861 video chip. (The 1861 will interfere with the I/O port allocation unless you use your giant board to reallocate I/O instructions to IC4 and IC5 on the product board.

When power is applied, the 7-segment displays should light up. With the latching switches up, press the RESET button. The RESET LED should be on, as well as SCo. PAUSE, SCI and Q LEDs should be off. Press the LOAD button. The RESET LED should go off. Enter a 7 on the hex keyboard, followed by a B, then depress the INPUT button. The display should read 0000 7B, indicating that a 7B is located at memory location 0000. Now input 7A, followed by a 3A and 00. The display should read 0003 00. This program first turns the Q light on, then turns it off and BRANCHES back to the beginning, running in a loop.

Now press RESET, followed by the EXECUTE RUN button. Both the RESET and PAUSE lights should go on, indicating that both the WAIT and CLEAR lines on the CPU are high or that the CPU is in the RUN mode. The Q light should glow. It is being turned on and off by the program. Now press the WAIT button. The PAUSE light should stay on, the RESET go off. The program can now stop at any point in the loop. Remember, it stops in any machine cycle, so it may stop in a FETCH or EXECUTE.

Depress E again. The program will start up where it left off. Try it a few times, noting that the program stops only at address 0000 through 0003 and that the Q, SCo and SCI LEDs may or may not be on. Try to estimate where the CPU has stopped. Now depress the S (STEP) button. Then depress E, holding the T (TOGGLE) button down. Rotate R3 until you can follow the program.

Note that the addresses displayed are one step ahead of the action on the data bus display and the Q LED. This is because the SINGLE-STEP stops at the beginning of a FETCH, while the DATA display and the Q LED are indicating the previous machine EXECUTE cycle. Refer to Fig. 4 and follow the timing diagram through the single-step mode.

To examine memory, press RESET, LOAD and P (Memory Protect). Remember to release the SINGLE-STEP button. Now, pressing INPUT will allow you to

step through your program. Pressing and holding the TOGGLE button will allow you to review it at a rate determined by R3. The M button is not used at this time. Provisions have been made to add a system monitor which will be activated with this button. To test the I/O ports, write a small program such as those in Fig. 9 using them.

Construction. Assembly of the development system is basically straightforward, but because of the complexity of the circuitry, use of pc boards is virtually a necessity. The boards are double-sided and very difficult to make, and their purchase is recommended. Because of their size, the foil patterns are not given here. The patterns and component layout guides may be obtained by sending a self-addressed 8-inch by 10-inch envelope with two units of postage to Editorial, Dept. MP, Popular Electronics, One Park Ave., New York, NY 10016. Several of the ICs are MOS devices and require the standard handling precautions.

Once you have assembled and checked out your development system, you will be well on the way to proficiency in designing with microprocessors. The scope of projects you can design and build is limited only by your imagination and ingenuity. Considering the vast possibilities offered by microprocessors, you may want to order a supply of several of the product boards. ◇

PARTS AND KIT AVAILABILITY

The following items are available from Netronics Research and Development, Ltd., 333 Litchfield Road, New Milford, CT 06776: complete Product Board kit including all components appearing in Product Board parts list, \$59.95; complete Programming Board kit including all components appearing in Programming Board parts list, \$79.95. The following are also available individually: Product Board printed-circuit board only, \$25.00; Programming Board printed-circuit board only, \$29.00; 86-contact edge connector with gold-plated contacts only, \$5.70; 8-volt power supply including plug-in transformer/bridge rectifier/filter capacitor assembly, \$8.95. Postage, handling and insurance charges for U.S.A. orders: complete Product Board kit, \$2.00; complete Programming Board kit, \$2.00; Product Board pc board only, \$1.50; Programming Board pc board only, \$1.50; 86-contact edge connector only, \$0.50; 8-volt power supply, \$0.80. Connecticut residents, add state sales tax. Toll-free telephone number for ordering purposes: 1-800-243-7428.



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