Student ID:

1. What is the average memory access time (AMAT) for a CPU with a direct-mapped cache, having a 90% hit rate, a 2ns hit time, and a 60ns miss penalty? [2pt]

$$2ns + (1-0.9) * 60ns = 8ns$$

2. We consider a direct-mapped cache design having 16-bit address, and the layout of the 16-bit address is listed as below. What is the ratio of the total number of bits needed for this cache implementation to the number of bits used to store data? [2pt]

Tag	Index	Offset
15-10	9-4	3-0

9-4 -> 6 bits, 64 entries

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64 entries * (1 valid + 6 tag + 16 * 8 data) = 64 * 135
Data bits = 64 entries * 16 * 8 data= 64 * 128
Ratio 135/128 = 1.05
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