

Lab07 Interrupt & Timer

PIC18F4520 Datasheet

MicroChip - PIC18F4520 Datasheet
(<https://ww1.microchip.com/downloads/en/DeviceDoc/39631E.pdf>).

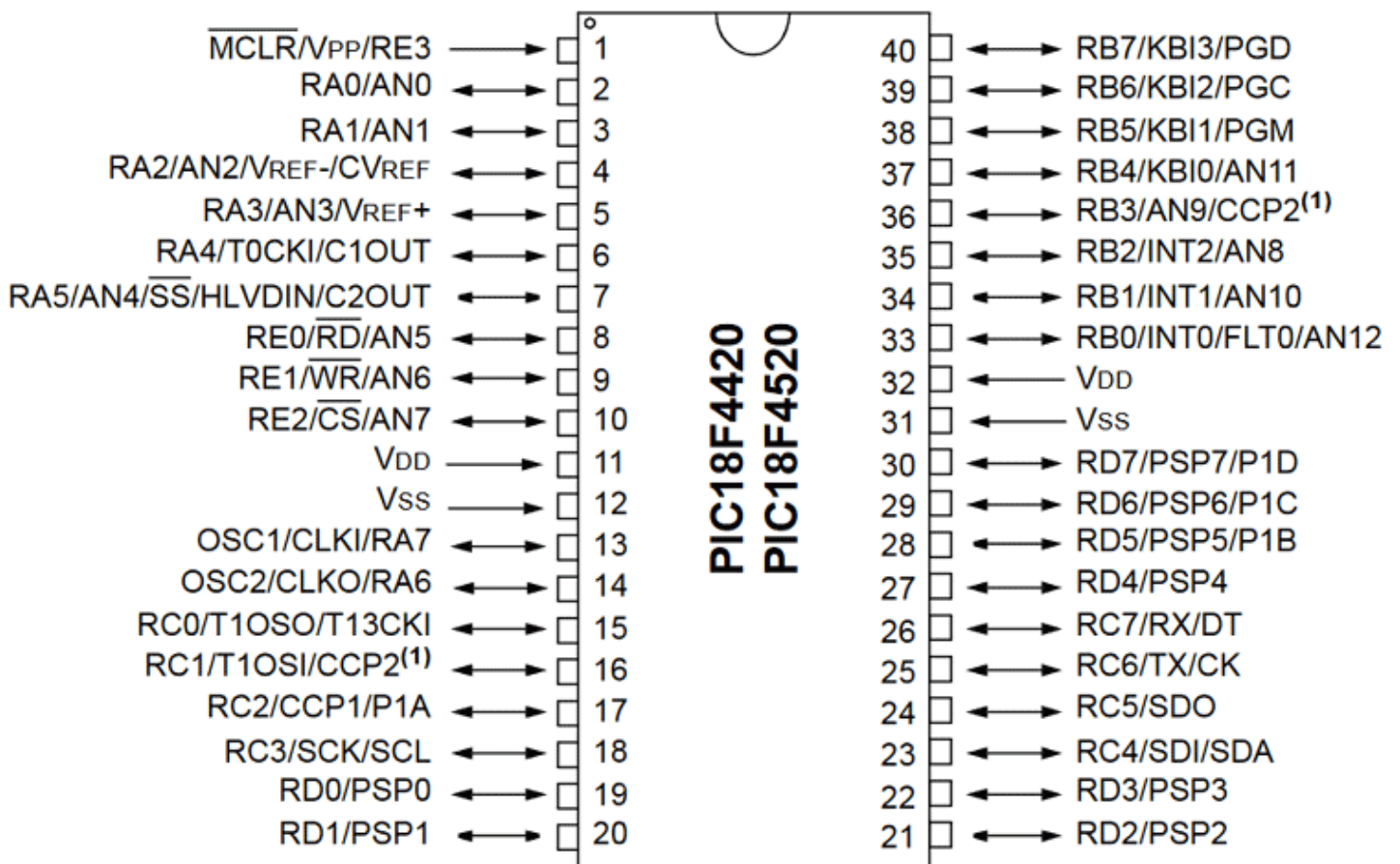
Interrupt用

| Register名稱 | 在第幾頁 | 用途 |
|------------|-------|---------------------------------|
| RCON | 第44頁 | IPEN: 設定Interrupt優先度 |
| INTCON | 第95頁 | GIE、INT0的[Flag bit, Enable Bit] |
| ADCON1 | 第226頁 | 設定數位類比 |

Timer用

| Register名稱 | 在第幾頁 | 用途 |
|------------|-------|--------------------|
| OSCCON | 第32頁 | 調整時脈 (可以玩看看) |
| T2CON | 第135頁 | 設定Timer2的啟動、預除器後除器 |
| PIR1 | 第98頁 | TMR2IF、TMR1IF等 |
| PIE1 | 第100頁 | TMR2IE、TMR1IE等 |
| IPR1 | 第102頁 | TMR2IP、TMR1IP等 |

PIC18F4520 架構圖



Interrupt 範例程式碼

```
#include "p18f4520.inc"

; CONFIG1H
CONFIG OSC = INTIO67      ; Oscillator Selection bits (Internal oscillator)
CONFIG FCMEN = OFF        ; Fail-Safe Clock Monitor Enable bit (Fail-Safe)
CONFIG IESO = OFF         ; Internal/External Oscillator Switchover bit

; CONFIG2L
CONFIG PWRT = OFF         ; Power-up Timer Enable bit (PWRT disabled)
CONFIG BOREN = SBORDIS    ; Brown-out Reset Enable bits (Brown-out Reset)
CONFIG BORV = 3           ; Brown Out Reset Voltage bits (Minimum setting)

; CONFIG2H
CONFIG WDT = OFF          ; Watchdog Timer Enable bit (WDT disabled)
CONFIG WDTPS = 32768      ; Watchdog Timer Postscale Select bits (1:32768)
```

```

; CONFIG3H
CONFIG  CCP2MX = PORTC      ; CCP2 MUX bit (CCP2 input/output is multiplexed with PORTC pins)
CONFIG  PBAEN = ON          ; PORTB A/D Enable bit (PORTB<4:0> pins are configured as analog input channels)
CONFIG  LPT1OSC = OFF       ; Low-Power Timer1 Oscillator Enable bit (Timer1 configured for low power operation)
CONFIG  MCLRE = ON          ; MCLR Pin Enable bit (MCLR pin enabled; RE3 input pin disabled)

; CONFIG4L
CONFIG  STVREN = ON         ; Stack Full/Underflow Reset Enable bit (Stack full or underflow will cause a reset)
CONFIG  LVP = OFF           ; Single-Supply ICSP Enable bit (Single-Supply ICSP mode is not available)
CONFIG  XINST = OFF         ; Extended Instruction Set Enable bit (Instruction set extension and Instruction Set Selector in the CLINT are disabled)

; CONFIG5L
CONFIG  CP0 = OFF           ; Code Protection bit (Block 0 (000800-001FFF))
CONFIG  CP1 = OFF           ; Code Protection bit (Block 1 (002000-003FFF))
CONFIG  CP2 = OFF           ; Code Protection bit (Block 2 (004000-005FFF))
CONFIG  CP3 = OFF           ; Code Protection bit (Block 3 (006000-007FFF))

; CONFIG5H
CONFIG  CPB = OFF           ; Boot Block Code Protection bit (Boot block code is protected)
CONFIG  CPD = OFF           ; Data EEPROM Code Protection bit (Data EEPROM code is protected)

; CONFIG6L
CONFIG  WRT0 = OFF          ; Write Protection bit (Block 0 (000800-001FFF))
CONFIG  WRT1 = OFF          ; Write Protection bit (Block 1 (002000-003FFF))
CONFIG  WRT2 = OFF          ; Write Protection bit (Block 2 (004000-005FFF))
CONFIG  WRT3 = OFF          ; Write Protection bit (Block 3 (006000-007FFF))

; CONFIG6H
CONFIG  WRTC = OFF          ; Configuration Register Write Protection bit (Configuration register is write-protected)
CONFIG  WRTB = OFF          ; Boot Block Write Protection bit (Boot block code is write-protected)
CONFIG  WRTD = OFF          ; Data EEPROM Write Protection bit (Data EEPROM code is write-protected)

; CONFIG7L
CONFIG  EBTR0 = OFF         ; Table Read Protection bit (Block 0 (000800-001FFF))
CONFIG  EBTR1 = OFF         ; Table Read Protection bit (Block 1 (002000-003FFF))
CONFIG  EBTR2 = OFF         ; Table Read Protection bit (Block 2 (004000-005FFF))
CONFIG  EBTR3 = OFF         ; Table Read Protection bit (Block 3 (006000-007FFF))

; CONFIG7H
CONFIG  EBTRB = OFF         ; Boot Block Table Read Protection bit (Boot block code is table read-protected)

L1 EQU 0x14
L2 EQU 0x15
org 0x00

DELAY macro num1, num2
    local LOOP1

```

```

    local LOOP2
    MOVLW num2
    MOVWF L2
    LOOP2:
        MOVLW num1
        MOVWF L1
    LOOP1:
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        DECFSZ L1, 1
        BRA LOOP1
        DECFSZ L2, 1
        BRA LOOP2
endm

```

； 程式邏輯：會一直卡在main裡面做無限迴圈，按下RB0的按鈕後會觸發interrupt，跳到ISR執行
 ； ISR裡的内容會亮起所有在RA上的燈泡，Delay約0.5秒後熄滅。

```

goto Initial                ; 避免程式一開始就會執行到ISR這一段，要跳過。
ISR:                        ; Interrupt發生時，會跳到這裡執行。
    org 0x08
    SETF LATA
    DELAY d'350' , d'180'   ; 約500_000cycles數， 在1MHz的情況下大約會Delay0.5
    CLRF LATA
    BCF INTCON, INT0IF
    RETFIE                  ; 離開ISR，回到原本程式執行的位址，同時會將GIE設為1，允

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Initial:                    ; 初始化的相關設定
    MOVLW 0x0F
    MOVWF ADCON1            ; 設定成要用數位的方式，Digital I/O

    CLRF TRISA
    CLRF LATA
    BSF TRISB, 0
    BCF RCON, IPEN
    BCF INTCON, INT0IF      ; 先將Interrupt flag bit清空
    BSF INTCON, GIE         ; 將Global interrupt enable bit打開
    BSF INTCON, INT0IE      ; 將interrupt0 enable bit 打開 (INT0與RB0 pin腳1

main:
    bra main
end

```

Timer2 範例程式碼

```
#include "p18f4520.inc"

; CONFIG1H
CONFIG OSC = INTIO67      ; Oscillator Selection bits (Internal oscillator)
CONFIG FCMEN = OFF        ; Fail-Safe Clock Monitor Enable bit (Fail-Safe)
CONFIG IESO = OFF         ; Internal/External Oscillator Switchover bit

; CONFIG2L
CONFIG PWRT = OFF         ; Power-up Timer Enable bit (PWRT disabled)
CONFIG BOREN = SBORDIS    ; Brown-out Reset Enable bits (Brown-out Reset)
CONFIG BORV = 3           ; Brown Out Reset Voltage bits (Minimum settings)

; CONFIG2H
CONFIG WDT = OFF          ; Watchdog Timer Enable bit (WDT disabled)
CONFIG WDTPS = 32768      ; Watchdog Timer Postscale Select bits (1:32768)

; CONFIG3H
CONFIG CCP2MX = PORTC     ; CCP2 MUX bit (CCP2 input/output is multiplexed)
CONFIG PBADEN = ON        ; PORTB A/D Enable bit (PORTB<4:0> pins are analog)
CONFIG LPT1OSC = OFF      ; Low-Power Timer1 Oscillator Enable bit (Timer1)
CONFIG MCLRE = ON         ; MCLR Pin Enable bit (MCLR pin enabled; RE3)

; CONFIG4L
CONFIG STVREN = ON        ; Stack Full/Underflow Reset Enable bit (Stack)
CONFIG LVP = OFF          ; Single-Supply ICSP Enable bit (Single-Supply)
CONFIG XINST = OFF        ; Extended Instruction Set Enable bit (Instruction)

; CONFIG5L
CONFIG CP0 = OFF          ; Code Protection bit (Block 0 (000800-001FFF))
CONFIG CP1 = OFF          ; Code Protection bit (Block 1 (002000-003FFF))
CONFIG CP2 = OFF          ; Code Protection bit (Block 2 (004000-005FFF))
CONFIG CP3 = OFF          ; Code Protection bit (Block 3 (006000-007FFF))

; CONFIG5H
CONFIG CPB = OFF          ; Boot Block Code Protection bit (Boot block)
CONFIG CPD = OFF          ; Data EEPROM Code Protection bit (Data EEPROM)

; CONFIG6L
CONFIG WRT0 = OFF         ; Write Protection bit (Block 0 (000800-001FFF))
CONFIG WRT1 = OFF         ; Write Protection bit (Block 1 (002000-003FFF))
CONFIG WRT2 = OFF         ; Write Protection bit (Block 2 (004000-005FFF))
```

```

CONFIG WRT3 = OFF           ; Write Protection bit (Block 3 (006000-007F)
; CONFIG6H
CONFIG WRTC = OFF           ; Configuration Register Write Protection bit
CONFIG WRTB = OFF           ; Boot Block Write Protection bit (Boot block
CONFIG WRTD = OFF           ; Data EEPROM Write Protection bit (Data EEPROM

; CONFIG7L
CONFIG EBTR0 = OFF          ; Table Read Protection bit (Block 0 (000800-
CONFIG EBTR1 = OFF          ; Table Read Protection bit (Block 1 (002000-
CONFIG EBTR2 = OFF          ; Table Read Protection bit (Block 2 (004000-
CONFIG EBTR3 = OFF          ; Table Read Protection bit (Block 3 (006000-

; CONFIG7H
CONFIG EBTRB = OFF          ; Boot Block Table Read Protection bit (Boot

    org 0x00

goto Initial
ISR:
    org 0x08                ; 大致效果：每0.5秒會進入一次interrupt
    COMF LATA                ; interrupt會開關LATA一次
    BCF PIR1, TMR2IF         ; 離開前記得把TMR2IF清空（清空flag bit）
    RETFIE

Initial:
    MOVLW 0x0F
    MOVWF ADCON1
    CLRF TRISA
    CLRF LATA
    BSF RCON, IPEN
    BSF INTCON, GIE
    BCF PIR1, TMR2IF         ; 為了使用TIMER2，所以要設定好相關的TMR2IF、TMR2IE、
    BSF IPR1, TMR2IP
    BSF PIE1, TMR2IE
    MOVLW b'11111111'        ; 將Prescale與Postscale都設為1:16，意思是之後每256
    MOVWF T2CON              ; 而由於TIMER本身會是以系統時脈/4所得到的時脈為主
    MOVLW D'122'             ; 因此每256 * 4 = 1024個cycles才會將TIMER2 + 1
    MOVWF PR2                ; 若目前時脈為250khz，想要Delay 0.5秒的話，代表每經過
                                ; 因此PR2應設為 125000 / 1024 = 122.0703125，約123
    MOVLW D'00100000'
    MOVWF OSCCON              ; 記得將系統時脈調整成250kHz

main:
    bra main

end

```

