

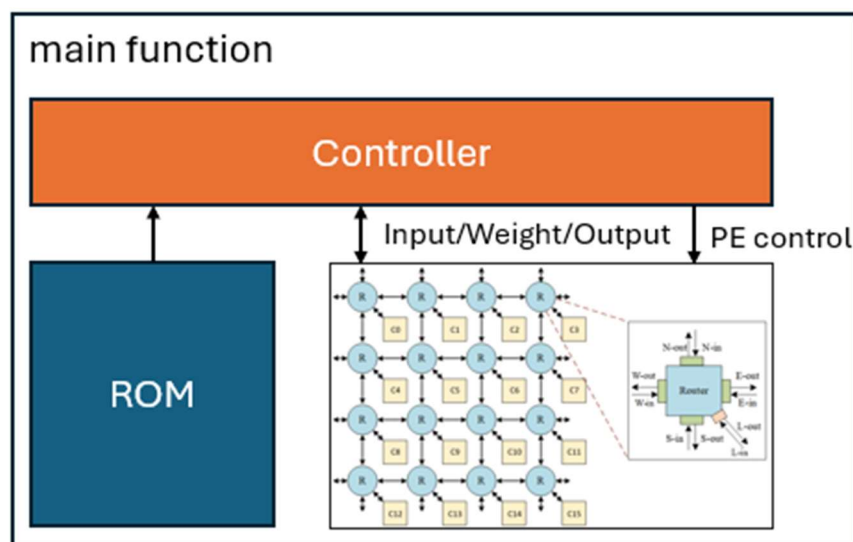
# Machine Learning Intelligent Chip Design

## [HW4] Integrate PEs into a NoC

### Description

In HW2, you can partition your neural network model by channel. In HW3, you use the 4x4 mesh-based NoC architecture to transfer packet from PE to PE. In this HW4, you should replace the PEs in HW3 with neurons from HW2 and integrate them into the NoC.

### Implementation Details



- **PE**  
You should place the partition NN layer to each PE and implement a register in the PE to record the destination of packet. The destination will be configured in the initial stage by CPU.
- **Controller**  
The controller will initialize the result destination for each PE. It reads the ROM data and transfers it to the PE. After the calculation is complete, the controller prints the results.
- **ROM**  
This module will read input data, weight and bias of each layer.

- **Router**

You should connect the router to the controller with the same communication protocol in the NoC. The controller will configure the PE control information by this way.

## Implement Notes

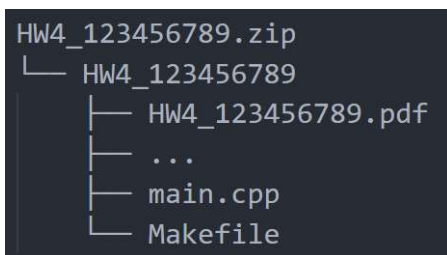
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There are 16 PEs and routers in HW3. Not all PEs and routers should be used with this homework. If your model layer partitions don't require as many resources, you can leave some PEs and routers unused.

## Submission Guidelines

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- **Please compress a folder named HW<ID>\_<student-ID> into a zip file with the same name and upload it to E3.**
- **The folder should include:**
  - Report (Name: HW<ID>\_<student ID>.pdf)
  - Codes
  - Makefile
- **Example:**



```
HW4_123456789.zip
├── HW4_123456789
│   ├── HW4_123456789.pdf
│   ├── ...
│   ├── main.cpp
│   └── Makefile
```

- **Ensure that your code is well-commented and organized for clarity and understanding.**
- **Plagiarism is forbidden, otherwise you will get 0 point!!!**

## Deliverables

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- **SystemC Implementation:**

Use SystemC to implement the 4x4 mesh-based NoC architecture.
- **Report:**

A brief report document containing

  - Simulation results with your workstation account.
  - How do you design the router and NI? What routing algorithm do you use? What is the depth of the buffer? Do you use virtual channels?
  - Your implementation approach, challenges faced, and any observations or insights gained during the implementation and simulation process.