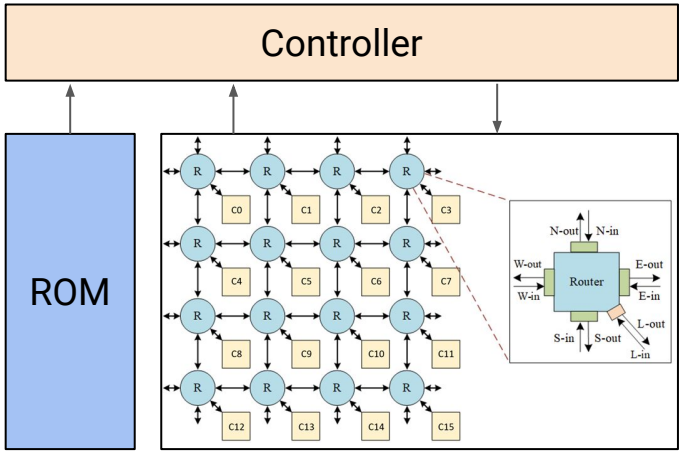
Machine Learning Intelligent Chip Design 2024 Spring

Final Project

Description

In final project, you should use the system architecture completed in HW4 and accomplish the following two tasks:

1. Use PA to simulate your HW4 architecture.
2. Rewrite the router module using Verilog and run co-simulate on PA.



Requirement

- You need to use at least **4** cores and **4** routers in your NoC architecture.
- Your router should be designed as a **sequential circuit**.
  (i.e. trigger only by reset and clock)
- Please attach the screenshots of the **block diagram** and **simulation result of PA** with your report.

Grading Policy

- Simulation Correctness on PA with Verilog version of router (80%)
- Report (20%)

Report

- Screenshots of the block diagram and simulation result of PA.
- How do you control the NoC? What is each module responsible for? (If you wrote it in the previous report, you can copy and paste it here.)
- Your implementation approach, challenges you face, and any observations or insights gained during the implementation and simulation process.

Submission

- Please compress a folder named **FP_<student ID>** into a zip file with the same name and upload it to E3.
- The folder should include:
  - Report (Name: FP_<student ID>.pdf)
  - Codes
  - Makefile
- Ensure that your code is well-commented and organized for clarity and understanding.
- **Plagiarism is forbidden, otherwise you will get 0 point!!!**

Bonus

- You can choose one topic in this class about NoC design methodology and do analysis based on HW4 by systemC. And you will get the extra bonus. There are some topic listed below for your reference.
  - For NoC
    - Routing policy (e.g., XY routing, west-first adaptive routing, etc.)
    - NoC topology (e.g., Mesh, Torus, etc.)
    - Virtual channel
    - Flow control
  - For DNN model
    - Data reuse
    - Output/input/weight stationary

Bonus Rule

- You don’t need to do co-sim by PA.
- Bonus points will be added to the HW score.
- You should submit another report describing the results of your analysis.
- Please clearly indicate the process and results of performance measurement in your report.
- The performance of your architecture can be analyzed using the following criteria.
  - Simulation time
  - Number of floating point multipliers in each Core.
  - etc.