# ECE385 Experiment #3

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## I. Introduction

THE purpose of this lab is to design and construct a four-bit serial logic processor that performs a total of eight logical operations in a bit-wise fashion. There are two four-bit words stored in two shift registers.

## II. Pre-Lab

Part A) Describe the simplest (two-input one-output) circuit that can optionally invert a signal (i.e., one input determines if the output is equal to the other input or equal to the other input inverted). Sketch your circuit.

Answer: The logic needed is shown in the following truth table:

| A | B | Inverted? |
|---|---|---|
| 0 | 0 | Yes |
| 0 | 1 | No |
| 1 | 0 | No |
| 1 | 1 | Yes |

This truth table can be created using a NXOR gate which is essentailly a comparator.

SHOW DIAGRAM FOR PART A HERE

Part B) Explain how a modular design such as that presented above improves testability and cuts down development time. Propose an approach that could be used to troubleshoot the modular circuit above if it appeared to be completing the computation cycle correctly but was not giving the correct output. (Be specific.)

Answer: A modular design allows the operator to unit-test each individual module. Once each module is successfully tested, the entire system can be integrated into a whole-system and tested. A modular design ideally will cut down the debugging time needed on the system as a whole.

## III. Description of Circuit

The team designed a total of four modular sub-systems in this lab. The following sub-systems were designed and constructed:

1) Loader and Data In
2) Computation Unit
3) Function Output Router
4) Control Logic Finite State Machine (FSM)

Each sub-system was tested individually and system integration tests were performed at the end

## IV. State Diagram

## V. Design

## VI. Block Diagram

## VII. Circuit/Logic Diagrams

Please refer t

## VIII. Component Layout Sheet

## IX. Documentation from Experiment

## X. Conclusion

## XI. Figures