ECE385 Experiment #5

Eric Meyers, Ryan Helsdingen

Section ABG; TAs: Ben Delay, Shuo Liu

February 24th, 2016

emeyer7, helsdin2

I. Introduction

The purpose of this lab was to design and construct a 2s compliment 8-bit multiplier that uses a shift-and-add algorithm. The user will input their desired multiplicand and multiplier into switches and these will be stored in two shift registers (A and B). The multiplier is built upon a control unit with a state machine, so once the ”run” button is pressed, the machine will cycle through multiple states and output the value in the combined 16-bit value ”AB”.

II. 8-bit Multiplication Example

RYAN SECTION
The multiplier

III. Purpose of Modules

The multiplier is broken down into four primary modules as listed below:

- Shift Register
- Full Adder/Subtractor
- Control Unit
- X Register

The first of these modules is the shift register and it’s purpose is to store the contents of each 8-bit word the user specifies.

The control unit is meant to determine the states of

IV. State Diagram

RYAN SECTION

V. Schematic/Block Diagram

Please refer to ”Section X : Figures” of this document to view the Schematic/Block Diagrams. Figure 5 displays the entire block diagram of the multiplier, with block labels and interconnections. The multiplier, as stated before is broken down into several modules. Those modules are as follows with the figure references aside them:

- Shift Register - Figure 6
- Full Adder/Subtractor - Figure 7
- Control Unit - Figure 8 (Top Half Only)
- Control Unit - Figure 9 (Bottom Half Only)
- X Register - Figure 10

VI. Pre-Lab Simulation Waveforms

Please refer to ”Section X : Figures” of this document to view the Pre-Lab Simulation Waveforms. There was a total of four simulations performed. All options were explored on this multiplier and the following inputs were used:

- +7 * -59 - (Figure 1)
- -7 * +59 - (Figure 2)
- +7 * +59 - (Figure 3)
- -7 * -59 - (Figure 4)

VII. Post Lab

RYAN SECTION

VIII. Conclusion

RYAN OR ERIC

IX. Figures

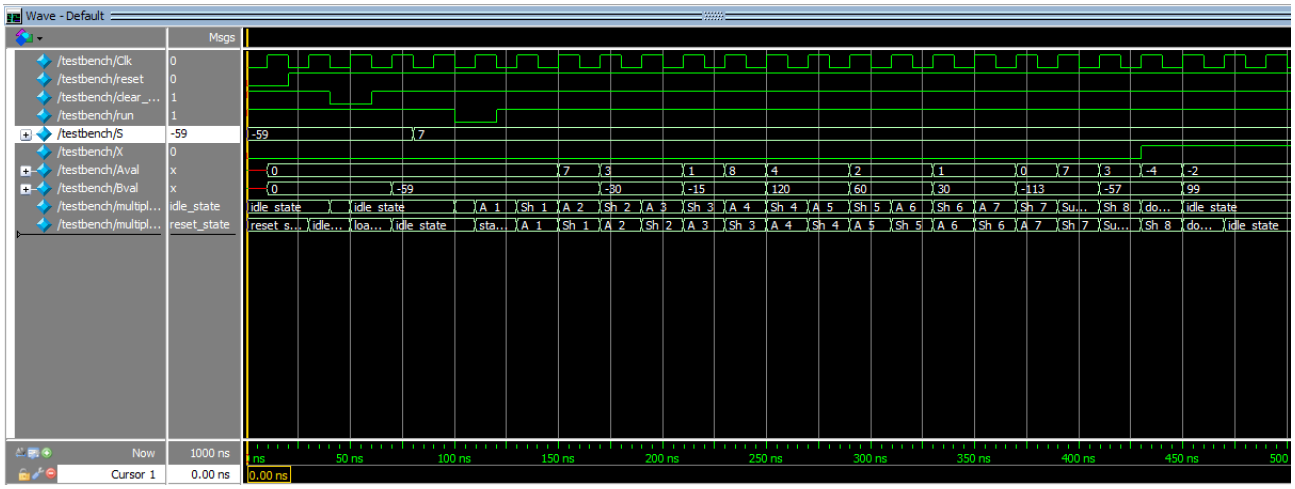

Fig. 1: ModelSim Simulation Output (+7 * -59)

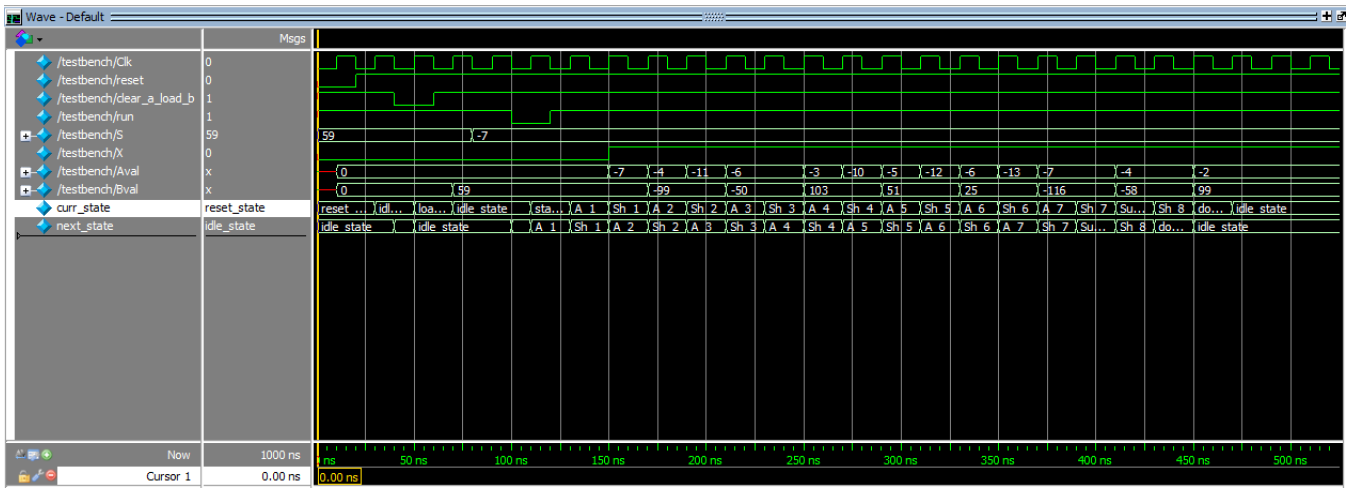

Fig. 2: ModelSim Simulation Output (-7 * +59)

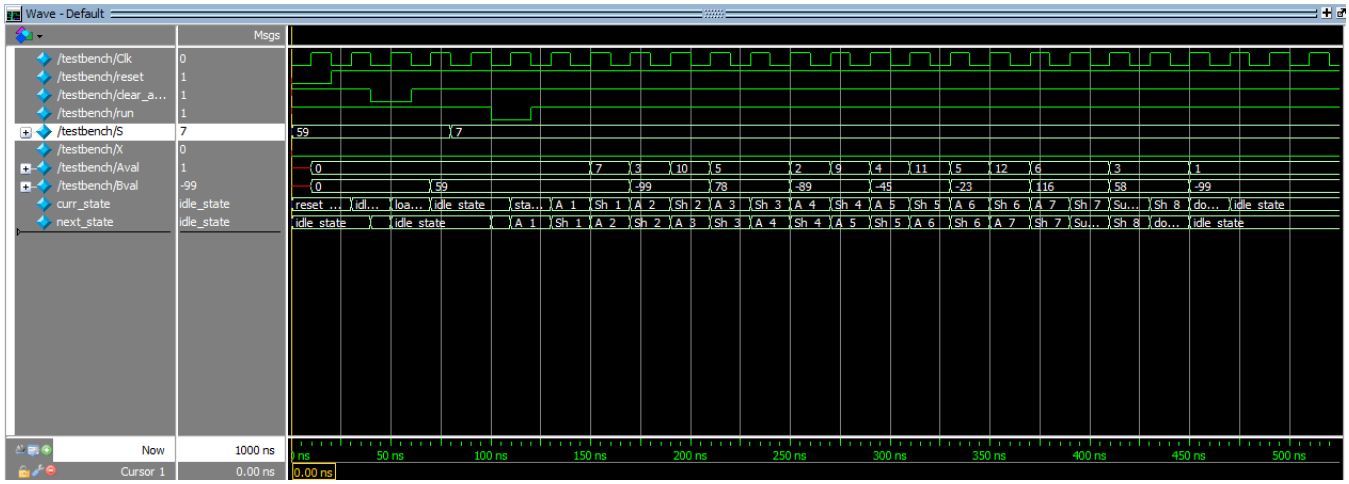

Fig. 3: ModelSim Simulation Output (+7 * +59)

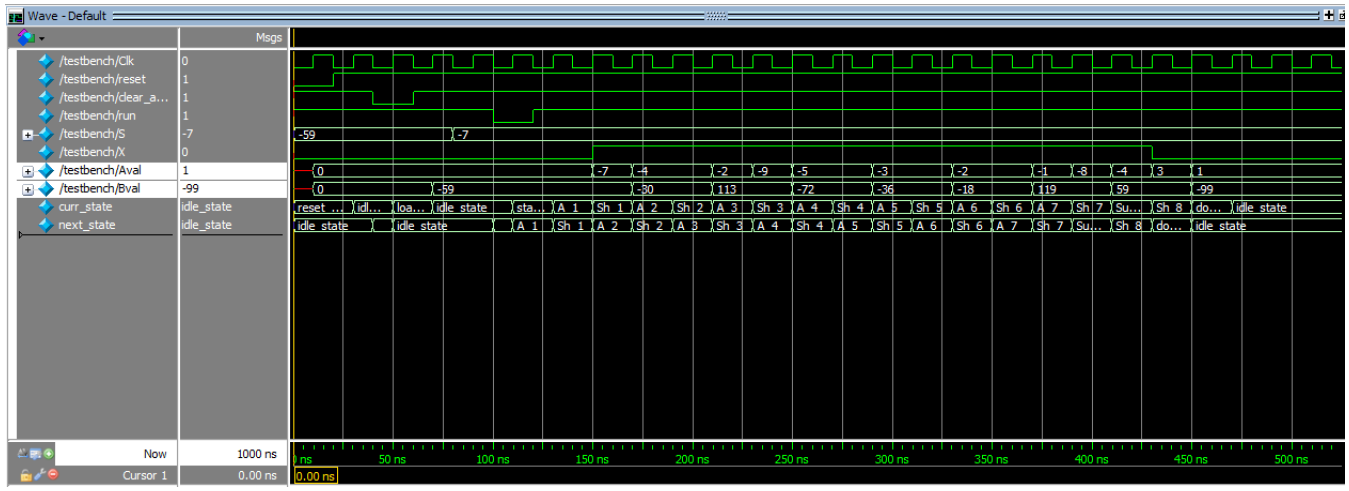

Fig. 4: ModelSim Simulation Output (-7 * -59)

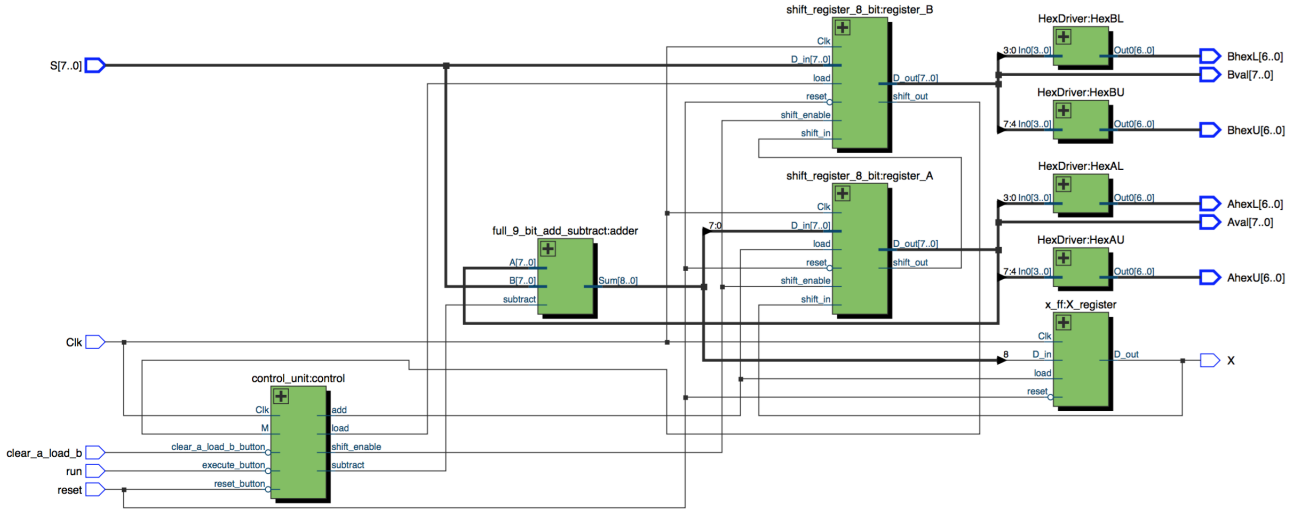

Fig. 5: Full Multiplier Block Diagram

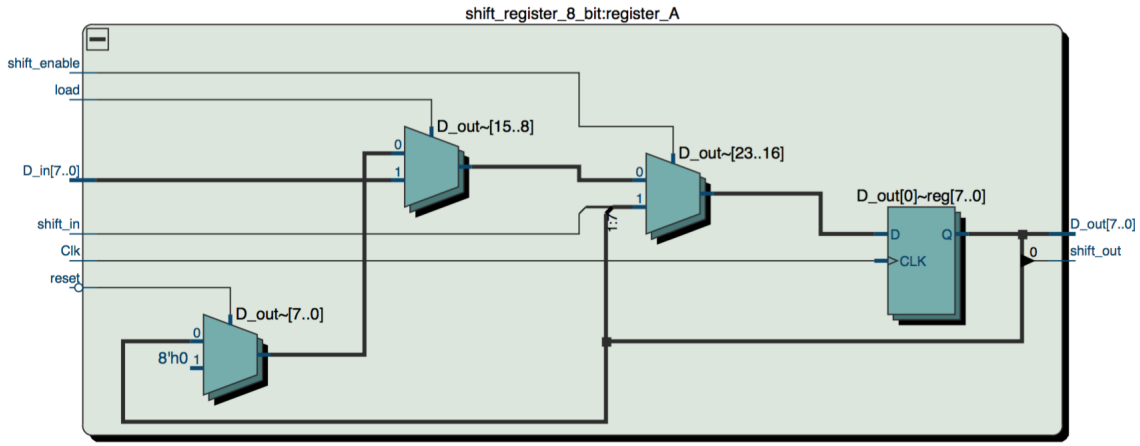

Fig. 6: Shift Register Block Diagram

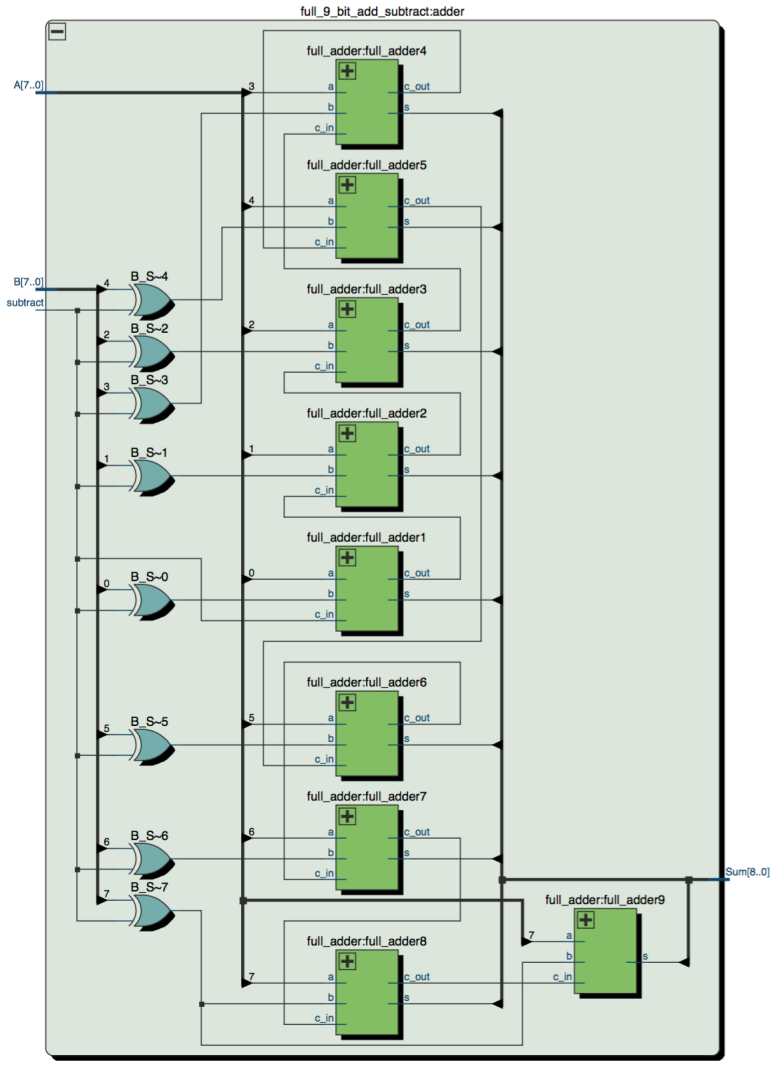

Fig. 7: Full Adder and Subtractor Block Diagram

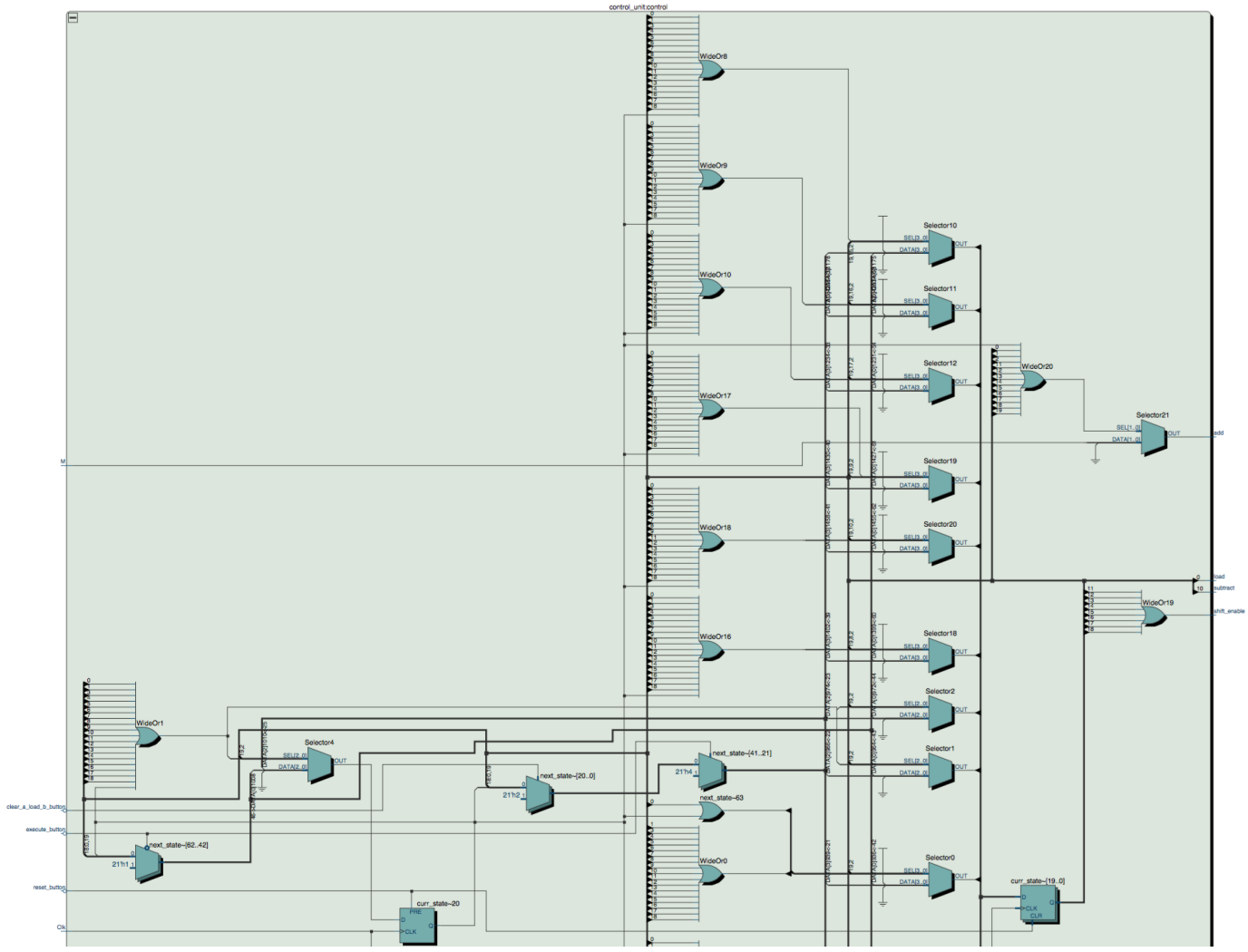

Fig. 8: Top Half Control Unit Block Diagram

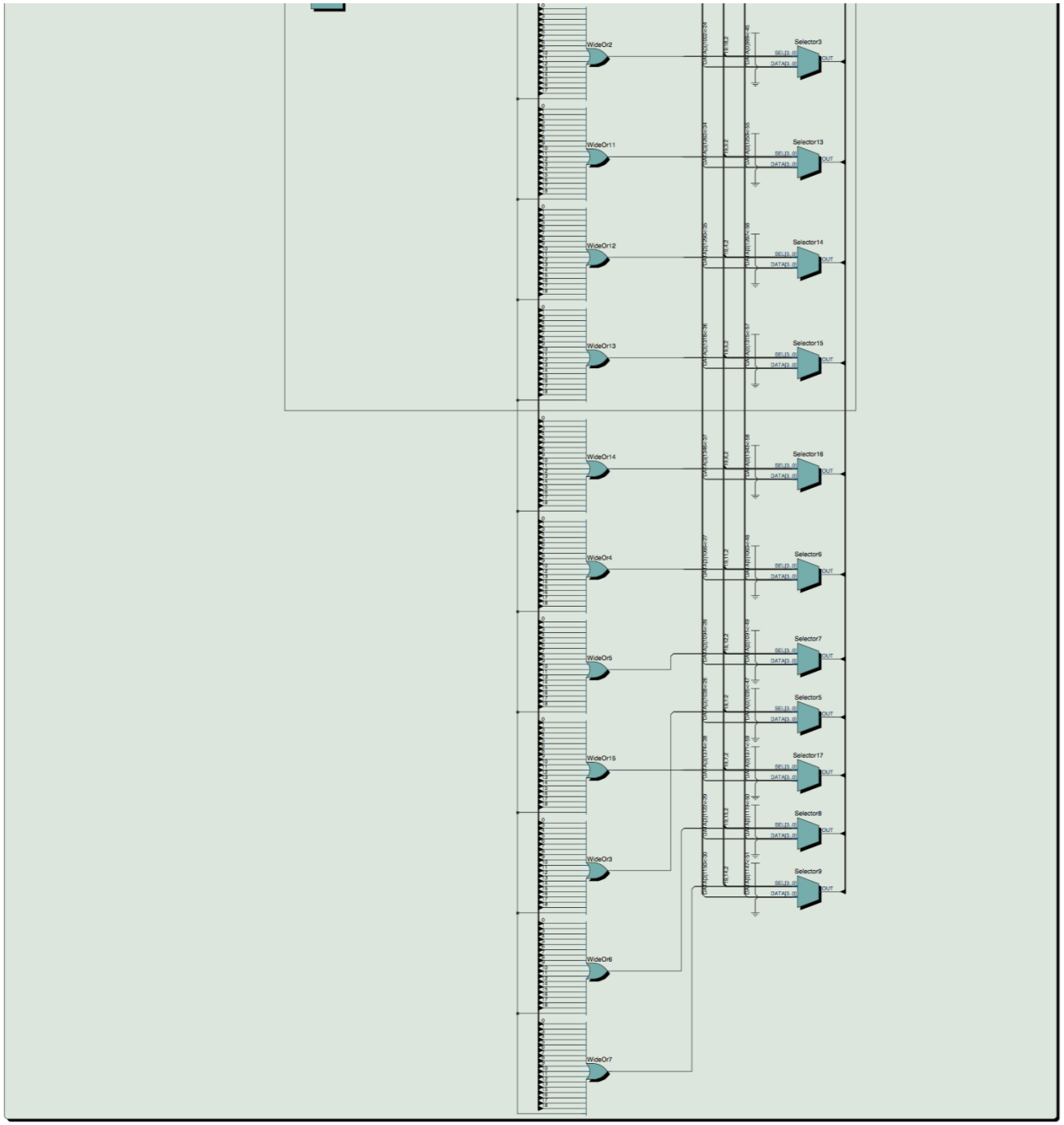

Fig. 9: Bottom Half Control Unit Block Diagram

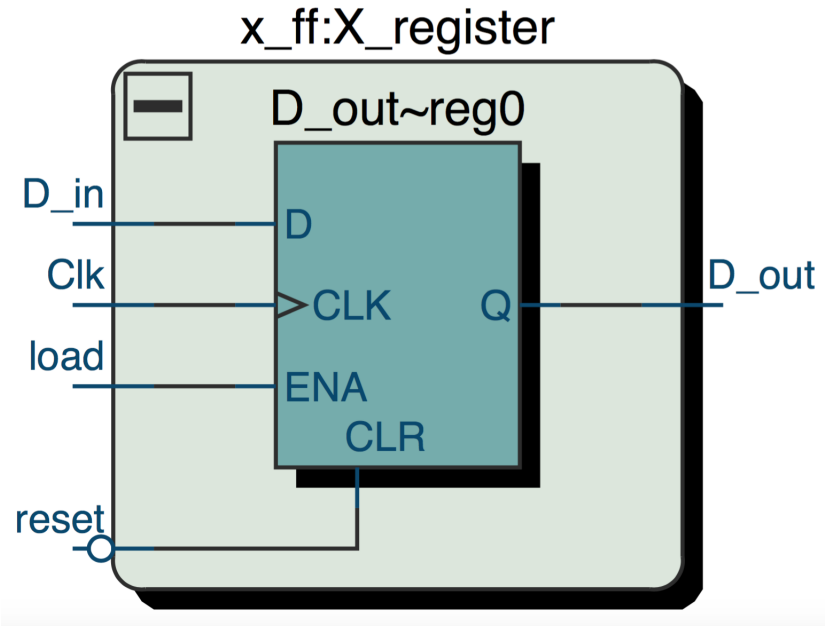

Fig. 10: X-Bit Flip Flop Block Diagram