

ECE 385

Spring 2016

Experiment #1

Introductory Experiment

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ABG – Wednesdays 12-2:50PM

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Introduction

The first lab of ECE 385 is intended to be an introductory lab. Equipment used throughout the course is introduced including the I/O boards, the Agilent MSO 6032A oscilloscope, and the HP 33120A pulse generator. More importantly, this lab applies past concepts such as Karnaugh maps, state diagrams, and truth tables. It then lays down new key concepts such as delays and glitches in the circuit and key techniques for debugging and organized design. All of which will become the foundation for future experiments.

Often overlooked in circuit design is the delay in the gate switching. The SN7400 for example has a maximum Low-to-High switch delay of 20ns and a maximum High-to-Low switch delay of 15ns. In the sample wave plot shown in Fig. 1, you can see this delay as the input signal for B in yellow implements a square wave and after sending these pulses through two or three NAND gates becomes a delayed square wave at the output shown in green.

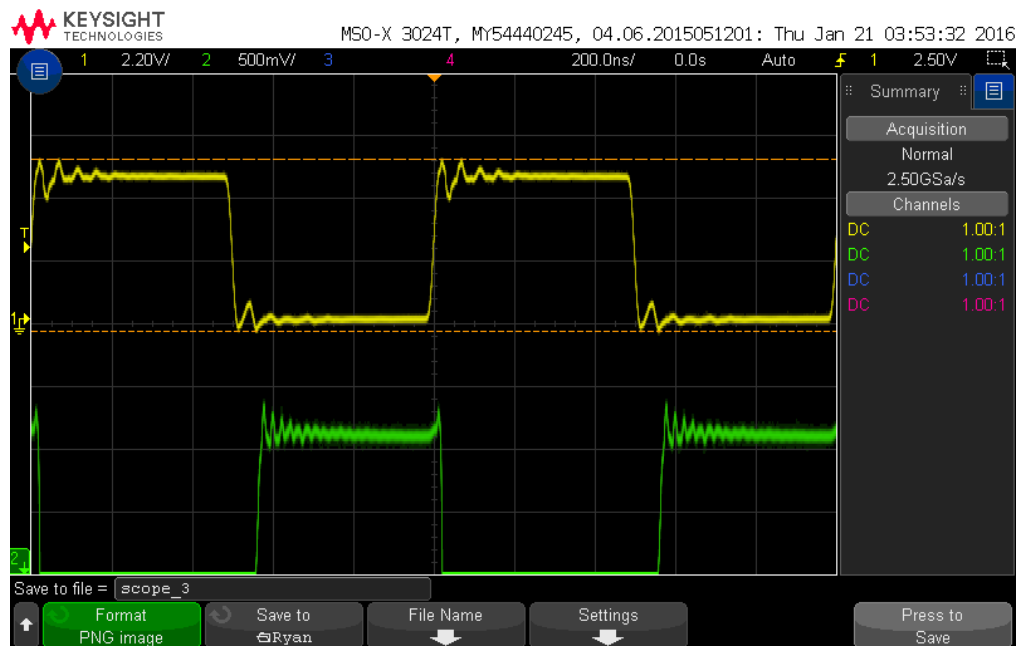


Figure 1: Sample input/output signal for circuit.

Delays such as the one shown can lead to glitches in TTL as was seen in this lab. A glitch occurs when the input changes and the output is incorrect due to it not switching fast enough from the effects of these propagation delays.

Lab Procedure (with answers to questions)

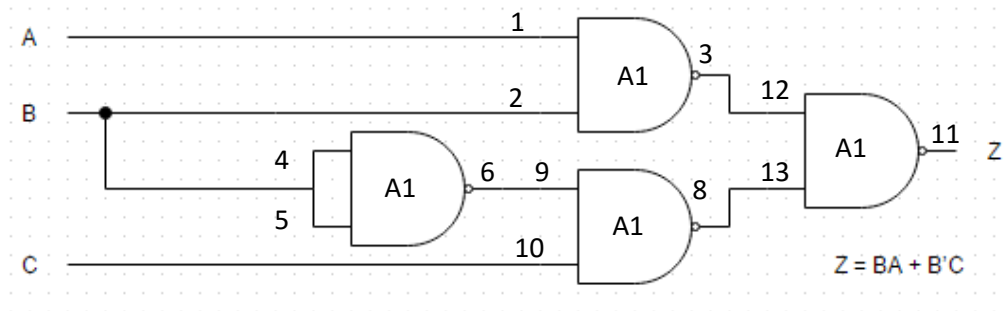


Figure 2: Circuit diagram for Part A.

In this lab, we begin by setting up the logic circuit shown in Figure 2 using an SN7400 Quad 2-input NAND gate. The inputs A, B, and C are all connected to input switches from the I/O board. All three inputs as well as output Z are connected to LEDs on the I/O board. The component layout sheet lays out the first circuit including the NAND gate at location A1. This simple circuit is operated by the switches which give a HIGH signal when the switch is on, and a LOW signal when the switch is off. The LEDs glow red for a LOW signal and green for a HIGH signal. The first circuit follows the logic equation $Z = BA + B'C$. From this equation, a K-Map can be formed.

		BC			
		00	01	11	10
A	0	0	1	0	0
	1	0	1	1	1

Figure 3: K-map for Part A circuit.

Notice that the two loops are not overlapping each other. The NAND gates are not controlled by a clock so they become asynchronous. BA occupies the top half of the circuit and only requires passing through two NAND gates to get to the output. On the other hand, $B'C$ passes through three NAND gates to reach the output which adds a greater delay and can create the glitch. Delay in the output depends on the longest path delay from its inputs. Given the delay through a single NAND is a maximum 20ns, the maximum delay at the output is $3 \times 20\text{ns} = 60\text{ns}$. However, this is not the case for when B goes from LOW to HIGH. $(AB)'$ goes low which makes the value of $(B'C)'$ irrelevant. The length of uncertainty is thus only 40ns for Z during this transition. The timing diagram shown in Figure 4 shows where the delays and uncertainty stack up.

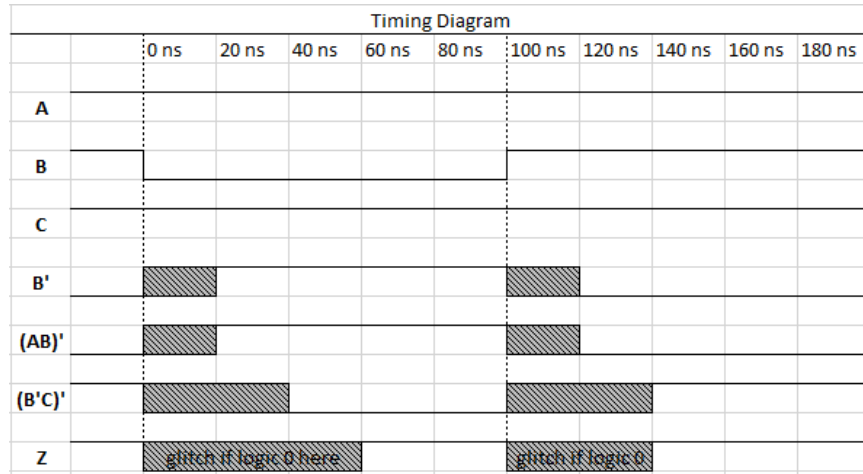


Figure 4: Timing Diagram for Part A circuit.

We visually see this glitch when B is powered by a function generator, generating a square wave operating at 1MHz from 0-5V. In Figure 5, A and C remain HIGH, while B fluctuates between high and low signals. Each time B switches there is a small but finite period of uncertainty in the output. Z fluctuates as the propagation delay tries to catch up to the output. For example, when B drops from HIGH to LOW given A and C are HIGH, BA drops to LOW but B'C may still be LOW because of the propagation delay. This is the glitch since the output Z at that small period of time will want to drop to zero given the 'or' statement when ideally it should remain high. Figure 5 shows that small dip as B goes from HIGH to LOW.

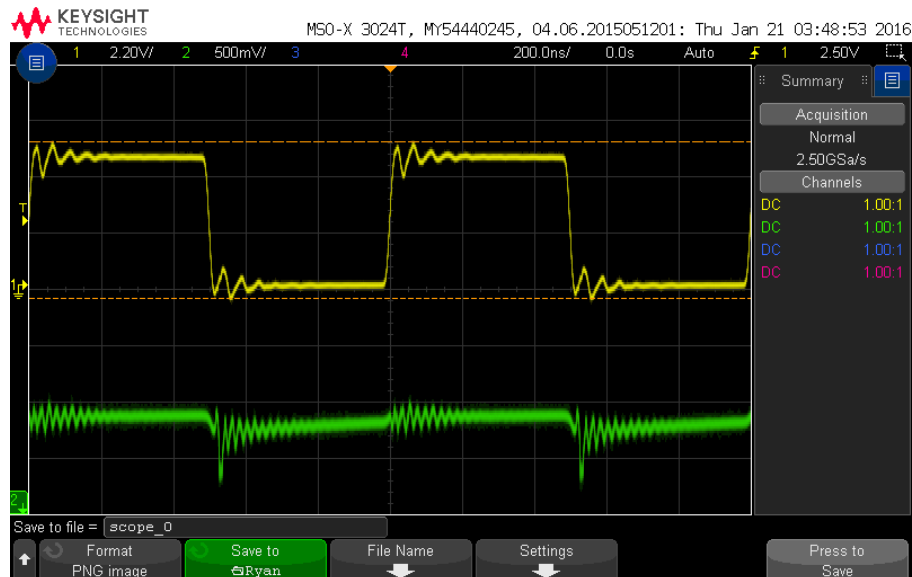


Figure 5: Signal B and output signal Z given A&C HIGH for Part A circuit.

The glitch, however, does not occur when B transitions from LOW to HIGH. BA changes to a high signal before B'C changes to a LOW signal which therefore retains the HIGH signal at the

output as expected. To answer question 2 in the postlab, the only possible unknown region where glitches may appear is where B goes from HIGH to LOW. The maximum length of time of this region is 60ns to account for three NAND gates that the signal must pass through is it generates the B' signal, then the $(B' \cdot C)'$ signal, and lastly the output signal Z.

The results in the waveform in Figure 5 differ from what was expected in the timing diagram in Figure 4. The signal for B is not as clean as the one shown in the timing diagram. This results in a rougher output wave that may have uncertainty in its output greater than the 60ns anticipated.

The circuit is then redesigned to eliminate this glitch. In order to do so, the two separated loops in the K-map must be linked together. While this creates redundancy, it is necessary for the two loops to become synchronized to minimize the glitch. The blue oval demonstrates this added link. The new equation for output becomes $Z' = BA + B'C + AC$.

		BC			
		00	01	11	10
A	0	0	1	0	0
	1	0	1	1	1

Figure 6: K-map for Part B circuit.

The circuit diagram now must be adjusted to the one in Figure 7. While it requires three more NAND gates, adding the redundancy helps to cover the gaps in the correct output signal that propagation delay may cause and reduce the glitch in the output.

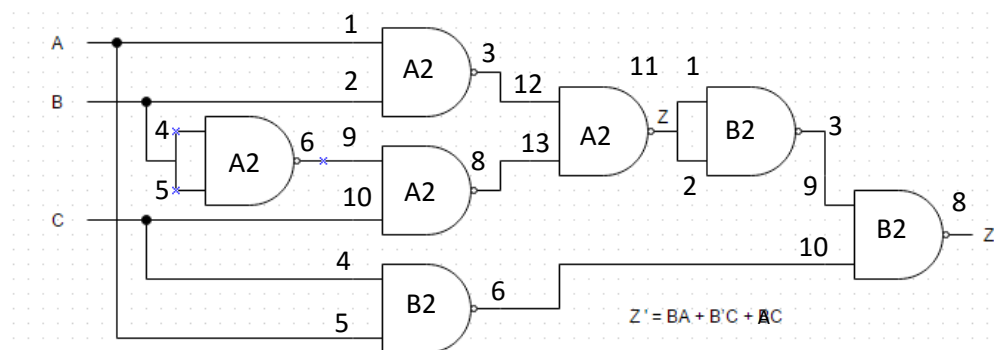


Figure 7: Circuit diagram for Part B.

Going back to the example earlier, when B drops from HIGH to LOW given A and C are HIGH, BA drops to LOW but $B'C$ may still be LOW because of the propagation delay. Adding the AC term will have the output always remain high since A and C are each always high thus fulfilling the 'or' statement. This addition can be added without affecting the output truth table since it is considered redundancy.

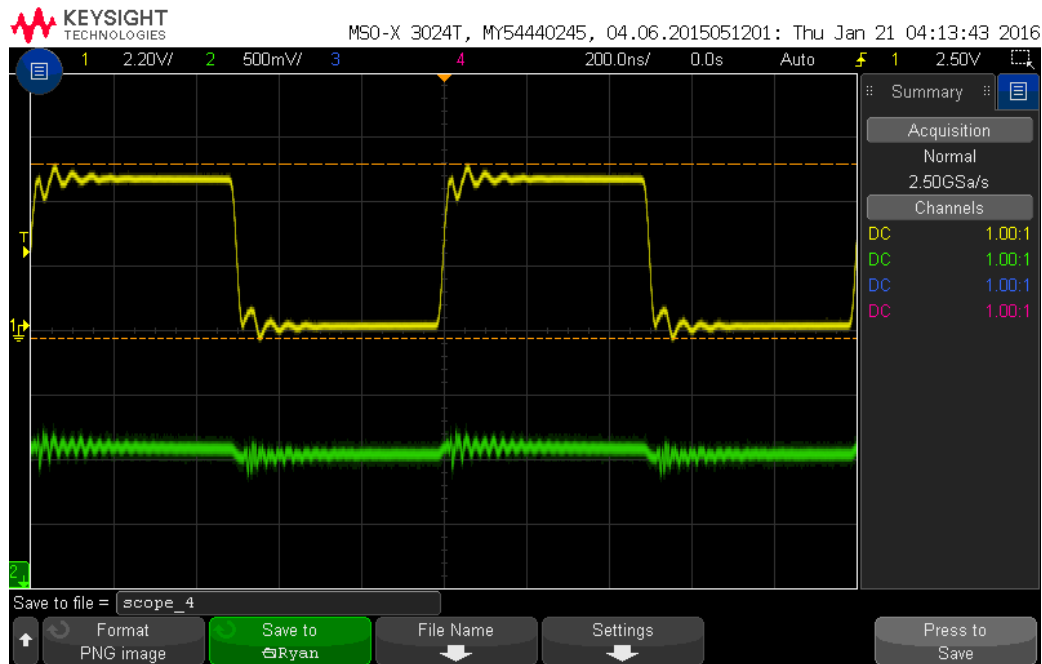


Figure 8: Signal B and output signal Z' given A&C HIGH for Part B circuit.

Using the same three input switches for part B, to the human eye it still responds the same as part A did. However, the difference is on the oscilloscope. Figure 8 shows the signal at B in yellow and the output signal in green. Notice the output signal is smoother than the one shown in Figure 5. This is thanks to the redundant AC term added in Part B.

Another problem with TTL that is already accounted for in this lab but should not be brushed under the rug is contact bounce. This occurs when the input switch is flipped and the mechanical contact bounces ever so slightly for milliseconds after the switch is flipped. This may not cause noticeable problems, but if the problem were not taken care of for this lab, it would be a problem since we are dealing with high frequencies. Figure 17 on page GG.32 of the general guide shows the Debouncer. The Debouncer is essentially an SR NAND latch. It is called a latch because it latches on to the signal. S stands for set and is represented by A in the diagram. R stands for reset and is represented by B in the diagram. When C comes into contact with A, D goes to ground and therefore Q must be HIGH. On the other hand, when C comes into contact with B, G goes to ground and therefore QN must be HIGH and Q must be LOW. The trick of this latch is when C is neither touching A nor B, for example when it bounces. In this state, both S and R = 1 and nothing happens to the output. This eliminates the contact bounce issue. In other words the latch requires only a single pulse to A in order to make Q HIGH, and only a single pulse to B to return Q to LOW.

Conclusion

The first lab worked through many of the topics of the General Guide such as delays/glitches, circuit bouncing, timing diagrams, debugging, and logic diagrams as well as refresher topics from ECE 198JL (now ECE 120) such as K-maps and truth tables.

This lab successfully found the glitch in the circuit. It proved that a circuit as simple as the one in Part A can suffer from the imperfect reality of TTL chips and hold that glitch. Although the circuit from Part B logically displayed the same results, its redundancy by adding the AC term eliminated the Static-1 Hazard that Part A had when input B transitioned from HIGH to LOW.