

ECE385 Experiment #5

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I. INTRODUCTION

The purpose of this lab was to design and construct a 2s compliment 8-bit multiplier that uses a shift-and-add algorithm. The user will input their desired multiplicand and multiplier into switches and these will be stored in two shift registers (A and B). The multiplier is built upon a control unit with a state machine, so once the "run" button is pressed, the machine will cycle through multiple states and output the value in the combined 16-bit value "AB".

II. 8-BIT MULTIPLICATION EXAMPLE

RYAN SECTION

III. DESCRIPTION OF CIRCUIT

ERIC SECTION

IV. PURPOSE OF MODULES

ERIC SECTION

V. STATE DIAGRAM

RYAN SECTION

VI. SCHEMATIC/BLOCK DIAGRAM

Please refer to "Section X : Figures" of this document to view the Schematic/Block Diagrams. Figure 2 displays the entire block diagram of the multiplier, with block labels and interconnections. The multiplier, as stated before is broken down into several modules. Those modules are as follows with the figure references aside them:

- Shift Register - Figure 3
- Full Adder/Subtractor - Figure 4
- X Register - Figure 7
- Control Unit - Figure 5 (TOP HALF ONLY)
- Control Unit - Figure 6 (BOTTOM HALF ONLY)

VII. PRE-LAB SIMULATION WAVEFORMS

Please refer to "Section X : Figures" of this document to view the Pre-Lab Simulation Waveforms. There was a total of four simulations performed. All options were explored on this multiplier and the following inputs were used:

- $+7 * +59$ - (Figure _)
- $+7 * -59$ - (Figure _)
- $-7 * +59$ - (Figure _)
- $-7 * -59$ - (Figure _)

VIII. POST LAB

RYAN SECTION

IX. CONCLUSION

RYAN OR ERIC

X. FIGURES

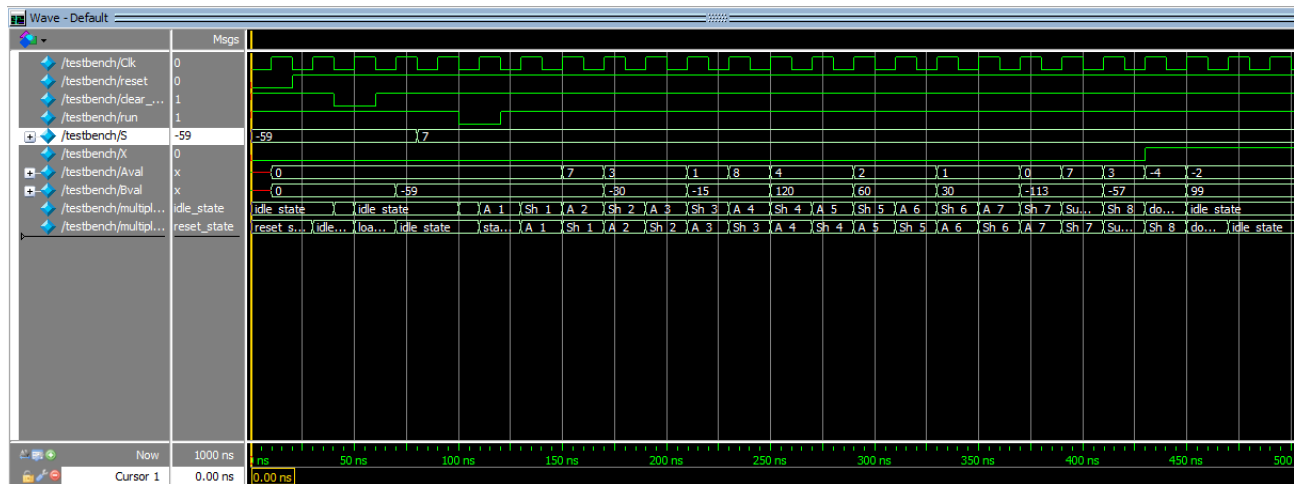


Fig. 1: ModelSim Simulation Output (+7 * -59)

NEED 3 MORE SIMULATIONS!!!!

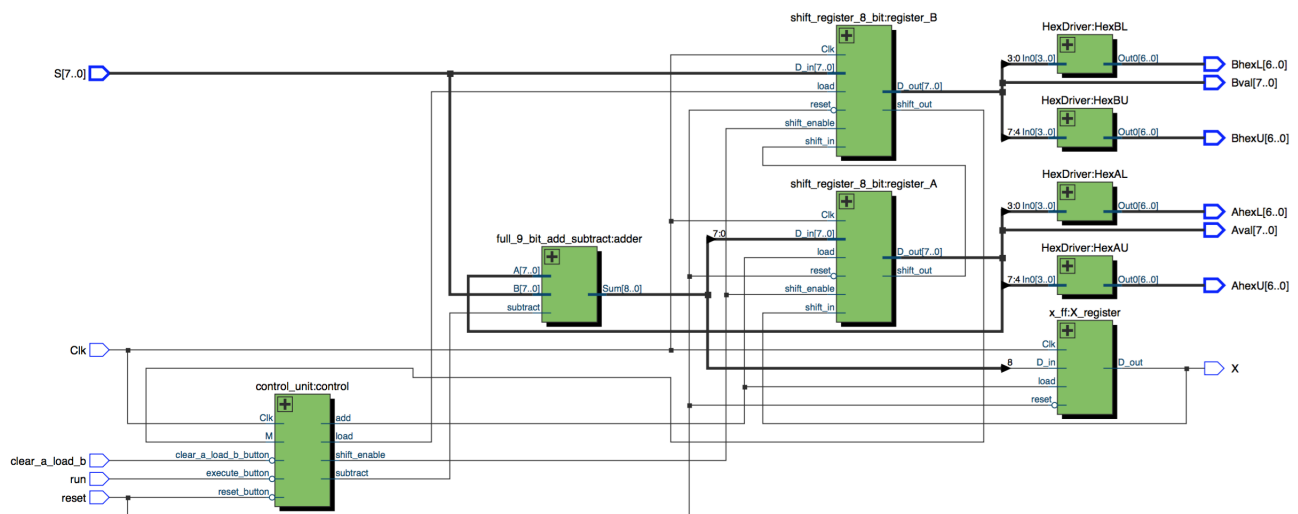


Fig. 2: Full Multiplier Block Diagram

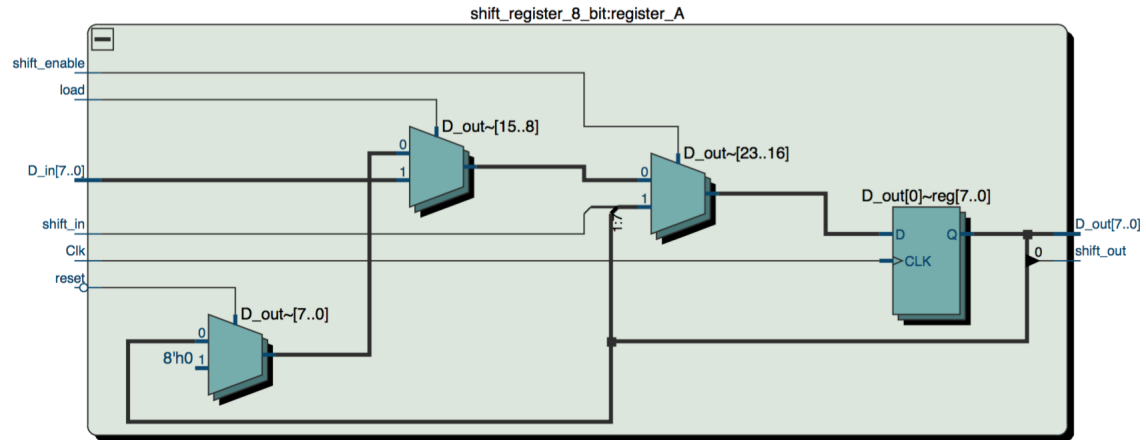


Fig. 3: Shift Register Block Diagram

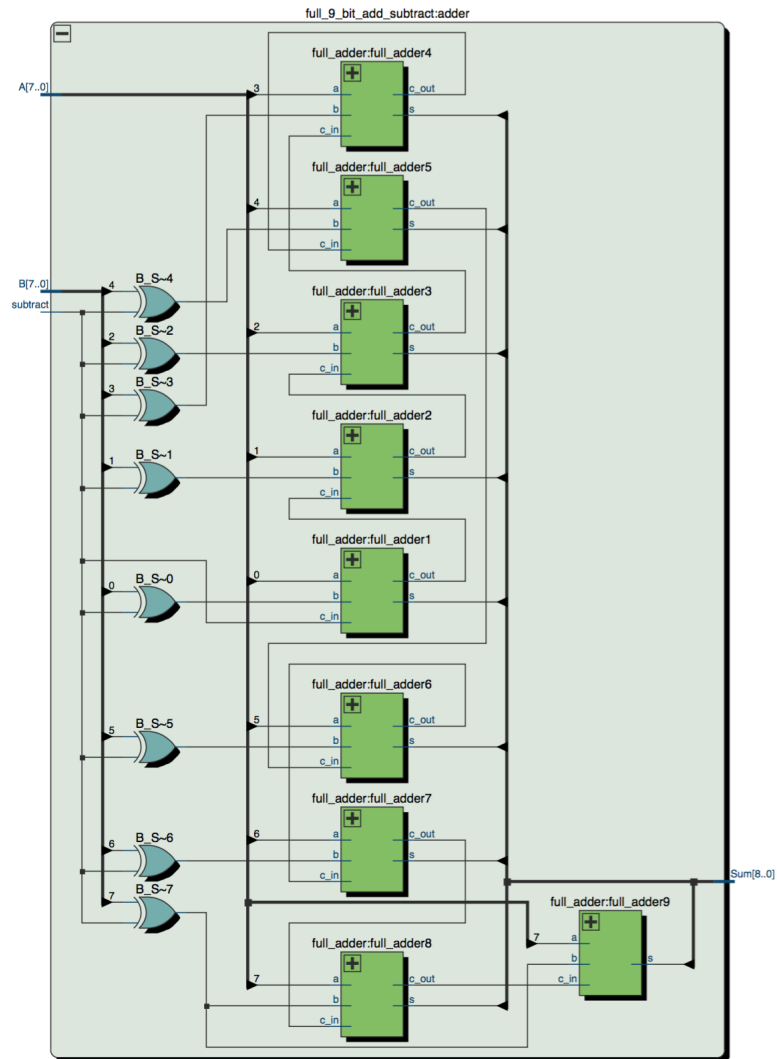


Fig. 4: Full Adder and Subtractor Block Diagram

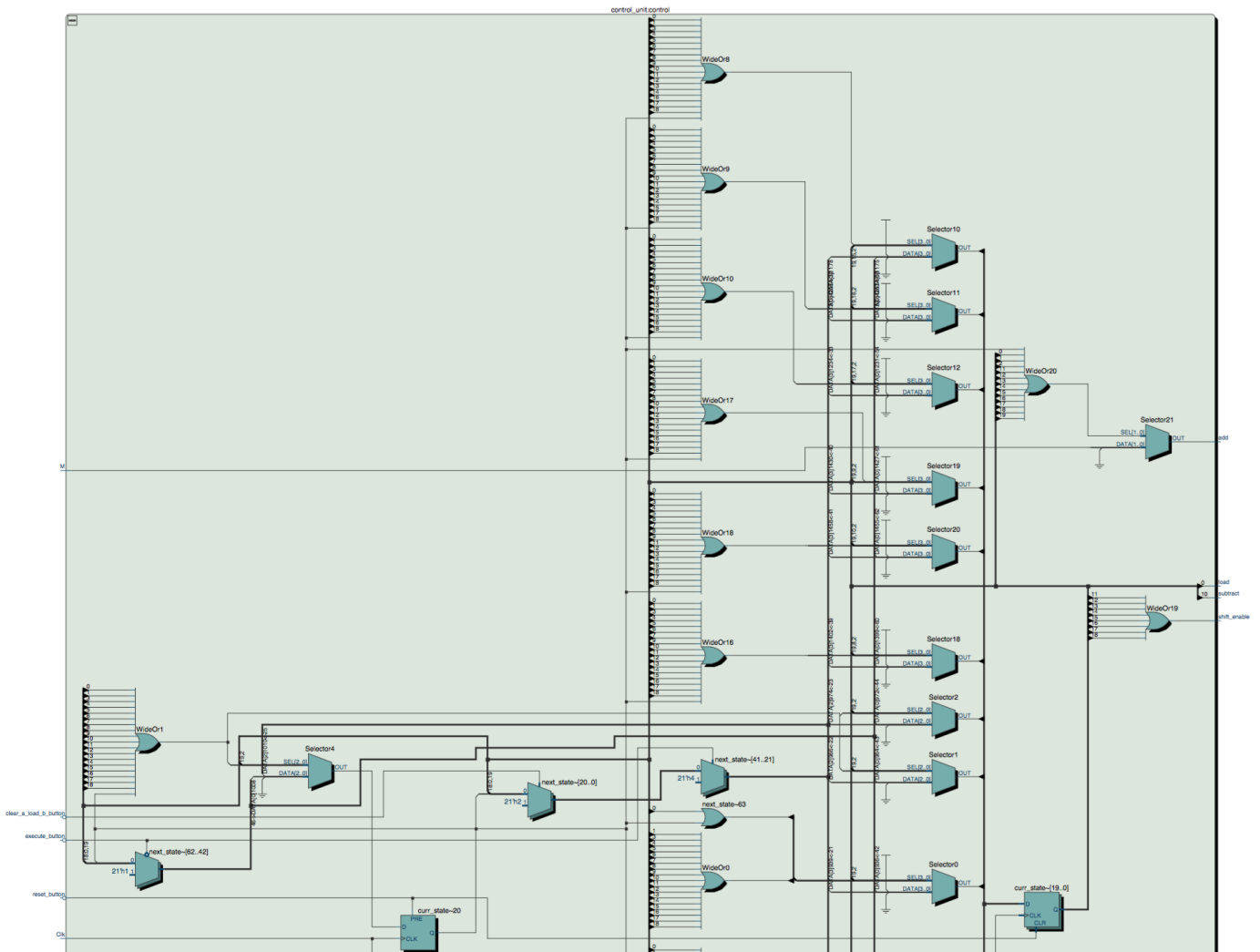


Fig. 5: Top Half Control Unit Block Diagram

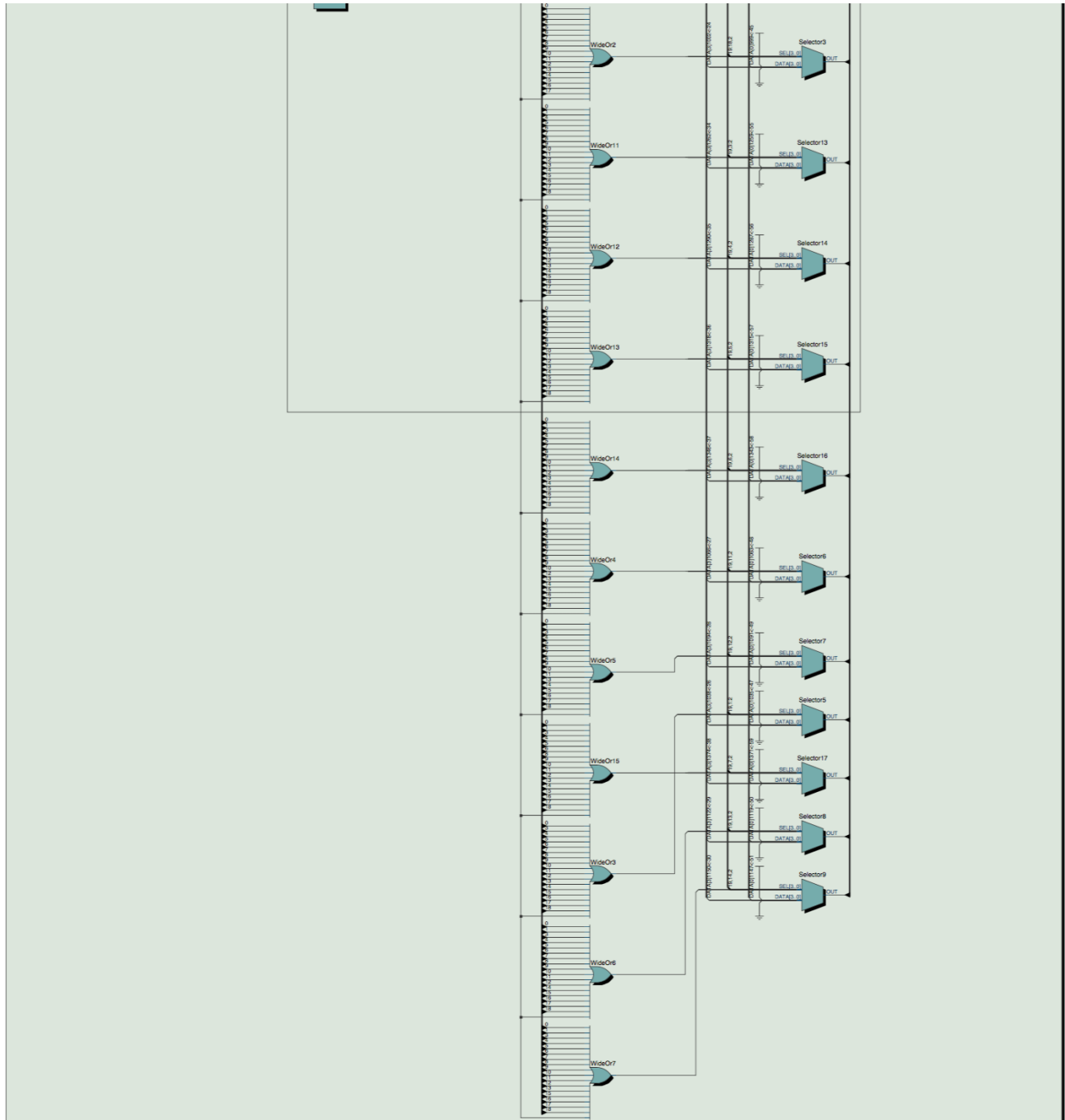


Fig. 6: Bottom Half Control Unit Block Diagram

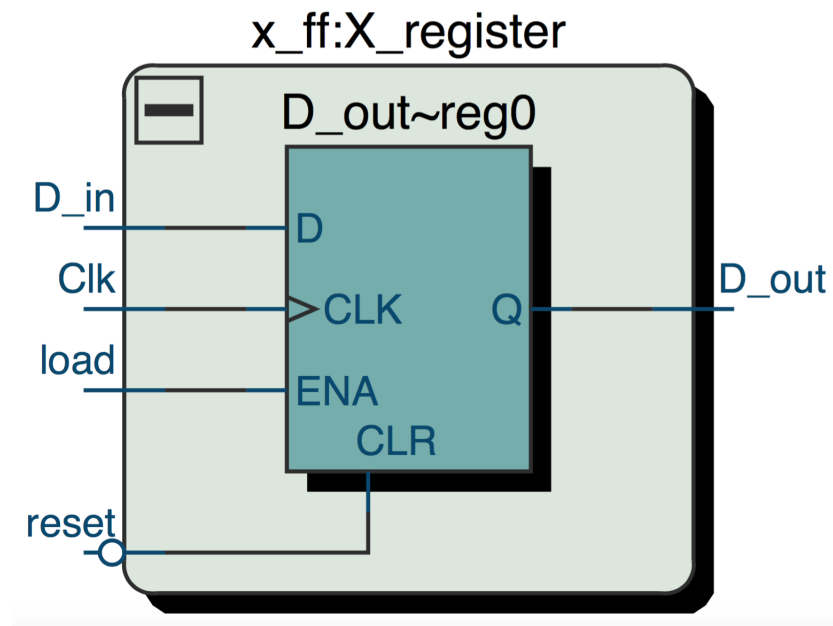


Fig. 7: X-Bit Flip Flop Block Diagram