ECE385 Experiment #4

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I. Introduction

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II. Schematic of Logic Processor

Please refer to Figure 1 in ”Section XI: Figures” to view the Schematic of the 8-bit Logic Processor designed in the Pre-Lab of this Experiment.

III. Design Simulations of Logic Processor

Please refer to Figure 2 in ”Section XI: Figures” to view the Annotated RTL Simulation Output of the 8-bit Logic Processor designed in the Pre-Lab of this Experiment.

IV. Written Description of Adder Circuit

V. Purpose of Modules

VI. State Machine

VII. Schematic Block Diagrams

VIII. Design Analysis Comparison

IX. Post-Lab

X. Conclusion

XI. Figures

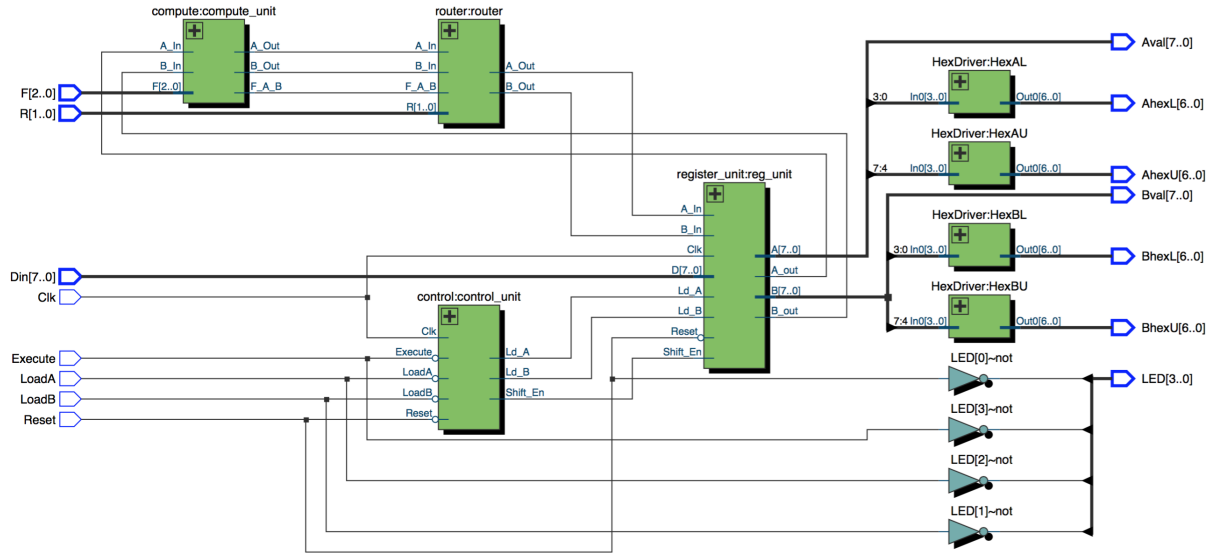

Fig. 1: Serial Logic Processor Schematic

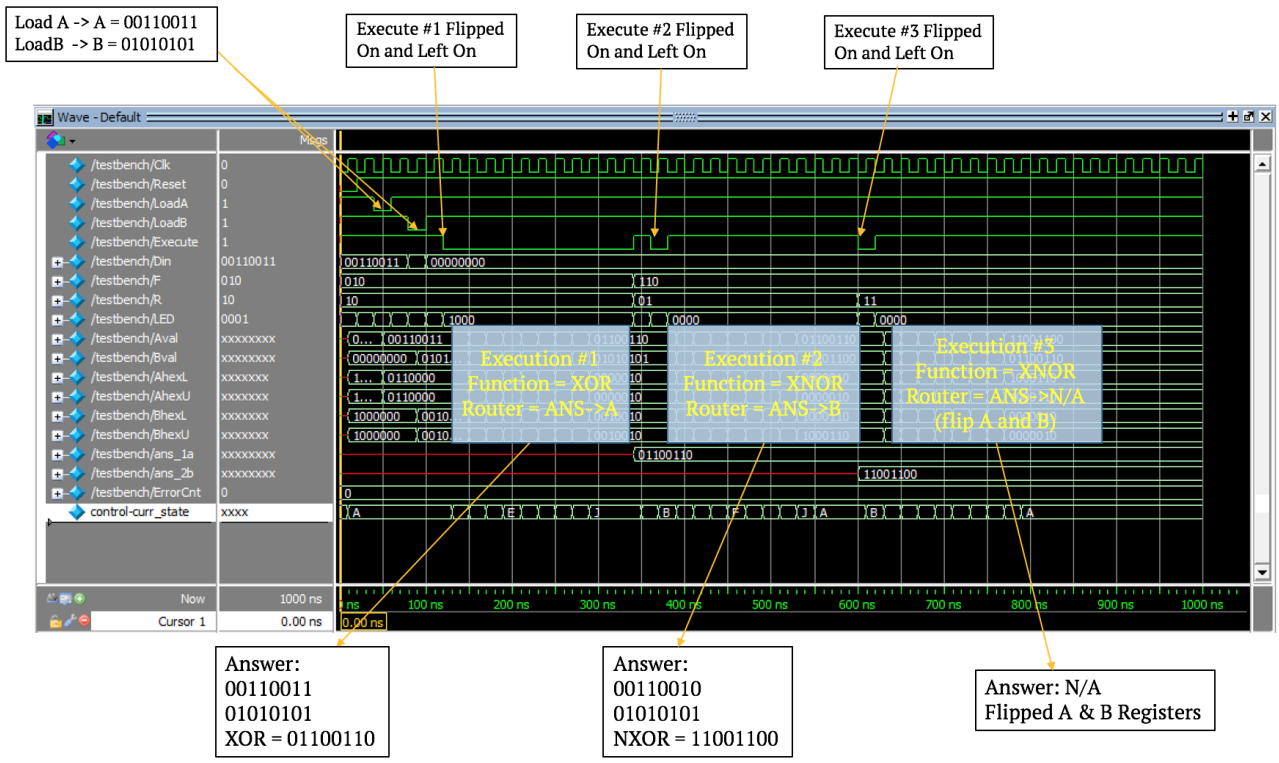

Fig. 2: Serial Logic Processor RTL Simulation Output

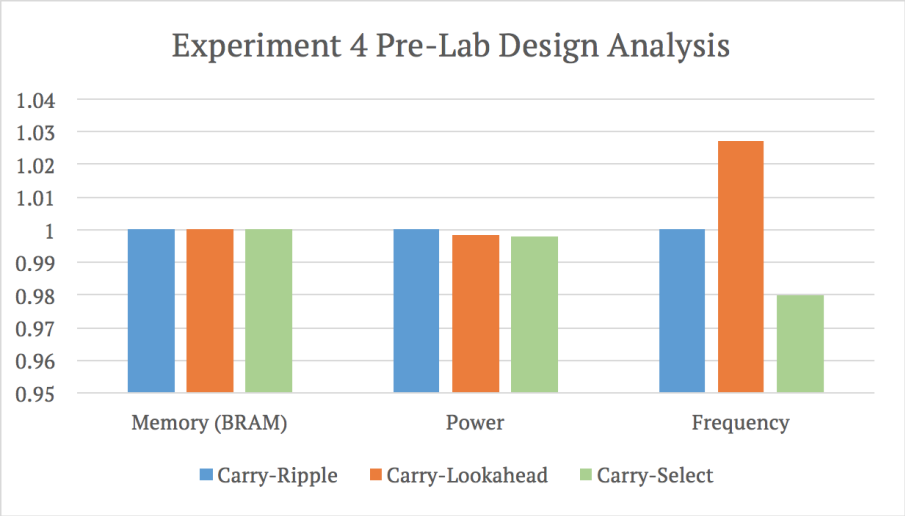

Fig. 3: Pre-Lab Adder Design Analysis (Area, Power, Frequency)