ECE385 Experiment #6

Eric Meyers, Ryan Helsdingen

Section ABG; TAs: Ben Delay, Shuo Liu

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emeyer7, helsdin2

I. Introduction

The purpose of this lab is to create a very primitive processing unit designed around the Little Computer 3 (LC3) that was explored during previous ECE curriculum. This will be referred to the SLC3 Processing Unit throughout this lab. The SLC3 is a condensed version of the LC3 that allows user interfacing through memory-mapped I/O on board the Altera Cyclone IV SRAM Module, along with switches and LED indicators to show the user the status of the data within registers of the SLC3.

II. Description of Circuit

The circuit consists of several modules specifically the high level SLC3 module, the register file, the datapath, the Instruction Decoder/Sequencer Unit (IDSU), the Arithmetic and Logic Unit (ALU), many 16-bit registers (MAR, MDR, IR, and PC), several multiplexers, and some tristate buffers. The datapath and ISDU (Control) are shown in Figure 1. This Figure directly below this in the same section (Figure 2) is the memory interface of the SLC3.

All of these modules work together with one another to form the top level SLC3. The SLC3 will perform a total of

III. Purpose of Modules

As stated in the previous section there are many modules that work together in this system to form the top level SLC3. The following modules were created:

- 16-bit Register
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16-bit Shift Register
2-to-1 Multiplexer
-created with 3 bit version too **4-to-1 Multiplexer**
16-bit Shift Register
16-bit Shift Register
16-bit Shift Register
16-bit Shift Register
16-bit Shift Register
16-bit Shift Register
16-bit Shift Register

IV. State Diagram

RYAN SECTION - Maybe get done on Thursday?

V. Instruction Sequencer / Decoder

ERIC SECTION - Write on Thursday

VI. Schematic/Block Diagram

RYAN SECTION

VII. Pre-Lab Simulation Waveforms

The Pre-Lab Simulation Waveforms can be found on Figure **??** in ”Section XI: Figures”. Finish on Sunday

VIII. Design Statistics

ERIC SECTION

IX. Post Lab

RYAN SECTION - Answer Questions

1.) What is MEM2IO used for, i.e. what is its main function?

2.) What is the difference between BR and JMP instructions?

X. Conclusion

RYAN SECTION

XI. Figures

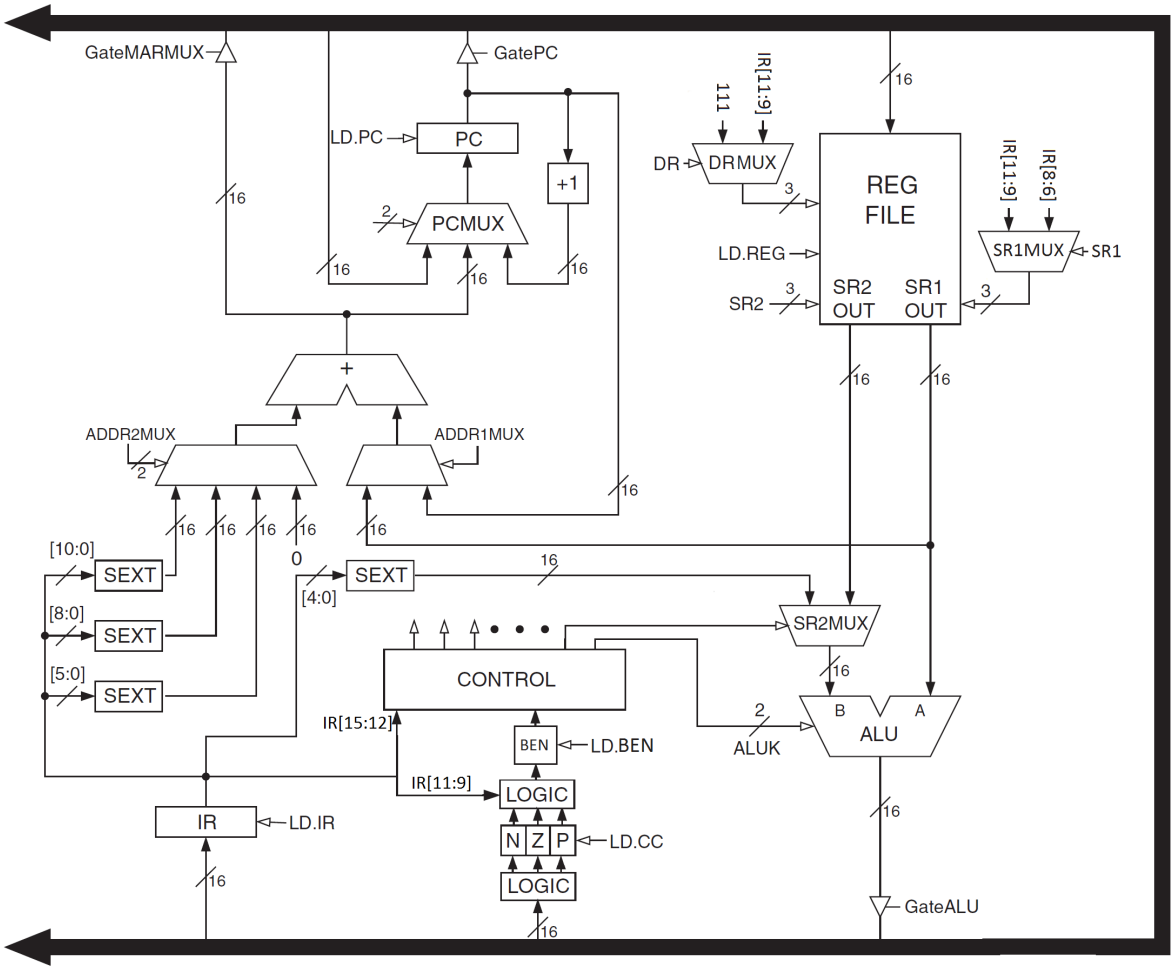

Fig. 1: SLC3 CPU

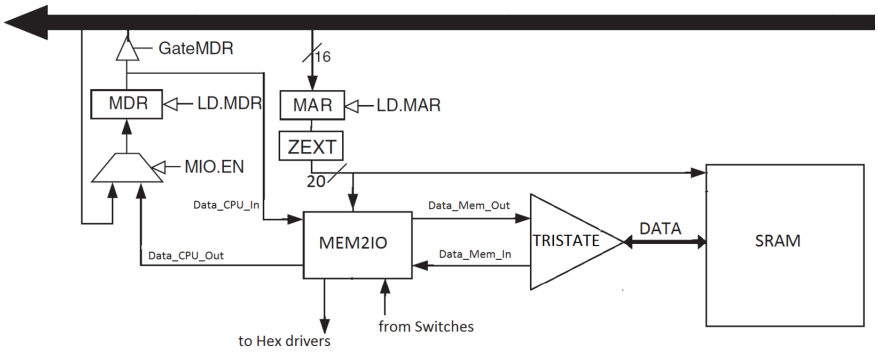

Fig. 2: Memory, MAR, MDR, Mem2IO Configuration