ECE385 Experiment #6

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I. Introduction

The purpose of this lab is to create a very primitive processing unit designed around the Little Computer 3 (LC3) that was explored during previous ECE curriculum. This will be referred to the SLC3 Processing Unit throughout this lab. The SLC3 is a condensed version of the LC3 that allows user interfacing through memory-mapped I/O on board the Altera Cyclone IV SRAM Module, along with switches and LED indicators to show the user the status of the data within registers of the SLC3.

II. Description of Circuit

The circuit consists of several modules specifically the high level SLC3 module, the register file, the datapath, the Instruction Decoder/Sequencer Unit (IDSU), the Arithmetic and Logic Unit (ALU), many 16-bit registers (MAR, MDR, IR, and PC), several multiplexers, and some tristate buffers. The datapath and ISDU (Control) are shown in Figure 1. This Figure directly below this in the same section (Figure 2) is the memory interface of the SLC3.

All of these modules work together with one another to form the top level SLC3. The SLC3 will perform a total of

TODO

III. Purpose of Modules

As stated in the previous section there are many modules that work together in this system to form the top level SLC3. The following modules were created:

16-bit Shift Register

These modules are 16 inputs and 16 outputs with a load_enable line that determines if the data-in is sent to the data-out. The Instruction Register, Memory Address Register, Memory Data Register, Program Counter Register, and Register File will all be utilizing this module.

Multiplexers

A 16-bit 2-to-1 MUX will be used for the ADDR1MUX and the SR2MUX. A 3-bit 2-to-1 MUX will be used for the DRMUX and the SR1MUX.

A 16-bit 4-to-1 MUX will be used for the ADDR2MUX only.

A 16-bit 3-to-1 MUX will be used for the PCMUX. This will take inputs of the databus, the 16-bit adder output, and the PC+1.

Instruction Sequencer and Decoder

This module will contain the state machine for the entire SLC3. It will have the ability to implement 11 states and cycle through all of them in a cyclic fashion.

NZP

TODO

Datapath

TODO

Arthmetic and Logic Unit

TODO

SEXT/ZEXT

TODO

Register File

TODO

16-bit Adder

TODO

Tristate Buffer

TODO

Tristate
TODO

Mem2IO
TODO

IV. State Diagram

RYAN SECTION

V. Instruction Sequencer / Decoder

ERIC SECTION

VI. Schematic/Block Diagram

RYAN SECTION

The Schematic / Block Diagrams can be found on Figure **??** in ”Section XI: Figures”.

VII. Pre-Lab Simulation Waveforms

The Pre-Lab Simulation Waveforms can be found on Figure **??** in ”Section XI: Figures”.

VIII. Design Statistics

ERIC SECTION

IX. Post Lab

RYAN SECTION - Answer Questions

1.) What is MEM2IO used for, i.e. what is its main function?

2.) What is the difference between BR and JMP instructions?

X. Conclusion

RYAN SECTION

XI. Figures

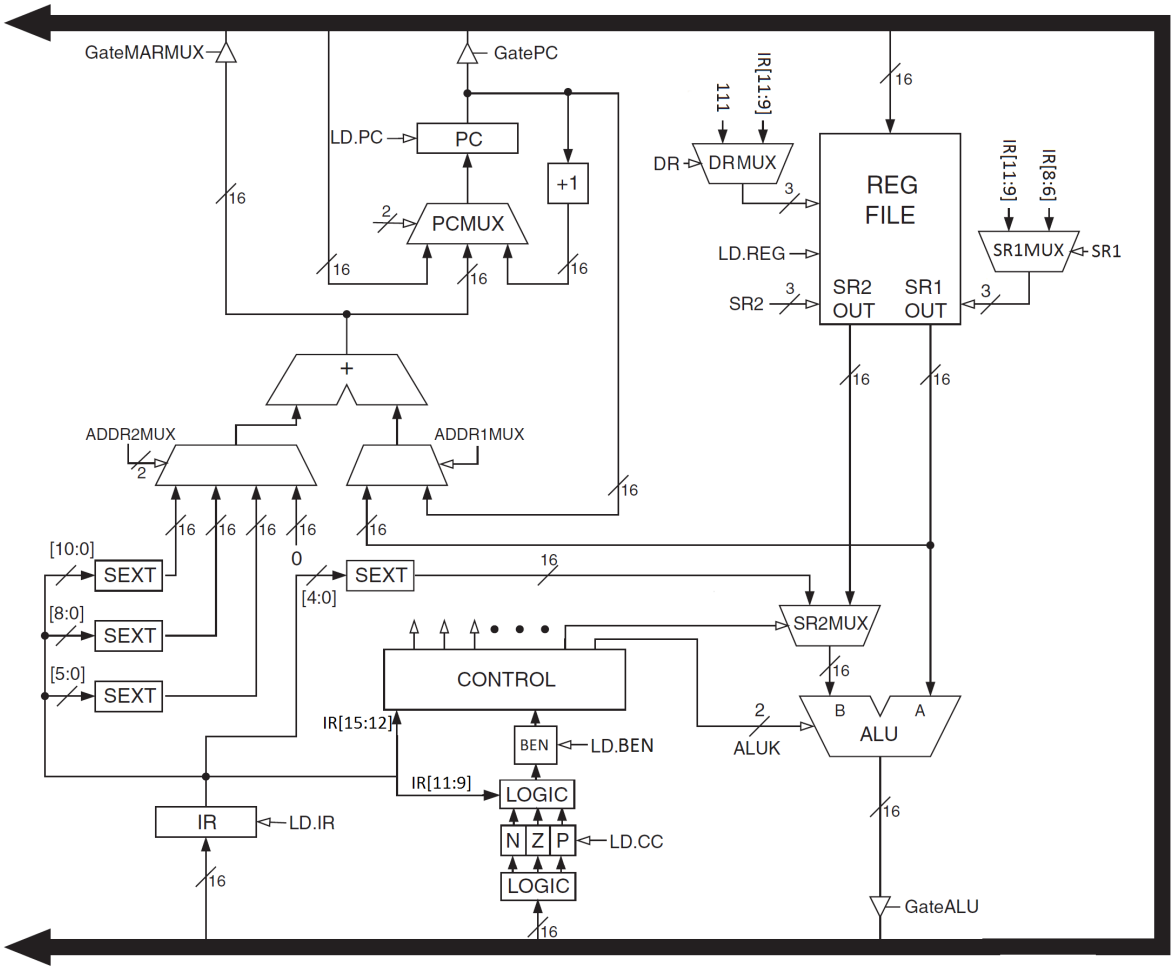

Fig. 1: SLC3 CPU

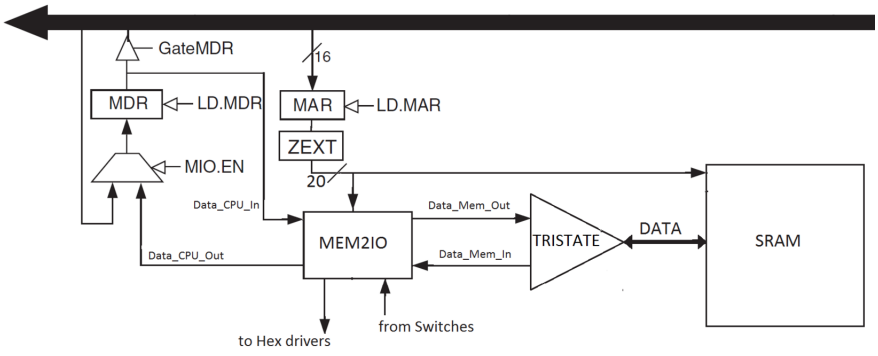

Fig. 2: Memory, MAR, MDR, Mem2IO Configuration