ECE385 Experiment #6

Eric Meyers, Ryan Helsdingen

Section ABG; TAs: Ben Delay, Shuo Liu

March 2nd, 2016

emeyer7, helsdin2

I. Introduction

The purpose of this lab is to create a very primitive processing unit designed around the Little Computer 3 (LC3) that was explored during previous ECE curriculum. This will be referred to the SLC3 Processing Unit throughout this lab. The SLC3 is a condensed version of the LC3 that allows user interfacing through memory-mapped I/O on board the Altera Cyclone IV SRAM Module, along with switches and LED indicators to show the user the status of the data within registers of the SLC3.

II. Description of Circuit

ERIC SECTION

III. Purpose of Modules

E

IV. State Diagram

RYAN SECTION?

V. Instruction Sequencer / Decoder

ERIC SECTION

VI. Schematic/Block Diagram

ERIC SECTION

VII. Pre-Lab Simulation Waveforms

ERIC SECTION

VIII. Design Statistics

ERIC SECTION

IX. Post Lab

RYAN SECTION

X. Conclusion

ERIC SECTION

XI. Figures