

ECE385 Experiment #4

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I. INTRODUCTION

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II. SCHEMATIC OF LOGIC PROCESSOR

Please refer to Figure 1 in "Section XI: Figures" to view the Schematic of the 8-bit Logic Processor designed in the Pre-Lab of this Experiment.

III. DESIGN SIMULATIONS OF LOGIC PROCESSOR

Please refer to Figure 2 in "Section XI: Figures" to view the Annotated RTL Simulation Output of the 8-bit Logic Processor designed in the Pre-Lab of this Experiment.

IV. WRITTEN DESCRIPTION OF ADDER CIRCUIT

V. PURPOSE OF MODULES

VI. STATE MACHINE

VII. SCHEMATIC BLOCK DIAGRAMS

VIII. DESIGN ANALYSIS COMPARISON

IX. POST-LAB

X. CONCLUSION

XI. FIGURES

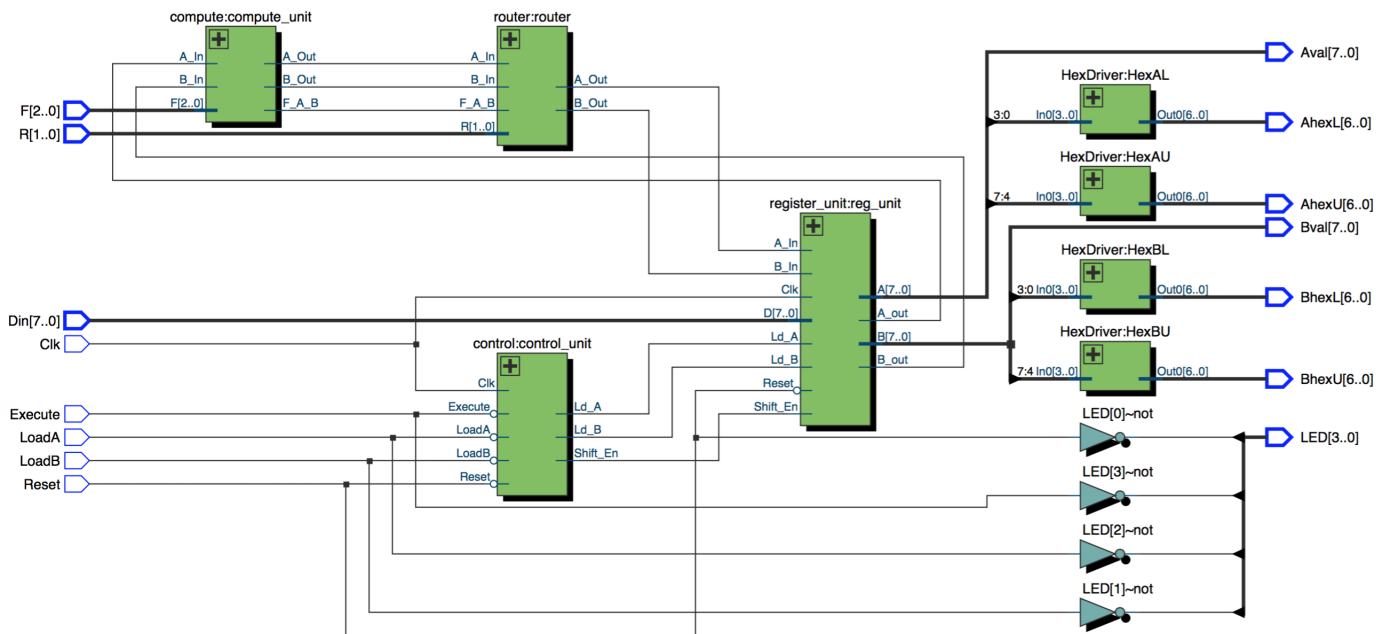


Fig. 1: Serial Logic Processor Schematic

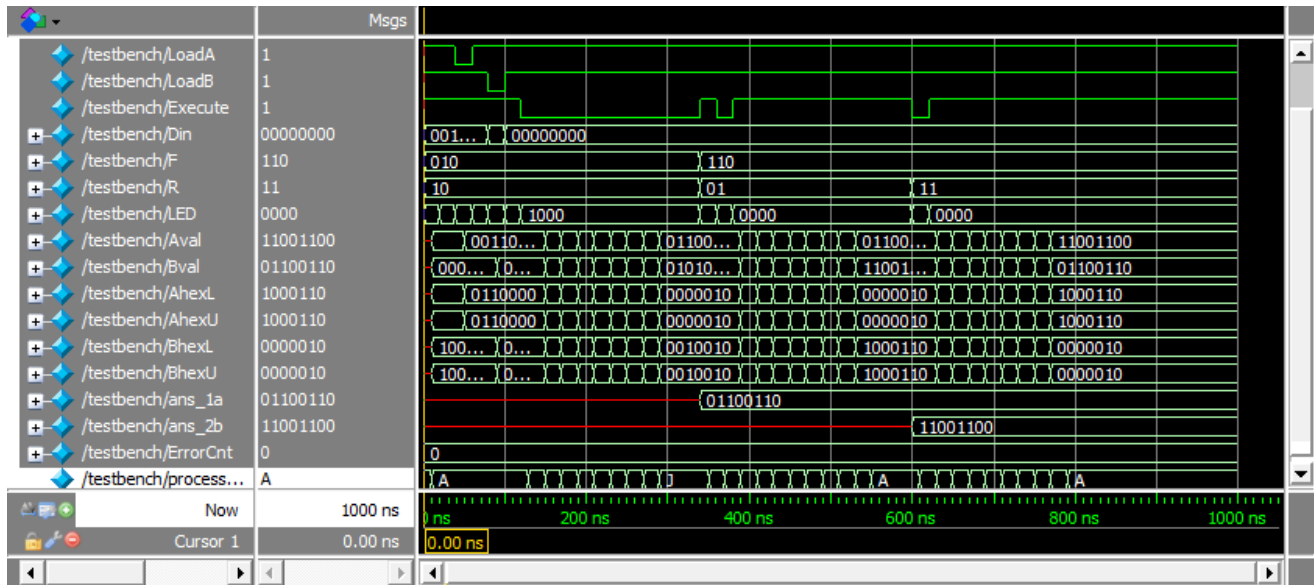


Fig. 2: Serial Logic Processor RTL Simulation Output