ECE385 Experiment #4

Eric Meyers, Ryan Helsdingen

Section ABG; TAs: Ben Delay, Shuo Liu

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emeyer7, helsdin2

I. Introduction

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II. Schematic of Logic Processor

Please refer to Figure 4 in "Section XI: Figures" to view the Schematic of the 8-bit Logic Processor designed in the Pre-Lab of this Experiment.

III. Design Simulations of Logic Processor

Please refer to Figure 5 in "Section XI: Figures" to view the Annotated RTL Simulation Output of the 8-bit Logic Processor designed in the Pre-Lab of this Experiment.

IV. Written Description of Adder Circuit

RYAN SECTION

V. Purpose of Modules

RYAN SECTION

VI. State Machine

ERIC SECTION

VII. Schematic Block Diagrams

VIII. Design Analysis Comparison

The following table displays the values the team received upon analyzing the metrics requested in the pre-lab.

Metric	Ripple	Lookahead	Select
Memory(BRAM)	0	0	0
Frequency (MHz)	62.81	64.526	61.55
Power (mW)	156.65	156.39	156.30

The following figure

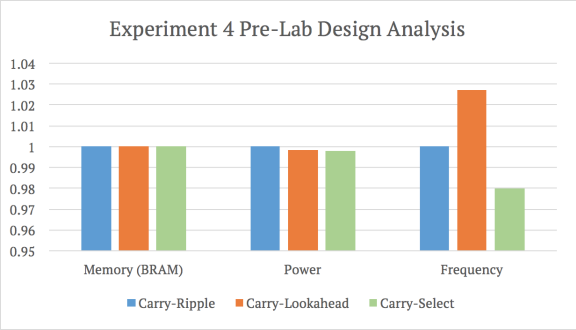

Fig. 1: Area, Power, Frequency Comparison

IX. Post-Lab

1) Compare the usage of LUT, Memory, and Flip-Flop of your bit-serial logic processor exercise in the IQT with your TTL design in Lab 3. Make an educated guess of the usage of these resources for TTL assuming the processor is extended to 8-bit. Which design is better, and why?

Answer: The System Verilog design used in Lab 4 clearly dominates the total usage of Logic Elements in Lab 3 almost by a factor of three. This is because _____.

8-bit Processor Comparison

	Lab4 - System Verilog	Lab3 - TTL Hardware
LUT (#)	67	186
Memory (#)	0	0
FlipFlop (#)	0	3

Fig. 2: Processor Area Comparison

2) For the adders, refer to the Design Resources and Statistics in IQT.30-32 and complete the following design statistics table for each adder. This is more comprehensive than the above design analysis and is required for every SystemVerilog circuit.

Adder Comparison

	Ripple Adder	Lookahead Adder	Select Adder
LUT (#)	114	114	114
DSP (#)	0	0	0
Memory (#)	0	0	0
Flip-Flop (#)	6	5	6
Frequency (MHz)	62.81	64.526	61.55
Static Power (mW)	98.55	98.55	98.55
Dynamic Power (mW)	3.67	3.39	3.28
Total Power (mW)	156.65	156.39	156.3

Fig. 3: Processor Area Comparison

X. Conclusion

Overall, the team successfully demonstrated all three different adder designs for full credit. A

ERIC SECTION

XI. Figures

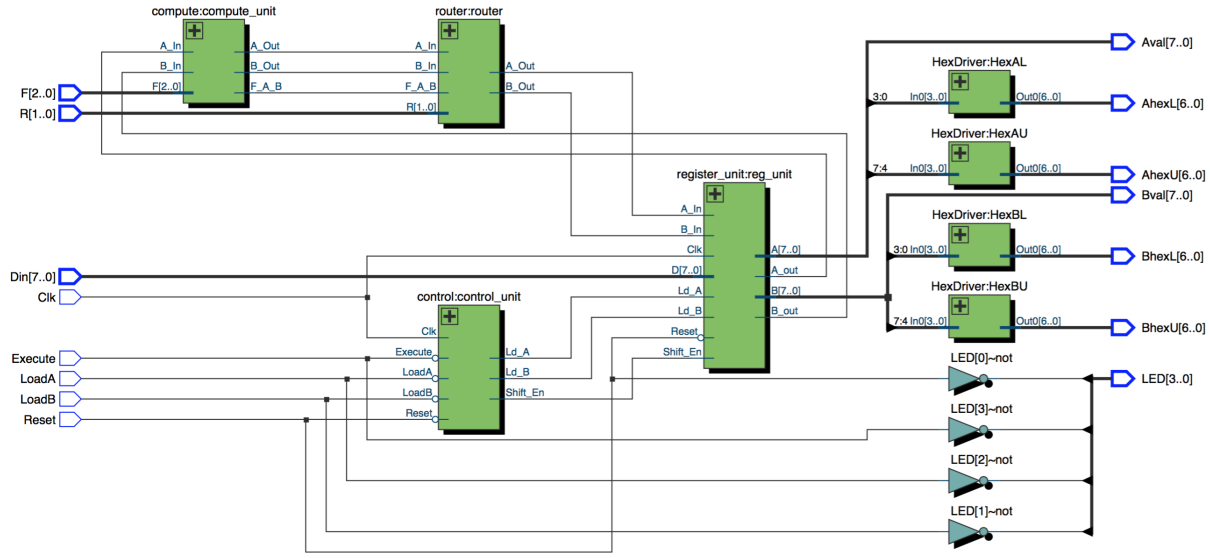

Fig. 4: Serial Logic Processor Schematic

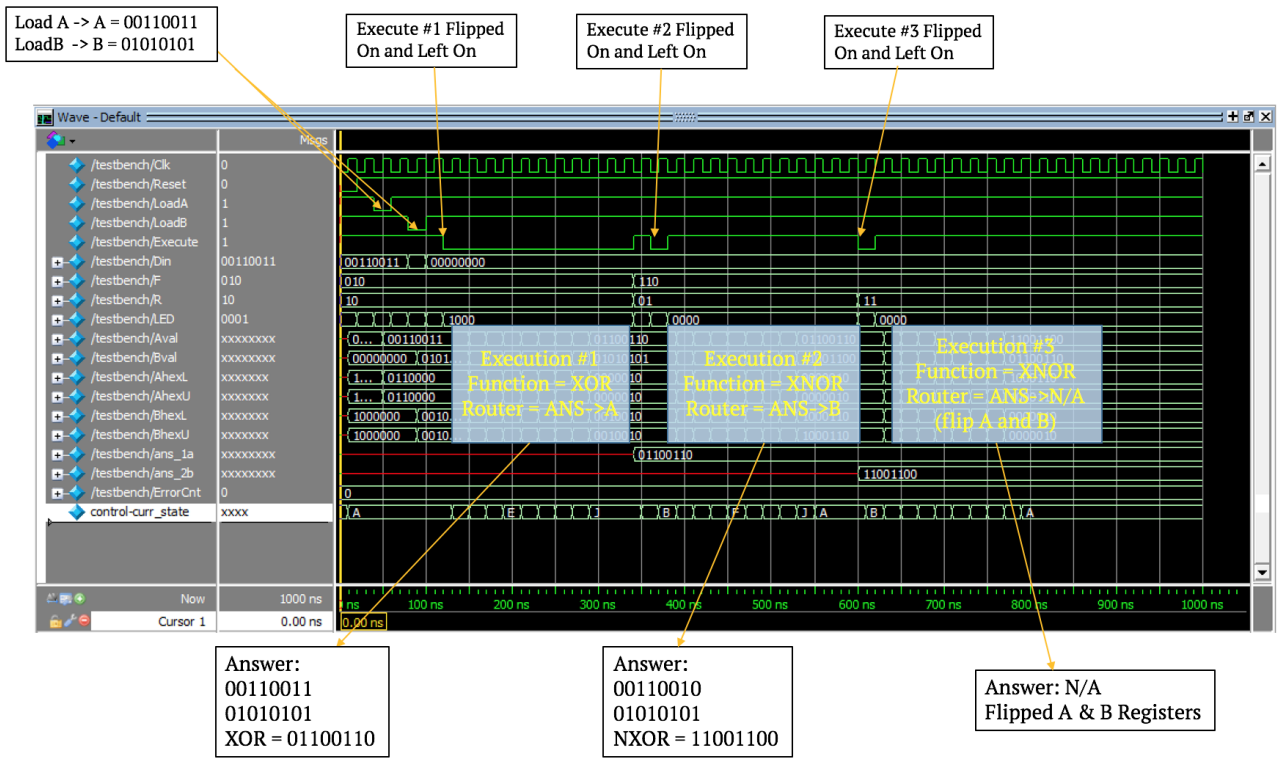

Fig. 5: Serial Logic Processor RTL Simulation Output

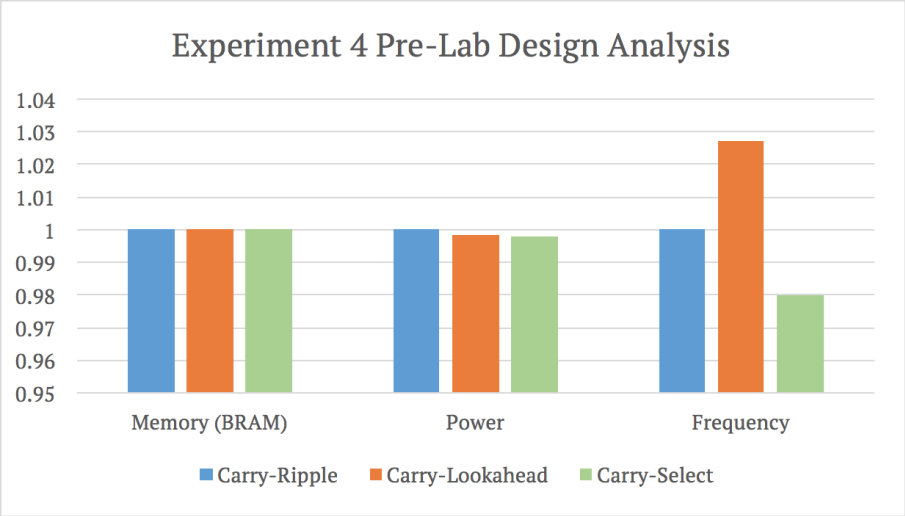

Fig. 6: Pre-Lab Adder Design Analysis (Area, Power, Frequency)