ABSTRACT

OPTIMIZATION OF FILM MORPHOLOGY FOR THE PERFORMANCE OF

ORGANIC THIN FILM SOLAR CELLS

By

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May 2013

The power conversion efficiency of organic thin film solar cells must be improved before they can become commercially competitive alternatives to silicon-based photovoltaics. Exciton diffusion and charge carrier migration in organic films are strongly influenced by film morphology, which can be controlled by the substrate temperature during film growth. Zinc-phthalocyanine/buckminsterfullerene bilayer film devices are fabricated with substrate temperatures between $25\,°C$ and $224\,°C$ and their solar cell performance is investigated here. The device open-circuit voltage, efficiency, and fill factor all exhibit peaks when films are grown at temperatures between $160\,°C$ and $180\,°C$, which is likely a result of both the increase in shunt resistance and reduction in undesirable back diode effects which occur between $100\,°C$ and $180\,°C$. The device performance can also be attributed to changes in the film crystallite size, roughness, and abundance of pinholes, as well as the occurrence of crystalline phase transitions which occur in both zinc-phthalocyanine and buckminsterfullerene between $150\,°C$ and $200\,°C$. The unusually high open-circuit voltage (1.2 V), low short-circuit current density (0.03 mA/cm^2), and low device efficiency (0.04%) reported here are reminiscent of single layer phthalocyanine-based Schottky solar cells, which suggests that pinholes in bilayer film devices can effectively lead to the formation of Schottky diodes.

OPTIMIZATION OF FILM MORPHOLOGY FOR THE PERFORMANCE OF

ORGANIC THIN FILM SOLAR CELLS

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CHAPTER 1

INTRODUCTION

The world's need for inexpensive renewable energy is presented as the primary motivation for investigating the characteristics of organic photovoltaics. A brief history of organic solar cells is provided, as well as a model for describing the main processes underlying the operation of organic photovoltaics. Finally, the significance of thin film morphology in regards to organic solar cell performance is discussed.

World Energy Demand

World energy demand is growing at an unprecedented rate. It is expected that by the year 2050, annual world energy consumption will be twice as high as it was in 2006 [1]. Over 85% of the world's energy is currently produced using fossil fuels (coal, crude oil, and natural gas) [2]. The widespread combustion of fossil fuels for energy generation is responsible for increases in the concentration of carbon dioxide in Earth's atmosphere, which may cause rapid global climate changes that are detrimental to plant and animal life [3]. Securing sustainable sources of energy is one of the biggest challenges that humans will face in the coming decades, as virtually all of the easily accessible fossil fuels on the planet may be depleted by the year 2100 [4, 5].

As fossil fuel reserves dwindle, the cost of the energy they produce will increase, making the development and implementation of alternative energy sources more attractive [6]. The beginning of this trend is already apparent; worldwide, government-funded subsidies for renewable energy increased from $39 billion in 2007 to $66 billion in 2010 [7]. Although $\sim$13% of the world's energy is currently produced by nuclear power plants [1], an increase in the global production of nuclear power is limited

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by sociopolitical constraints because of the hazardous radioactive waste produced by reactors and the susceptibility of nuclear power facilities to catastrophic accidents. The problems associated with nuclear power generation dictate that the implementation of alternative energy sources will be needed if the world's energy demand is to be met without the future availability of fossil fuels.

The harvesting of sunlight as an energy source has a number of advantages over the use of other renewable energy technologies like wind turbines and hydroelectric systems. Solar irradiance provides more power to the surface of the earth each day than the entire world consumes every year [8]. Solar energy can be harnessed by stationary devices, which reduces the amount of maintenance required to keep solar collection systems operational. Photovoltaic devices can be incorporated into the architecture of buildings, making them more aesthetically desirable than wind turbines, and are not vulnerable to catastrophic failure like hydroelectric dams or nuclear power generators. More importantly, solar energy is most abundant in Africa, Asia, and South America, areas where the energy use by developing countries has risen over 400% in the last 30 years, and where future energy demand is estimated to be the highest in the world [9, 10]. The advantages to using sunlight as an energy source have caused world market shares in solar energy technologies to increase nearly ten-fold in the last 20 years [11].

The most common way to harvest solar energy is through the use of photovoltaic (PV) cells, or solar cells, devices traditionally fabricated using inorganic semiconductors like silicon (Si). Over 95% of commercially available PV cells are currently Si-based, primarily because of its resistance to degradation and its relatively high power conversion efficiency ($\sim$15%-25%) [11]. The primary factor that currently limits the large-scale fabrication and implementation of PV cell arrays is the high cost and energy expenditure associated with the manufacture of Si-based PV modules [12]. The high demand for Si in integrated circuits and other semiconductor devices has caused the

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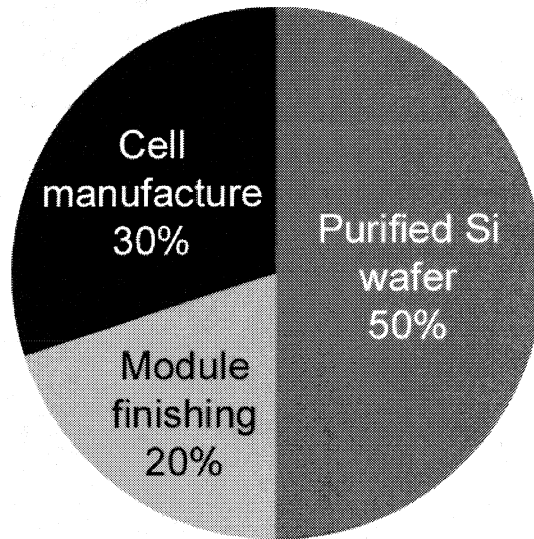
FIGURE 1. Cost of a Si-based solar cell module. The cost of purified Si wafers account for roughly half the cost of a Si-based module [17]. The high cost of Si-based devices currently limits the widespread implementation of solar energy generation. (Source: Harriet Kung, U.S. Department of Energy, 2005)

price of Si to more than double between 1977 and 2009 [11, 13]. The processed Si wafers themselves account for roughly half of the total PV module cost (see figure 1) because of the enormous energy requirements needed for Si crystal growth, high-temperature (up to $900\,^{\circ}C$) purification and doping, and wafer cutting and cleaning. The substantial amounts of water and energy that these processes require result in extremely expensive power generation ($3.50 - 4.50$ \$/W) [9, 14, 15, 17].

Interest in inexpensive alternatives to traditional Si-based PVs has grown as the cost of Si continues to rise and Si-based PV technology approaches its theoretical efficiency limit ($\sim$30%) [16]. PV devices made of low-cost materials are especially attractive because of their potential implementation in developing countries such as China and India, which are currently responsible for the largest growth in world energy demand. The development of efficient, inexpensive PV technology would increase the

availability of electricity in developing countries while enabling solar power to become a financially competitive source of energy in developed countries.

Thin Film Organic Photovoltaics

One inexpensive (1 − 3 $/W) alternative to Si-based PVs is a thin film (< 1 μm) device based on organic semiconductors [18]. Organic photovoltaics (OPVs) are attracting increasing attention because of their low production costs, ease in manufacturing, light weight, and ability to be fabricated on flexible substrates [11]. Although the power conversion efficiency of OPVs is currently too low (<15%) to make them commercially competitive with existing inorganic devices, low fabrication costs give OPVs a distinct advantage over Si-based systems [15].

The properties of organic semiconductors strongly influence OPV device design. Average charge carrier mobilities are lower and exciton diffusion lengths are shorter in organic semiconductors (∼5-15 nm) than diffusion lengths in inorganic semiconductors (∼1 μm). The low mobilities are primarily caused by the small crystallite sizes (< 1 μm) and high disorder of crystallite orientations in organic films. Low charge carrier mobilities dictate that OPV device thicknesses must be limited to the 100 nm range to ensure sufficient charge migration [19, 20, 21]. The high absorption coefficients ($\geq 10^5$ cm^{-1}) of many organic semiconductors allow for ∼100% absorption even with device thicknesses < 200 nm [22, 23]. The strong absorption and low charge carrier mobility in organic semiconductors make thin film device structures ideal for efficient OPV design. Thin film OPVs are the best-studied OPV devices today because of their potential to become competitive with Si-based devices in the near future [20].

The first OPV device to achieve a power conversion efficiency of ∼1% was reported by Tang in 1986 [24]. Previously, most experimental OPV devices consisted of a single organic semiconducting thin film sandwiched between two disparate electrodes [8]. Tang showed that device efficiency improves when a second organic

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ZnPc

C$_{60}$
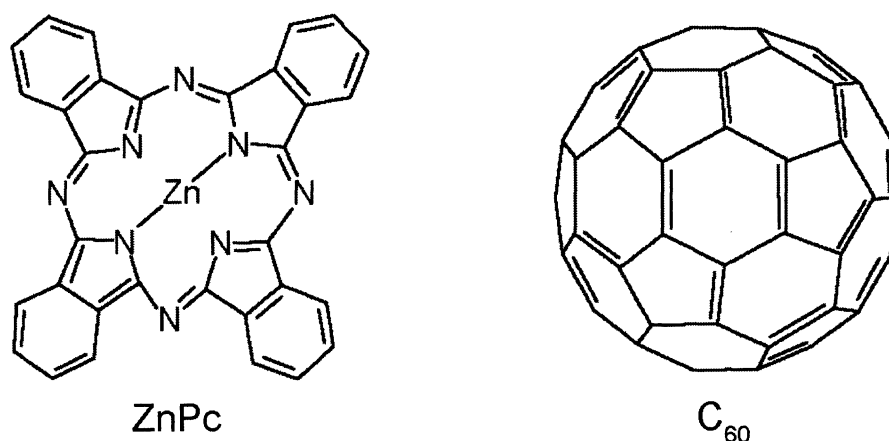
FIGURE 2. ZnPc and C$_{60}$ molecules. The planar metallophthalocyanine molecule is an intrinsic p-type organic semiconductor, popular for use in OPVs because of its strong absorption. Shown on the left is zinc-phthalocyanine (ZnPc). The spherical molecule buckminsterfullerene (C$_{60}$) is an intrinsic n-type organic semiconductor. A well-studied bilayer OPV device structure consists of a heterojunction formed by thin films of ZnPc and C$_{60}$.

semiconductor is introduced, so that a bilayer heterojunction is formed between an electron donor (p-type) and an electron acceptor (n-type) material. It is the donor-acceptor (D-A) interface that is responsible for the dominant photovoltaic properties of the device, not the difference in work functions of the electrodes [24].

The organic semiconductor copper phthalocyanine (CuPc) was used as the electron donor in Tang's device [24]. Metallophthalocyanine (C$_{32}$H$_{16}$N$_8$M, where M is the metal) is a planar organic molecule with one metallic atom in the center, as shown in figure 2. Phthalocyanines (Pcs) are commonly used as strong blue-green pigments in industrial applications. Their behavior as intrinsic p-type semiconductors and their strong absorption of visible light make Pcs some of the most popular materials for use in OPVs today [25].
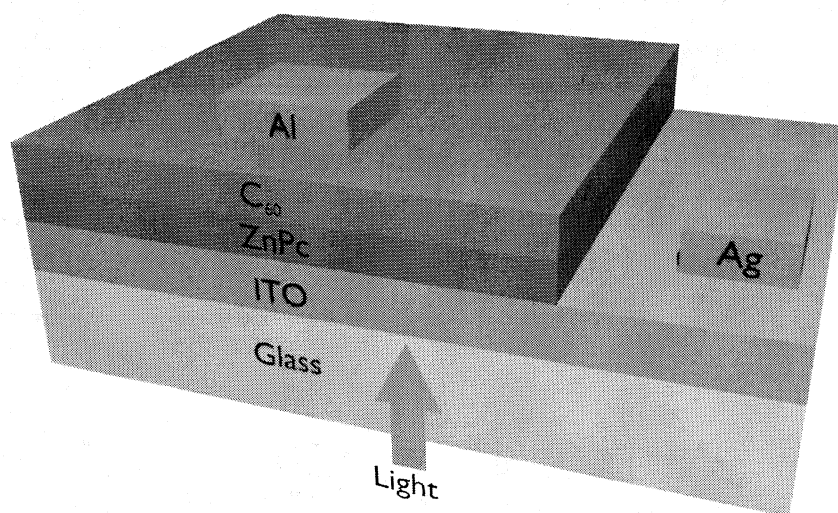
FIGURE 3. Architecture of a bilayer heterojunction OPV device. A well-studied bilayer heterojunction device structure consists of organic thin films of ZnPc and C_{60} sandwiched between the transparent electrode ITO and an aluminum electrode.

Since Tang's findings in 1986, major improvements have been reported in the power conversion efficiencies of bilayer heterojunction OPVs, with some devices achieving efficiencies as high as 3% [20]. One well-studied device structure consists of a bilayer heterojunction between thin films of p-type zinc-phthalocyanine (ZnPc) and n-type buckminsterfullerene (C_{60}) [25, 26]. The organic films are sandwiched between two electrodes, usually the transparent conductor indium tin oxide (ITO) and aluminum (Al), as shown in figure 3. ITO thin films are commonly used as transparent electrodes because of their high reflectivity of infrared radiation and low sheet resistance ($< 100 \, \Omega$). It has been shown that of all the common MPcs, the best device performance is realized when ZnPc is used as an electron donor in conjunction with C_{60} as an electron acceptor. This is due to the the strong absorption of visible light by ZnPc and the difference in energies between the valence and conduction band orbitals in ZnPc and C_{60}, as discussed in the next section [25].

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Although the ZnPc/C_{60} bilayer heterojunction device structure has been studied extensively, the bulk heterojunction system has attracted even more attention because it has achieved efficiencies of as high as 6% [25]. In a bulk heterojunction structure, the active layer of the device consists of a mixed film of both donor and acceptor materials. The effect of the film morphology on the operation of bulk heterojunction devices has been studied in detail [22, 26], but much less is known about how morphology influences the performance of bilayer systems. The purpose of this study is to determine how thin film morphology, especially the size of crystallites in the films, can affect the performance of bilayer heterojunction solar cells. The influence of film morphology on bilayer device performance is compared to results from similar studies on bulk heterojunction devices in chapter 3.

Organic Bilayer Heterojunction Solar Cell Operation

The working principles behind the operation of a bilayer heterojunction OPV device will be described in the following sections. These principles are best illustrated in terms of the energy differences between the molecular orbitals of the donor and acceptor materials and the creation, diffusion, and dissociation of excitons, as outlined in figure 4. The power conversion efficiency η of a bilayer OPV device can be characterized in terms of the efficiencies of each of its internal processes: the efficiency of exciton creation η_{EC}, the efficiency of exciton diffusion η_{ED}, the efficiency of the charge transfer reaction η_{CT} at the D-A interface, and the efficiency of charge carrier collection η_{CC} at the electrodes [23]. The overall device efficiency can be summarized as

$$\eta = \eta_{EC} \times \eta_{ED} \times \eta_{CT} \times \eta_{CC}.$$

Exciton Creation

In a molecule in its ground state, electrons with the most energy are located in the highest occupied molecular orbital (HOMO). If an electron in the HOMO is excited by an incident photon of sufficient energy, it will be promoted to the lowest unoccupied
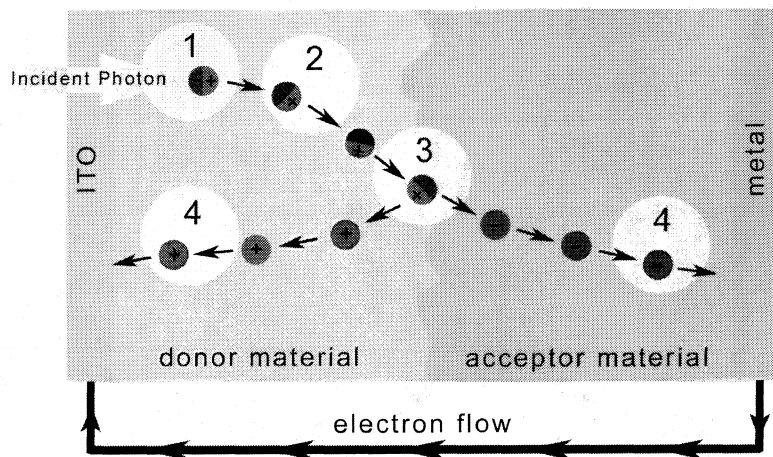
FIGURE 4. Exciton creation, diffusion, and dissociation. The operation of bilayer heterojunction OPVs can be described in a four step process. (1) Incident light is absorbed by an electron donor molecule, resulting in the creation of an exciton. (2) The exciton diffuses to the D-A interface. (3) The difference in energies of the molecular orbitals at the D-A interface causes dissociation of the exciton into its constituent free charge carriers. (4) Charge carriers migrate to opposite electrodes and flow through an external load. Alternative processes, such as electron-hole recombination and the diffusion of excitons to electrodes, can lead to decreases in device efficiency.

molecular orbital (LUMO). The photoexcitation of an electron from the HOMO to the LUMO level effectively leaves behind a hole in the HOMO level. The hole can be regarded as a positive charge carrier that may become bound to the excited electron by electrostatic attraction. The bound state between the electron and hole, called an exciton, can be thought of as a quasiparticle which can transfer energy without carrying a net charge.

In the ground state of a ZnPc molecule, all the metal d-orbitals are filled and the HOMO is the ligand π orbital a_{1u} [25]. An electron in the HOMO can be promoted to the LUMO by photoexcitation, which is the ligand π^* orbital $2e_g$. The electron excitation $a_{1u} \rightarrow 2e_g$ requires ~1.8 eV [26]. Energies of ~1.8 eV are carried by photons of wavelength 689 nm, which lies inside the strong optical absorption region of ZnPc, as shown in figure 5. The strong absorption of ZnPc at wavelengths between 600 and
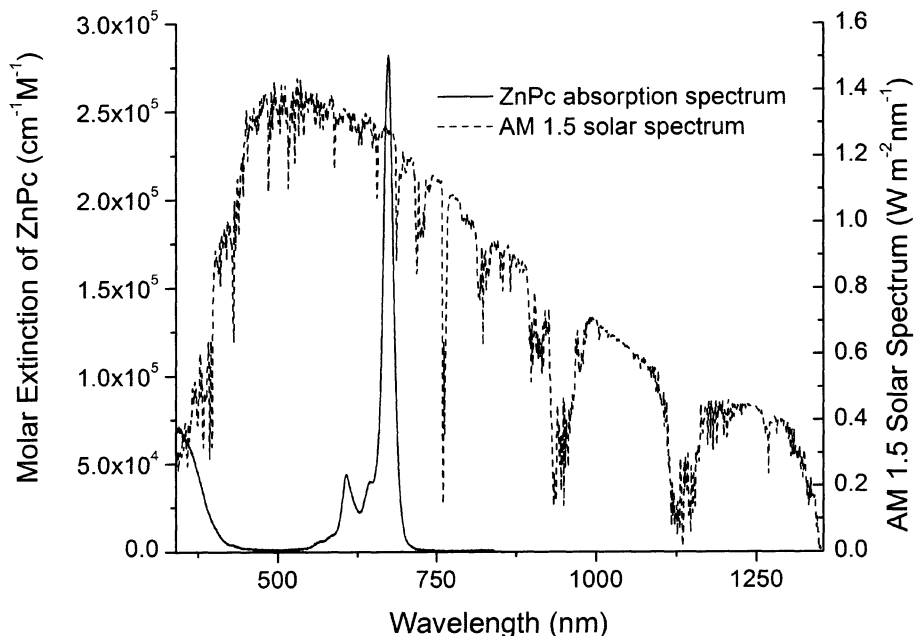
FIGURE 5. Absorption spectrum of ZnPc. ZnPc strongly absorbs light in the 600 − 700 nm wavelength range, which corresponds to a region of high terrestrial solar irradiance [38, 39]. This makes ZnPc an ideal material for use in thin film OPVs.

700 nm results in efficient exciton creation ($\eta_{EC} \approx 100\%$) in films with thicknesses over 100 nm [23].

Exciton Diffusion

Although exciton generation is critical for efficient device operation, excitons are electrically neutral and thus cannot be used to produce electrical power. Excitons must dissociate into their constituent electrons and holes in order to contribute to the production of photocurrent generated by a device. Typical exciton binding energies E_b in organic semiconductors are between 0.1 and 2.0 eV [23]. The strength of the electric field inside most OPV devices (10^6 V/cm) is insufficient ($\eta_{CT} < 10\%$) to overcome the binding energy and separate electrons from holes. In order to dissociate into free charge carriers, excitons generated inside the donor material must first diffuse to the

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heterojunction between the donor and acceptor materials, where stronger electric fields are present [23].

The diffusion of excitons through organic films is predominantly influenced by the film morphology, or anisotropic accumulation of the semiconductor material, which includes the shapes of crystallites, sizes of crystallites, and intermolecular spacing [19]. The average exciton diffusion length L_D in ZnPc films is $\sim$15 nm [41]. If a ZnPc exciton is generated at a distance greater than L_D away from the heterojunction, then the electron and hole generally recombine, resulting in $\eta_{ED} < 50\%$. The likelihood that an exciton will diffuse to the heterojunction without recombination occurring first is highly dependent on the shape of the heterojunction, as shown in figure 6. As the roughness between two adjacent films increases, the surface area of the interface between them also increases. This effectively reduces the average distance between exciton creation and the D-A interface, which leads to an increase in η_{ED}. When the organic films are very smooth, the interface between them can be modeled as a planar heterojunction. This configuration effectively maximizes the distance between exciton generation and the D-A interface, which can lead to lower η_{ED}. Therefore, the roughness of the organic films is extremely important for efficient exciton diffusion. Film roughness is dependent on the sizes of crystallites in the films, with larger crystallites leading to rougher films [35]. The influence of the crystallite size on bilayer heterojunction OPV performance is the primary focus of this study.

Exciton Dissociation

The exciton dissociation, or charge transfer reaction, occurs when an exciton reaches the D-A interface and is split into its constituent free charge carriers. A heterojunction between an electron donor material with a low ionization potential (IP_D) and an electron acceptor material with a high electron affinity (EA_A) is required at the
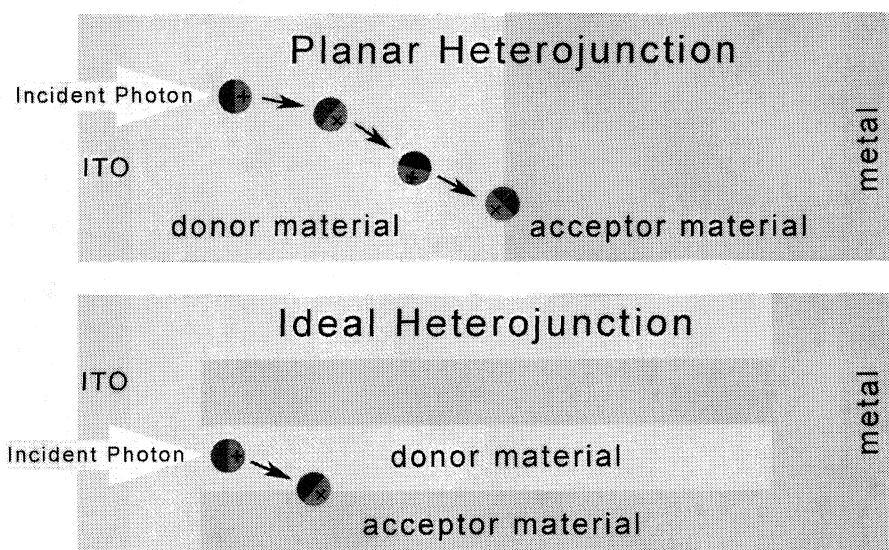
FIGURE 6. Planar and ideal D-A interfaces. The average exciton diffusion length L_D in a ZnPc thin film is ~ 15 nm. To ensure high η_{ED}, exciton generation must occur within a distance L_D from the D-A interface. The heterojunction between two smooth films is planar. This configuration effectively maximizes the average distance between exciton generation and the D-A interface. The interface between two very rough films increases the surface area of the heterojunction, and minimizes the average distance from exciton generation to the heterojunction. This configuration is ideal for high η_{ED}.
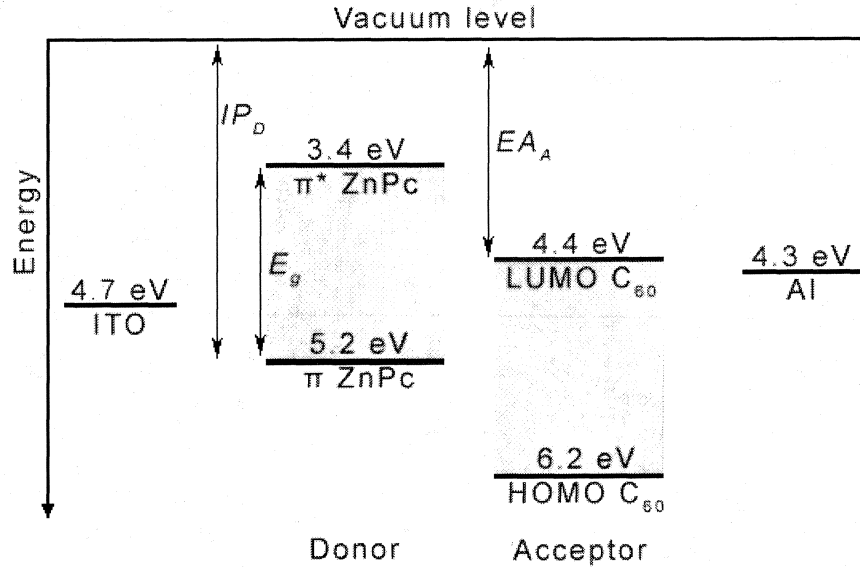
FIGURE 7. Energy levels at the D-A interface. Efficient exciton dissociation occurs at the heterojunction between an electron donor material with a low ionization potential (IP_D) and an electron acceptor material with a high electron affinity (EA_A). The energies of the molecular orbitals in ZnPc and C_{60} make these materials ideal for use in bilayer heterojunction devices [26].

D-A interface for high η_{CT}, as illustrated in figure 7. The high electron affinity of C_{60} ($\sim$4.4 eV) makes it an ideal acceptor material [28].

The energy of an exciton is $E_{ex} = E_g - E_b$, where E_g is the band gap energy between the HOMO and LUMO levels of the material where the exciton is generated, and E_b is the exciton binding energy. If $E_{ex} > IP_D - EA_A$, then it becomes energetically favorable for excitons to dissociate at the D-A interface [23]. The HOMO and LUMO levels of ZnPc and C_{60} are aligned such that $E_{ex} > IP_D - EA_A$ and $\eta_{CT} \approx 100\%$ at the D-A interface [23]. Although it is widely believed that the energy difference between the HOMO of the donor material and the LUMO of the acceptor material is what primarily determines the maximum possible voltage produced by a PV device, there is still some disagreement about the extent to which other factors can influence device
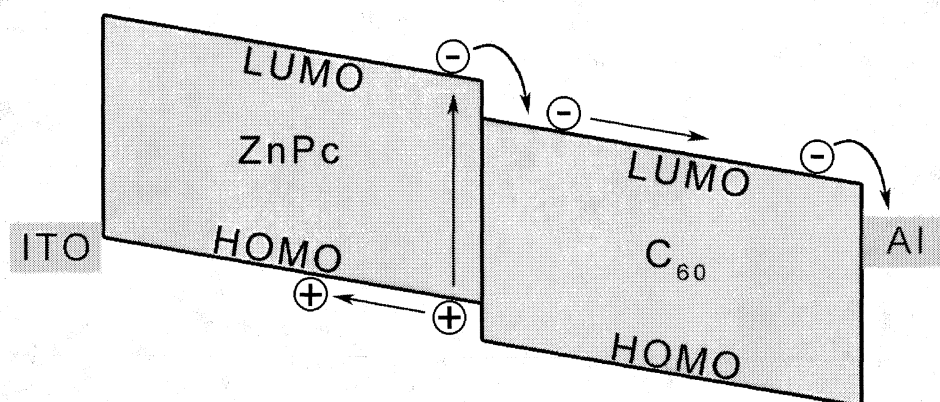
FIGURE 8. Band tilting. When the thin films of organic semiconductors are sandwiched between two disparate electrodes, an electric field arises inside the semiconductors. This field creates tilting of the energy bands and helps to drive free charge carriers to opposite electrodes, where they can flow out through an external load.

voltage [23, 51]. The origin of the open-circuit voltage will be discussed in detail in chapter 3.

Charge Carrier Migration

Free charge carriers produced by exciton dissociation must migrate to opposite electrodes in order to contribute to the photocurrent produced by a PV device. The migration of charge carriers is largely driven by the built-in electric field inside the semiconductor materials [42]. When the donor and acceptor materials are brought in contact with each other and sandwiched between two electrodes to form a circuit, an electric field arises inside the semiconductors. This built-in field gives rise to band tilting of the energy levels of the semiconductor materials, as shown in figure 8. The band-tilting helps drive free charge carriers towards opposite electrodes after exciton dissociation has occurred. The migration of charge carriers is also strongly influenced by film morphology [27]. The effect of film morphology on all aspects of solar cell operation is described in detail in the next section.

Morphology of Organic Thin Films

The electronic and optical properties of organic thin films are strongly influenced by their morphology, or microcrystalline structure, which includes the size and shape of crystallites, the orientation of stacked molecules, and the film surface roughness [35]. Film morphology has been shown to affect nearly all the processes in solar energy conversion, including light absorption, exciton generation, exciton diffusion and dissociation, and the migration of charge carriers to the electrodes [43].

Organic thin films are commonly grown by thermal evaporation, in which the organic material is heated until it sublimes and deposits on a substrate. The temperature of the substrate during the deposition process strongly influences the morphology of the deposited film [35]. During the growth of MPc thin films, van der Waals interactions and the structural anisotropy of the MPc molecule leads to the formation of crystallites, or grains, in which the central metallic atoms of the MPc molecules line up to form chains. The sizes and shapes of the grains can have important consequences for the electronic behavior of the films [25]. Films deposited at room temperature typically contain small circular grains with diameters < 50 nm. As the substrate temperature is increased, the deposited molecules have more energy with which to react to the van der Waals forces. High substrate temperatures result in the formation of longer metal atom chains and more elongated grains, as shown in an atomic force microscope (AFM) image in figure 9. Depending on the temperature of the substrate, the deposited grains can range from a few nm to a few μm in length [35].

The grain size in organic films can affect the performance of OPV devices because it strongly influences the mobility of charge carriers [47]. In order to travel from the D-A interface to electrodes, free charge carriers must migrate through grains, as well as traverse grain boundaries. However, both charge carrier transport and exciton diffusion lengths are limited by trap states located at grain boundaries [27]. A charge
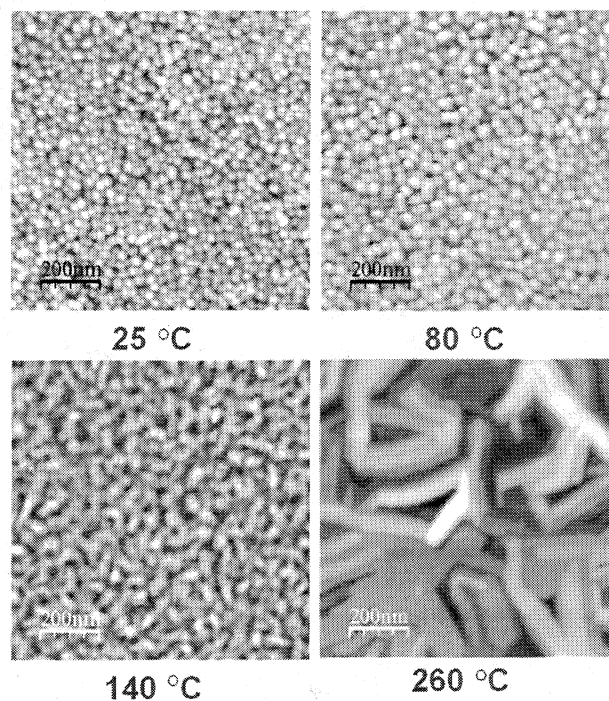
FIGURE 9. Grain size in Pc thin films. The crystallites, or grains, that comprise an MPc thin film become larger and more elongated as the temperature of the substrate is increased. The morphology of organic films can influence nearly every aspect of OPV device performance. Image courtesy of K. P. Gentry [35].

carrier migrating through a film made of large, elongated grains does not encounter as many grain boundaries as one which travels through a film comprised of smaller grains. There is less probability that a charge carrier will fall into a trap state at a grain boundary when larger grains are present. It has been shown that charge carrier mobility in organic films can increase nearly 3-fold when the temperature of the substrate during film deposition is increased from 20 °C to 175 °C [27]. The increase in η_{CC} is largely due to the reduction in the number of grain boundaries that charge carriers must cross during their migration to electrodes.

Film roughness can also affect organic solar cell performance. As MPc films are grown on substrates at temperatures greater than 200 °C, the roughness of films increases dramatically. In fact, the rms surface roughness of films deposited at temperatures from 230 °C to 260 °C (3.1 nm) can be more than twice as high as the roughness of films deposited from 25 °C to 200 °C (1.3 nm) [35]. The heterojunction formed between two rough films has a higher surface area than the heterojunction between two smooth films. The larger area heterojunction reduces the distance that excitons must travel before they can dissociate into free charge carriers. This means that rougher films may give rise to a higher η_{CT} [37, 36].

In addition to grain size and roughness, the orientation of the molecular stacking also changes as MPc is deposited at different temperatures. In ZnPc films, an $\alpha \rightarrow \beta$ phase transition occurs at deposition temperatures between 150 °C and 200 °C [43]. This phase transition causes the distance between the closest zinc atoms in adjacent chains to increase from 12.22 Å (α phase) to 13.31 Å (β phase) [43], as shown in figure 10. The increase in distance between adjacent zinc atom chains can have a strong influence on organic solar cell performance because exciton diffusion is highly dependent on intermolecular spacing [19]. In order to diffuse to adjacent zinc chains in a ZnPc film, an exciton must diffuse roughly 9% farther through β phase crystallites than α phase

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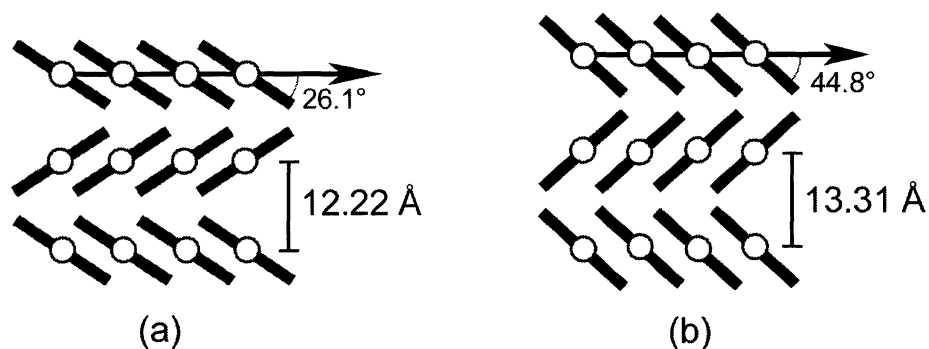
FIGURE 10. ZnPc crystal structure. The ZnPc crystallite structure consists of adjacent chains of zinc atoms. Here, the ZnPc molecules, viewed along their planar axis, are represented by the black rectangles. The zinc atoms are represented by the white circles in the center of the molecules. (a) Adjacent zinc atom chains in the ZnPc α phase are spaced about 12.22 Å apart from each other. At temperatures between 150 °C and 200 °C, ZnPc undergoes an α → β phase transition. This transition leads to the more stable β configuration (b) where the adjacent chain spacing is roughly 13.31 Å. Exciton diffusion is highly dependent on intermolecular spacing, so the increase in chain spacing may cause significant decreases in η_{ED}.

crystallites. The small L_D of ~15 nm in ZnPc films means that an increase in the intermolecular spacing may lead to significant decreases in η_{ED}. The influence of the morphology on solar cell performance will be analyzed in detail in chapter 3.

CHAPTER 2

EXPERIMENT

This chapter describes the process of device preparation, fabrication, testing, and characterization. $ZnPc/C_{60}$ bilayer thin film structures were grown by thermal evaporation at different substrate temperatures. After electrical contacts were applied, the current-voltage (I-V) characteristics of each device were measured. Important operating parameters of the devices were extracted from the I-V curves. The crystalline phases present in the films were determined using X-ray diffraction (XRD).

Materials and Preparation

Glass slides precoated with the transparent conductor ITO (thickness 30-60 nm, sheet resistance 30-60 Ω, nominal transmittance > 80%, and surface roughness < 0.15 μm / 20 mm) were obtained from SPI Supplies[1] and used as substrates for film growth. Each substrate was precoated with two silver busbars (resistivity < 0.5 $\Omega \cdot cm$) for use as electrical contacts. Before use, the substrates were carefully cleaned with 99% pure isopropanol and blown dry with nitrogen gas. An aluminum foil shadow mask was used to cover ~25% of each substrate to prevent organic films from growing on the silver busbars during the deposition process.

ZnPc (5 grams, 97% pure) was obtained from Sigma-Aldrich[2] and C_{60} (5 grams, 99.5% pure) was obtained from MTR Ltd[3]. Further purification of the ZnPc was carried

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[1]569 East Gay St., West Chester, PA 19380, USA

[2]3050 Spruce St., St. Louis, MO 63103, USA

[3]6108 Whiteford Dr., Cleveland, OH 44143, USA

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out by thermal gradient sublimation inside a tube furnace at a maximum temperature of 440 °C. After 100 hours, the purified ZnPc was harvested from the furnace. All organic materials and substrates were stored in a UV-blocking desiccator to prevent degradation and contamination.

Si wafers (diameter 100 mm, thickness 250 μm, resistivity < 0.1 Ω·cm) were purchased from Virginia Semiconductor[4] and cut into 1×2 cm rectangles for XRD studies. Prior to use, the Si wafers were cleaned in an ultrasonic bath of acetone for 5 minutes to remove adsorbed contaminants. The Si was then cleaned in an ultrasonic bath of methanol for 5 minutes to remove traces of the acetone, and blown dry with nitrogen gas for the removal of methanol.

<div align="center">Device Fabrication</div>

A Nano-Master NTE 3000 thermal evaporator was used for the deposition of the organic films. Films were grown on cleaned ITO substrates with shadow masks for use as solar cells, and cleaned Si substrates for use in XRD studies. Prior to film growth, the vacuum chamber was pumped down to $< 10^{-5}$ Torr and baked out by slowly heating the organic material and the substrates to 110 °C to facilitate the outgassing of contaminants.

After the bake-out process, the chamber was pumped down for at least 12 hours until the pressure was $\sim 10^{-6}$ Torr. The substrate plate was then heated to the desired temperature. Once the temperature of the substrates was stable, roughly 80 nm of ZnPc was deposited at a rate of 0.4-0.9 Å/s. Around 80 nm of C_{60} was then deposited on top of the ZnPc at a rate of 0.4-0.9 Å/s. Films were deposited in this way at seven different temperatures: 25 °C, 77 °C, 110 °C, 160 °C, 180 °C, 200 °C, and 224 °C. The film thickness and growth rate were measured in arbitrary units by a quartz crystal monitor (QCM) inside the thermal evaporator. The conversion from arbitrary thickness units to

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[4]1501 Powhatan St., Fredericksburg, VA 22401, USA

FIGURE 11. Shadow masks for top electrical contacts. A sputter deposition system was used for the application of top electrical contacts to each device. The ZnPc/C$_{60}$ film on the left is shown covered with the 6-hole shadow mask to allow for the deposition of multiple small Al contacts. The film on the right is uncovered.

nm was established using X-ray diffraction, in which a film of 500 thickness units was determined to be 22.2 nm thick. The deposition of 1818 thickness units yielded films roughly 80 nm thick. The deposited films were allowed to cool to room temperature before being exposed to air.

Once the film deposition was complete, Al electrical contacts were applied to the top of each bilayer film structure. The application of top contacts was complicated by the presence of pinholes in the thin films. As the size of crystallites in the films increases at higher deposition temperatures, film coverage over the substrate becomes less uniform. This nonuniformity of film growth allows for the existence of large (up to ~10 nm) gaps between grains. Multiple gaps that are stacked on top of each other may form a pinhole, or position on the substrate with little or no film coverage. The application of an electrical contact on top of a pinhole would allow current to flow through the pinhole from one electrode to the other without ever traversing the organic

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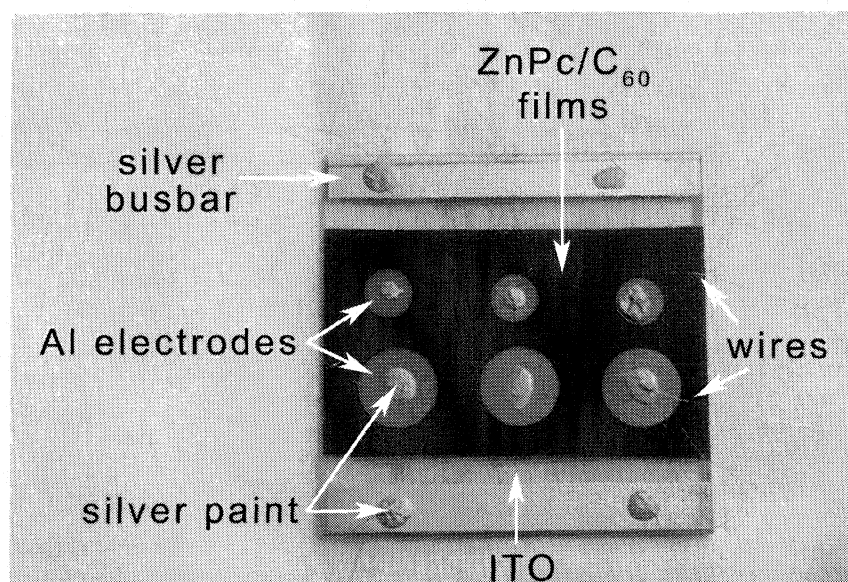
FIGURE 12. Completed ZnPc/C_{60} device. A completed device consists of an 80 nm thin film of C_{60} deposited on top of an 80 nm film of ZnPc on a glass substrate coated with the transparent conductor ITO. Al electrodes are sputtered on top of the organic films and wires are attached to the electrodes and busbars using silver paint.

films, resulting in a shunt current and possibly a short circuit. The probability that an electrical contact is located over a pinhole is reduced if the size of the contacts are reduced. The presence of multiple contacts on each device increases the chances that there is at least one contact that is not located over a pinhole. For these reasons, instead of applying one large (1×1 cm) electrical contact to each device, 6 smaller (3-5 mm diameter) contacts were deposited. The contacts located over pinholes that caused short-circuiting during device testing were not used for data collection.

To define the active area of each device and allow for the application of multiple small electrical contacts, 0.25 mm thick 3×3 cm^2 steel plates were used as shadow masks during the deposition of top electrodes. Each steel plate was drilled with six holes to allow for the application of three 0.3 cm diameter and three 0.5 cm diameter metal contacts, as shown in figure 11. Although smaller electrical contacts are less likely to be located on a pinhole, they also introduce more noise into electrical measurements.

Therefore, electrical contacts with different sizes were used so that the larger contacts that did not cause short-circuiting could be used for data collection. An EMS575X sputter deposition system was used for the application of top contacts. Aluminum contacts (thickness 80 nm) were deposited on the organic films through shadow masks at a rate of 0.2-0.8 Å/s at 3.5×10^{-3} Torr.

For conducting electrical measurements, 32 AWG polythermaleze wires were attached to each device at the silver busbars and the aluminum contacts, as shown in figure 12. The wires were mounted using conductive silver paint. Prior to testing, all devices were stored in a desiccator to prevent degradation.

<u>Data Collection</u>

The operating parameters used to characterize device performance were determined by measuring the I-V characteristics of each completed device. An I-V characteristic curve is obtained by sweeping the electric potential (V) across the device and recording the current (I) through the device as each voltage is applied. I-V measurements were acquired using a custom-built application created with the computer program LabView. A Keithley 2000 multimeter was used to measure current while voltage was applied by an Agilent E3646A DC power supply. The voltage was increased in 7.5 mV increments from 0 to 1.5 V while the current was measured at each voltage step. Average I-V curves were obtained for each device by compiling data from between 5 and 10 I-V sweeps. From the I-V curves, important operating parameters were extracted and compared between different devices. The uncertainty in each operating parameter was obtained from the standard deviation in the data representing that parameter.

A Solar Light 150 W Xenon short arc lamp was used as a light source to simulate solar irradiance conditions. I-V measurements were carried out under standard PV device testing conditions (air-mass 1.5, intensity 1000 W/m², 1 atm). The air-mass (AM)

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coefficient refers to the optical path length through the atmosphere that sunlight must traverse before it reaches the surface of the earth. AM1 corresponds to the solar spectrum after sunlight has passed through earth's atmosphere one time when the sun is at its zenith. AM1.5 corresponds to the solar spectrum after sunlight has passed through an equivalent of 1.5 of earth's atmospheres. AM1.5 is considered the standard solar spectrum for device testing conditions because it refers to a solar zenith angle of 48.2°, which represents a more realistic estimate of the spectrum at temperate latitudes where the majority of the world's large population centers are located [39]. An AM1.5 optical filter was used for simulating the AM1.5 solar spectrum, and the intensity of the light source was adjusted to 1000 W/m^2 prior to each measurement.

The relative abundances of crystalline phases present in the organic films were investigated using a Rigaku SmartLab X-ray Diffractometer with CuK$_\alpha$ radiation ($\lambda = 1.5418$Å). Bilayer ZnPc/C$_{60}$ film structures deposited at 77°C and 224°C on 1×2 cm^2 Si substrates were investigated using small angle $\theta/2\,\theta$ measurements. The peaks in the X-ray diffraction spectra were analyzed to determine the average grain size in the films and to detect the presence of different crystalline phases.

Device Characterization

In order to characterize the performance of a PV device, its internal electronic behavior must be properly understood. This can be achieved by modeling the device as an electrical circuit so that different currents and resistances inside the device can be identified. A PV device under illumination can be represented by an equivalent circuit consisting of an ideal p-n junction diode in parallel with a current source, as shown in figure 13(a). The diode is responsible for the nonlinear I-V characteristics of the device, while the current source represents photocurrent generated by incident light. When illuminated, the I-V curve of a PV device is shifted upwards along the y-axis from the

origin by an amount equal to the maximum current generated the the device, as shown in figure 14.

During the operation of real PV devices, parasitic resistances may contribute to undesirable power dissipation across internal device components, and internal short circuits can lead to the creation of shunt currents. The equivalent circuit of a PV device can better reflect these behaviors if series and shunt resistances are introduced, as shown in figure 13(b). The series resistance R_S represents all the internal resistances present in a device. Resistances at the D-A interface, in the organic semiconductor layers, and at the electrical contacts all contribute to R_S [22]. The shunt resistance R_{SH} represents the presence of short circuit currents that flow between the electrical contacts, such as those which may arise from the presence of pinholes in the organic layers [25]. In an ideal solar cell, there is no internal resistance ($R_S = 0\ \Omega$) and there are no shunt currents ($R_{SH} = \infty$).

From the equivalent circuit with R_S and R_{SH}, the current I produced by the PV device is

$$I = I_L - I_D - I_{SH}, \tag{2.1}$$

where I_L is the photocurrent generated by incident light, I_D is the current through the diode, and I_{SH} is the shunt current. The diode current I_D is given by the Shockley diode equation

$$I_D(V_D) = I_o(e^{qV_D/k_BT} - 1), \tag{2.2}$$

where I_o is the reverse bias diode saturation current and V_D is the voltage across the diode [56]. By Ohm's law, $I_{SH} = V_{SH}/R_{SH}$, so

$$I = I_L - I_D - I_{SH} = I_L - I_o(e^{qV_D/k_BT} - 1) - \frac{V_{SH}}{R_{SH}} \tag{2.3}$$
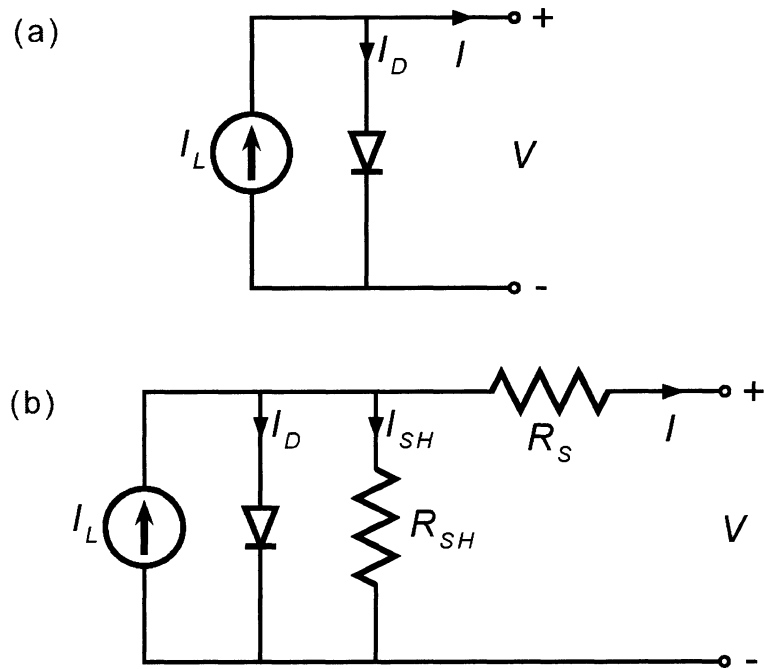
FIGURE 13. Equivalent circuit of a PV device. (a) The equivalent circuit of an ideal PV device consists of a current source in parallel with a diode. (b) A more realistic equivalent circuit contains series resistance R_S and shunt resistance R_{SH}. These parasitic resistances are used to represent the presence of undesirable internal resistances and shunt currents.

and $V_{SH} = V + IR_S$, so

$$I = I_L - I_o(e^{q(V+IR_S)/k_BT} - 1) - \frac{V + IR_S}{R_{SH}}. \tag{2.4}$$

Using this model, it is possible to determine how the operating parameters of PV devices can be influenced by R_S and R_{SH}. One of the most important operating parameters of a PV device is the short-circuit current (I_{sc}). I_{sc} is the maximum amount of current that a device can generate while illuminated with no load and no external voltage applied. This occurs at the beginning of the forward-bias I-V curve measurement sweep, when $V = 0$. For an ideal device, $I_{sc} = I(V = 0) = I_L$. In reality, I_{sc} is strongly dependent on R_S and R_{SH}, both of which influence free charge carrier migration and exciton diffusion. The morphology of organic films in bulk heterojunction devices has been shown to influence R_S and R_{SH}, and hence I_{sc} as well [47]. When I_{sc} is dependent on the active area of the device, which is the case with PV cells, the short-circuit current density J_{sc} is used to characterize the device. J_{sc} is obtained from the y-intercept of the I-V characteristic curve, as shown in figure 14. J_{sc} is calculated by $J_{sc} = I_{sc}/A$, where A is the area of the top electrical contact used for the I-V measurement.

The maximum voltage produced by a PV device is called the open-circuit voltage (V_{oc}), and occurs when the load resistance approaches infinity, or $V_{oc} = V(I = 0)$. V_{oc} is obtained from the x-intercept of the I-V curve, as shown in figure 14. In an ideal device, $I_L = I_{sc}$, and

$$V_{oc} = V(I = 0) = \frac{k_BT}{q} \ln\left(\frac{I_{sc}}{I_D} + 1\right). \tag{2.5}$$

Experimentally, V_{oc} is strongly dependent on R_S. Undesirable voltage drops can occur across high series resistances inside the device, which limits V_{oc}. Since the organic film morphology affects R_S, it can influence V_{oc} as well.

Each point along the I-V curve corresponds to a different device power density output. The maximum power density generated, P_{max}, is equal to the area of the largest

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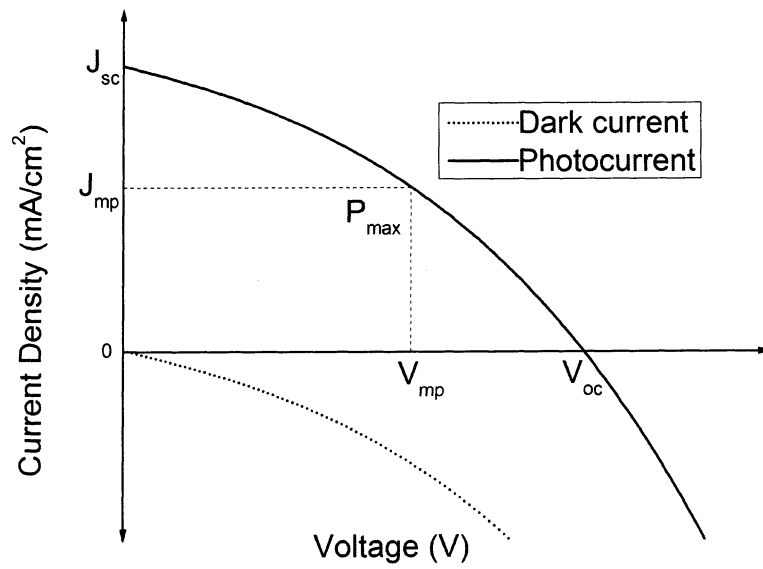
FIGURE 14. I-V characteristics of a typical PV device. The I-V characteristic curve of a PV device is shifted upward on the y-axis from the origin by an amount equal to J_{sc} when the device is illuminated. V_{oc}, J_{sc}, V_{mp}, J_{mp}, and P_{max} are important parameters for characterizing PV devices. From these parameters, the device efficiency η and the fill factor FF can be calculated.
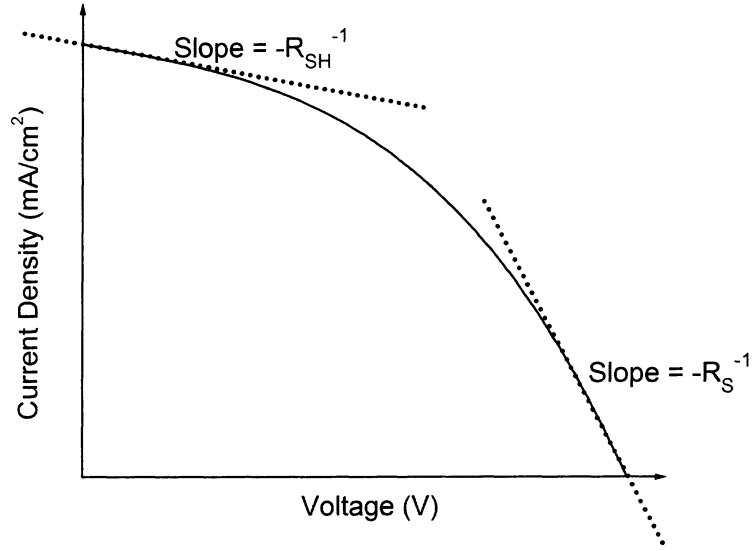
FIGURE 15. R_S and R_{SH}. Increasing the series resistance R_S and decreasing the shunt resistance R_{SH} create undesirable consequences for PV device performance. The values of the resistances can be found by taking the inverse of the slopes of the I-V curves at V_{oc} and J_{sc}. In a perfectly ideal device, $R_S = 0\ \Omega$ and $R_{SH} = \infty$, and the I-V curve would intersect the x and y axes perpendicularly to form a rectangle, resulting in $FF = 1$.

rectangle that can fit under the I-V curve, as shown in figure 14. The P_{max} operating point is related to the voltage at maximum power V_{mp} and current density at maximum power J_{mp}. These are the voltage and current density being produced by the device when it is delivering P_{max}. Just like V_{oc} and J_{sc}, P_{max} can be influenced by R_S and R_{SH}. When R_S increases, V_{mp} decreases, which leads to a reduction in P_{max}. When R_{SH} decreases, J_{mp} decreases, and P_{max} is further reduced. The influence of R_S and R_{SH} is present in nearly all areas of device operation. The film morphology in organic solar cells is important in large part because it can strongly influence the values of these parasitic resistances [47].

A common measure of the quality of a PV device is the ratio between the area of the P_{max} rectangle and the rectangle formed by V_{oc} and J_{sc}. This ratio, or measure of how much the P_{max} rectangle fills the $V_{oc} \times J_{sc}$ rectangle, is called the fill factor (FF), and is

calculated by

$$FF = \frac{V_{mp} \times J_{mp}}{V_{oc} \times J_{sc}} = \frac{P_{max}}{V_{oc} \times J_{sc}}.$$ (2.6)

The I-V curve of a perfectly ideal PV device intersects the current and voltage axes perpendicularly to form a rectangle, which results in $FF = 1$. The effect of introducing undesirable resistances on the shape of the I-V curve is shown in figure 15. The FF corresponds to how much power a device generates compared to how much it would generate if $R_S = 0$ Ω and $R_{SH} = \infty$. Typical FFs for Si-based solar cells lie between 0.45 and 0.75. As the value of the FF essentially includes contributions from J_{sc}, V_{oc}, and P_{max}, it is a widely used comprehensive measure of device quality.

If the PV device with an active area A is illuminated with irradiance L, the power conversion efficiency η of the device is found by

$$\eta = \frac{P_{max}}{L \times A}.$$ (2.7)

η is the most widely used measure of device performance because it relates the power of incident light to the amount of power generated by the device. While η typically ranges from 15% to 25% in Si-based photovoltaics, bilayer heterojunction devices commonly exhibit $\eta < 3\%$ [11, 23]. Only after $\eta > 15\%$ and higher lifetimes for OPVs are achieved can they begin to compete commercially with existing Si-based systems [19, 20].

Together, the parameters J_{sc}, V_{oc}, P_{max}, FF, and η comprehensively characterize the performance of a PV device. The values of these parameters measured in bilayer devices fabricated here are presented in the next chapter.

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CHAPTER 3

RESULTS AND ANALYSIS

The results of I-V measurements and XRD measurements on ZnPc/C$_{60}$ bilayer

solar cells are presented and analyzed in this chapter. From the I-V measurements,

important device operating parameters are extracted and compared between films

fabricated at different temperatures. The magnitude of the parasitic resistances R_S and

R_{SH} is determined and their effect on device operation is discussed. The presence of a

back diode effect in the I-V measurements and the influence that this effect has on device

performance is investigated. Finally, the results of XRD measurements are used to gather

information about the relative abundances of different crystalline phases present in the

organic films. This information is used for additional analysis of the I-V characteristics.

Current-Voltage Characteristics

The operating parameters used to describe solar cell performance were obtained

from the I-V characteristics of a series of ZnPc/C$_{60}$ bilayer heterojunction devices. The

variation in the shapes of the I-V curves in figure 16 suggests that the film deposition

temperature has a strong influence on the electronic properties and solar cell

performance of the organic films. The temperature dependence of each device operating

parameter is plotted in figures 17-24. Before discussion of the device parameters can

take place, an unexpected feature of the I-V curves should be noted. A sharp decrease in

the current density at low voltages occurs in every device. This undesirable phenomenon,

known as a back diode effect, is discussed in detail at the end of this section.

The open-circuit voltage V_{oc}, short-circuit current density J_{sc}, power conversion

efficiency η, and fill factor FF of devices fabricated at different deposition temperatures

Film Deposition Temperature:
— 25°C
— — ·77°C
· · · · 110°C
—·— 160°C
············ 180°C
—··— 200°C
—···— 224°C
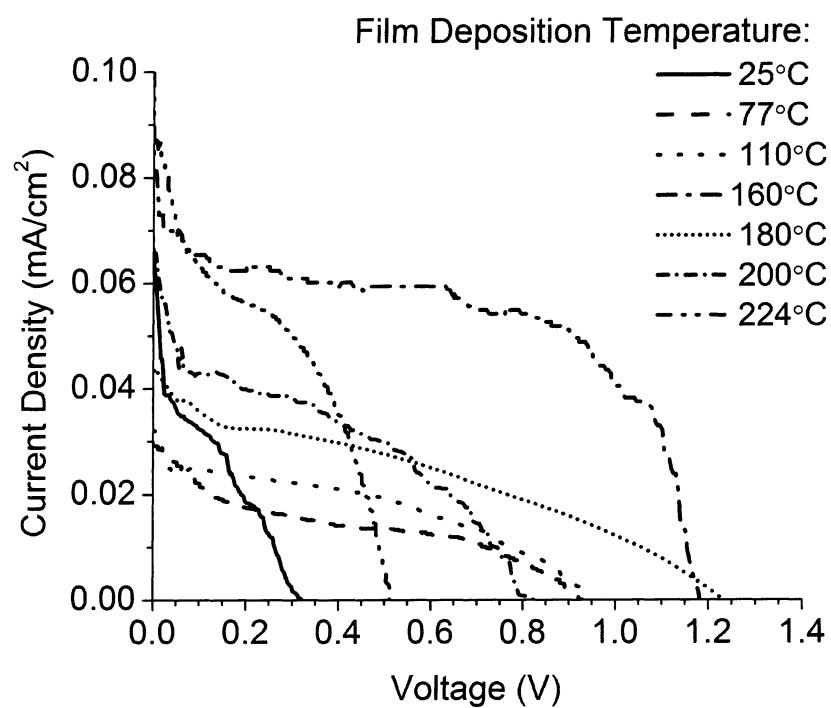
FIGURE 16. Dependence of I-V characteristics on film deposition temperature. The I-V characteristic curve of each thin film device is influenced by the temperature at which the film was deposited. Each parameter that can be used to characterize solar cell performance is extracted from the I-V curves.

T_{dep} are shown in table 1. Uncertainties in the measurements are indicated with parentheses. The values of these parameters will be discussed in the following sections.

TABLE 1. Performance of ZnPc/C$_{60}$ Bilayer Thin Film Devices

T_{dep} (°C)	V_{oc} (V)	J_{sc} (mA/cm^2)	η (%)	FF (%)
25	0.3(1)	0.07(1)	0.005(4)	25(5)
77	0.9(1)	0.03(2)	0.008(5)	29(1)
110	0.9(1)	0.03(1)	0.012(4)	39(7)
160	1.2(1)	0.08(1)	0.043(6)	45(4)
180	1.2(2)	0.04(1)	0.024(5)	46(10)
200	0.8(2)	0.07(1)	0.017(6)	31(7)
224	0.5(2)	0.11(2)	0.016(8)	28(7)

Device Performance Parameters

Short-Circuit Current Density

One of the important operating parameters used to characterize device performance is the short-circuit current density J_{sc}, which is equal to the y-intercept of the I-V curve. The dependence of J_{sc} on the film deposition temperature is shown in figure 17. Although a strong correlation between J_{sc} and deposition temperature is not observed, films deposited at temperatures over 150 °C generally result in higher J_{sc}. This can be understood in terms of charge carrier mobility in the bulk organic materials. Undesirable electron-hole recombination occurs most efficiently at grain boundaries [11]. This recombination limits charge carrier migration, which leads to a reduction in J_{sc}. The number of grain boundaries decreases as the grain size increases, so films grown at higher temperatures typically allow for higher charge carrier migration and therefore higher J_{sc} [27].

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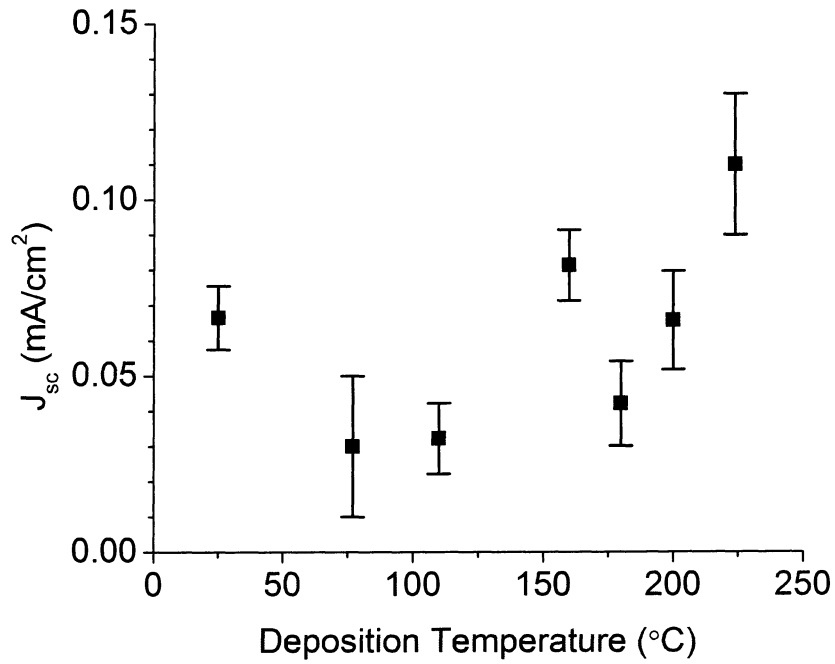FIGURE 17. Dependence of J_{sc} on film deposition temperature. Although a strong correlation between J_{sc} and deposition temperature is not observed, J_{sc} is generally higher at temperatures over 150 °C. This is likely due to the improved charge carrier migration in large grains that form at higher deposition temperatures.

The J_{sc} values presented here are around one order of magnitude lower than typical J_{sc} values reported for ZnPc/C_{60} bilayer heterojunction devices $(0.5 - 1.5 \text{ mA/cm}^2)$ [8, 56]. Although the fundamental structure of bilayer devices is the ZnPc/C_{60} interface, nearly all of the devices in the literature contain additional organic exciton-blocking layers or doped layers between the organic materials and electrodes which have been shown to improve device performance. Exciton-blocking layers prevent the migration of electron-hole pairs to electrical contacts, and doping in charge transport layers helps to increase charge carrier mobility and improve the quality of the contact between the ITO and the organic materials. It has been demonstrated that these additional active layers lead to significant increases in J_{sc} [23, 26, 51]. The low J_{sc} values reported here are likely the result of a combination of factors, including the absence of exciton-blocking layers and the strong presence of back diode effects. The reduction of J_{sc} by the presence of back diodes has been observed in many similar studies [23, 46, 48, 53].

Although the influence of the film deposition temperature on solar cell performance has been well-studied for bulk heterojunction devices, it has not been thoroughly investigated in bilayer heterojunction devices [37, 36, 40]. For this reason, the deposition temperature dependence of J_{sc} presented here can be compared to results obtained from studies only on bulk heterojunction devices. Typically, J_{sc} is much higher in bulk devices $(0.5 - 15 \text{ mA/cm}^2)$ because of the shorter average distance between exciton creation and the D-A interface [25, 36, 37, 40, 47]. Although a difference of around two orders of magnitude exists between the J_{sc} reported here and the J_{sc} reported in bulk devices, the deposition temperature dependence of J_{sc} can be compared across both types of devices. The results found here are plotted with those reported in three different studies on 1:1 ZnPc/C_{60} bulk heterojunction devices in figure 18 [36, 37, 40]. It
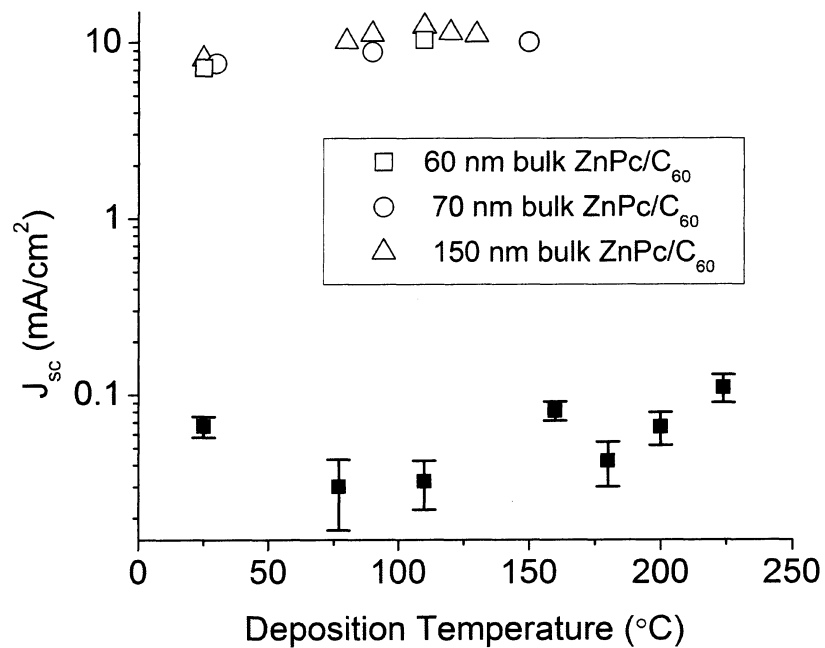
FIGURE 18. Comparison of J_{sc} results. The J_{sc} values determined here (solid black squares) are about two orders of magnitude smaller than those found in studies on bulk heterojunction devices [36, 37, 40]. In both bilayer and bulk devices however, it is found that J_{sc} is not strongly influenced by deposition temperature.

is clear that J_{sc} is not strongly influenced by the deposition temperature in either bilayer or bulk heterojunction devices.

The interface between the organic materials and the top metal contact can strongly influence J_{sc} [55, 56]. It has been observed that a thin insulating layer can form between the Al top electrode and the electron acceptor material during device fabrication [26]. This insulating layer can result in J_{sc} as low as 0.125 mA/cm^2, which is about an order of magnitude smaller than J_{sc} values measured in devices that are fabricated with silver contacts [54]. This small J_{sc} is similar to the J_{sc} values presented here, which suggests that the C_{60}/Al interface contains a thin insulating layer of AlO. This insulating layer reduces the number of charge carriers that reach the electrode, which further limits the value of J_{sc}. The effect of oxygen diffusion into the device materials is described in further detail during the discussion of back diode effects.

Open-Circuit Voltage

Another important device operating parameter is the open-circuit voltage V_{oc}, which is equal to the x-intercept of the I-V curve. The dependence of V_{oc} on the film deposition temperature is shown in figure 19. The value of V_{oc} is found to vary by nearly 1 V depending on the deposition temperature, and exhibits a clear peak in films deposited at temperatures near 180 °C. Interestingly, this result disagrees with the findings of many previous studies on organic heterojunction devices (see figure 20), in which V_{oc} is thought to depend only on the energies of the HOMO and LUMO levels of the donor and acceptor materials and the work functions of the electrodes [25, 36, 37, 40, 42].

Studies that discuss the origin of V_{oc} commonly employ the metal-insulator-metal (MIM) model, which dictates that the value of V_{oc} arises solely from the energies of the molecular orbitals of the device materials, not from the film morphology. The MIM model places the theoretical limit of V_{oc} in ZnPc/C_{60} devices near 0.8 V, which is equal to the energy difference between the ZnPc HOMO and the C_{60} LUMO levels. The
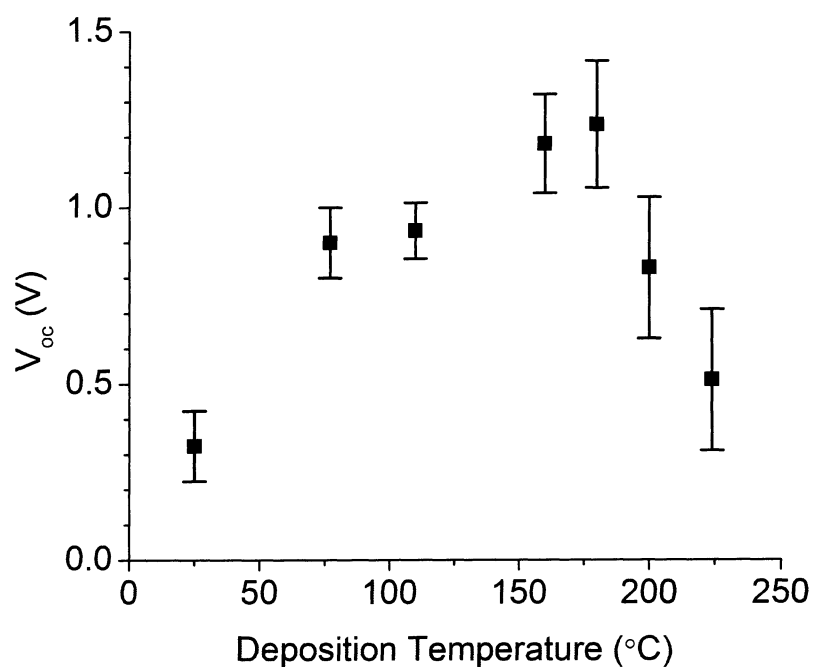
FIGURE 19. Dependence of V_{oc} on film deposition temperature. V_{oc} exhibits a peak when films are deposited at temperatures near 180 °C. This result is contradictory to the predictions of the MIM model, which asserts that V_{oc} is a consequence of the device materials, not the device morphology.
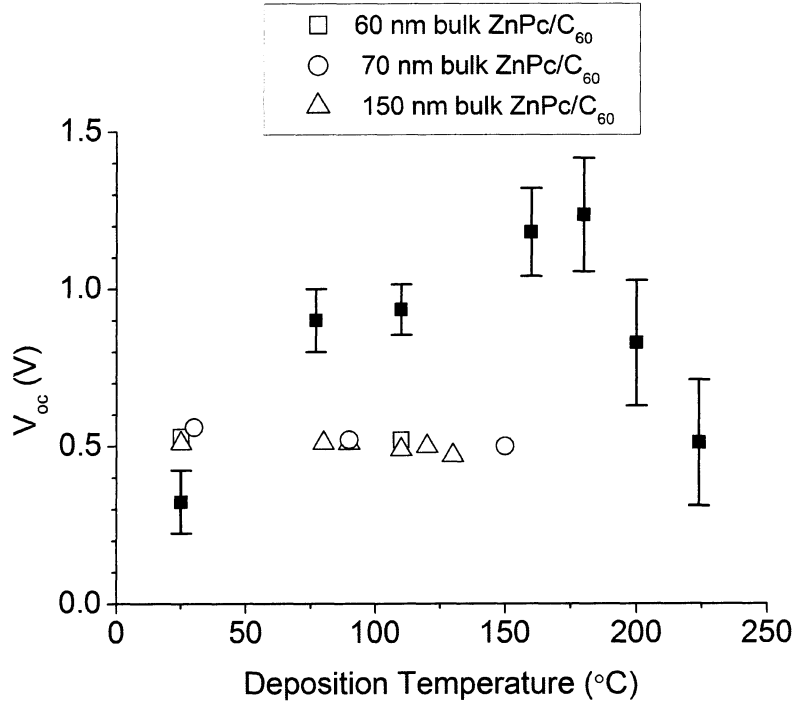
FIGURE 20. Comparison of V_{sc} results. The V_{oc} values reported here (black squares) exhibit a peak when films are deposited at temperatures near 180 °C. In bulk ZnPc/C_{60} devices, V_{oc} is not strongly influenced by the film deposition temperature [36, 37, 40]. It is possible that the high V_{oc} values reported here are a consequence of pinholes in the C_{60} layer, which results in the presence of ITO/ZnPc/Al interfaces. These interfaces behave like single layer organic Schottky diode solar cells, which typically produce higher V_{oc} and lower J_{sc} and η than bilayer heterojunction devices [58, 61].

presence of R_S in experimental devices can lower V_{oc} to around 0.5 V, which is a common value of V_{oc} reported in the literature [25, 51]. However, recent investigations have shown that the MIM model cannot adequately explain the source of V_{oc}, and it is recognized among many researchers that the exact origin of V_{oc} cannot be accounted for by any of the common models used to describe organic heterojunction devices [28, 52]. It is now acknowledged that several factors which can influence V_{oc} are not incorporated in the MIM model, including charge transport in the donor and acceptor materials, the active layer thicknesses, and the morphology of the active layers [28, 52, 55, 56].

The thickness of the organic layers can have a strong influence on V_{oc} [55]. In fact, it has been demonstrated that V_{oc} can be increased from 0.2 V to 0.6 V merely by reducing the thickness of the C_{60} film from 75 nm to 25 nm in a ZnPc/C_{60} bilayer device [56]. This effect is thought to result from the appearance of pinholes in the C_{60} layer at low film thicknesses. The presence of pinholes in the C_{60} film may allow for the creation of ZnPc/Al interfaces. This would effectively transform the bilayer device ITO/ZnPc/C_{60}/Al into the single layer device ITO/ZnPc/Al. Single layer phthalocyanine solar cells, or Schottky diode solar cells, typically produce higher V_{oc} and lower J_{sc} and η than bilayer devices [58, 61]. In Schottky diode solar cells consisting of a single layer of copper phthalocyanine (CuPc), V_{oc} as high as 1.2 V, J_{sc} as low as 6.8 μA/cm^2, and η as low as 0.003 % have been reported [61]. These values are consistent with the findings of this study, in which unusually high V_{oc} and unusually low J_{sc} and η values are measured in bilayer devices. The I-V behavior measured here is consistent with single layer Schottky devices (see table 2), indicating that the presence of C_{60} pinholes may allow for the formation of ZnPc/Al interfaces. The high V_{oc} produced in Schottky devices is believed to be a result of the difference in energy between the ZnPc HOMO level and the work functions of the electrodes [23, 28]. In bilayer devices, the ZnPc HOMO and C_{60} LUMO levels are separated by 0.8 eV (see figure 7), which places a theoretical upper limit of 0.8 V on V_{oc} [28]. If pinholes in the C_{60} layer result in the formation of an ITO/ZnPc/Al junction, then the theoretical upper limit of V_{oc} is the energy difference between the ZnPc LUMO level and the work function of ITO, which is 1.3 V. This voltage is similar to the highest reported V_{oc} here, 1.2 V, which suggests that the devices exhibiting V_{oc} over 0.8 V predominantly exhibit Schottky diode solar cell behavior instead of bilayer heterojunction device behavior. As shown in table 2, most of the ZnPc/C_{60} devices fabricated here exhibit the high V_{oc} and low J_{sc} that are characteristic of single layer phthalocyanine-based Schottky solar cells.

Although the presence of an ITO/ZnPc/Al junction can result in higher V_{oc}, it is undesirable because the efficiency of the charge transfer reaction at this interface is very low ($\eta_{CT} < 10\%$) [23]. The low rate of exciton dissociation results in a lack of free charge carriers, which drastically reduces J_{sc} and η. If the majority of exciton dissociation occurs at the ITO/ZnPc interface, it is likely that the measured J_{sc} and η would be at least an order of magnitude lower than expected for bilayer devices. This is consistent with the results found here, as summarized in table 3. Since the formation of ITO/ZnPc/Al junctions leads to a reduction in η, the peak in device efficiency for devices fabricated between 150 °C and 200 °C is likely a consequence of the reduction in back diode effects observed at these temperatures, not the presence of ITO/ZnPc/Al junctions. The peak in η is analyzed further during the discussion of back diode effects.

TABLE 2. Comparison of Bilayer Device to Single Layer Pc Schottky Devices

Active Material	Thickness (nm)	V_{oc} (V)	J_{sc} ($\mu A/cm^2$)	η (%)	Ref.
ZnPc/C$_{60}$	80/80	1.2(1)	80(10)	0.04(1)	-
CuPc	100	0.9	24	0.004	[59]
PbPc	100	0.7	1	0.08	[60]
CuPc	80	0.9	17	-	[61]

It is useful to compare the results measured here with the results of other studies on ZnPc/C$_{60}$ bilayer solar cells. Since the majority of the bilayer devices investigated in the literature are deposited at room temperature [25, 56, 57], they are compared to the device fabricated at room temperature in this study in table 3. The first row of the table presents parameters measured in this study, while the following rows each describe the ZnPc/C$_{60}$ bilayer device performance measured in other experiments. From the table, it is clear that the V_{oc} produced by the room temperature device measured here is

consistent with the values reported in other studies. Only in devices fabricated at higher temperatures does V_{oc} become unusually high. The J_{sc} value reported here is lower than that of the other devices. It is possible that this is a result of the presence of pinholes in the C_{60} layer, as discussed previously. Although the FF measured here is lower than those reported other studies, the FF increases for devices fabricated at higher temperatures. This can partly be attributed to the increase in grain size, and hence charge carrier mobility, which occurs at higher deposition temperatures [27, 35]. Although the devices compared in table 3 contain different layer thicknesses, no obvious trend between thickness and performance is observed. It is recognized that layer thickness can strongly influence device performance, but the optimum layer thicknesses in $ZnPc/C_{60}$ bilayer devices is still under debate in the literature [25, 56]. η reported here is around two orders of magnitude lower than typical η in $ZnPc/C_{60}$ bilayer devices. From tables 2 and 3, it is clear that the majority of the devices fabricated here exhibit characteristics which more closely resemble single layer Pc Schottky solar cells than $ZnPc/C_{60}$ bilayer heterojunction solar cells. This suggests that poor film coverage on the substrates led to the presence of ITO/ZnPc/Al interfaces, which result in Schottky-like device behavior.

While it is possible that pinholes in the C_{60} result in the unusually high V_{oc} and low J_{sc} and η measured here, perhaps the presence of the peak in V_{oc} can also be explained in terms of pinholes. Since the presence of pinholes would allow Schottky-type diode solar cells to form at ITO/ZnPc/Al interfaces adjacent to $ZnPc/C_{60}$ interfaces, the resultant device I-V characteristics may contain contributions from both interfaces [56]. Films grown near room temperature generally contain smaller grains than those grown at higher temperatures, which reduces the probability of pinhole formation [35]. As the film deposition temperature is increased, larger grains form, and the chances of pinhole formation increase. An increase in the amount of pinholes allows for the presence of more ITO/ZnPc/Al interfaces, which leads to a higher measured V_{oc}.

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C_{60} undergoes a phase transition near 150 °C, as described in the last section of this chapter. During this phase transition, the density of the bulk C_{60} film decreases by around 8.5% [49]. This decrease in density may allow for the diffusion of Al atoms from the top electrode into the C_{60} layer. The diffusion of metal atoms into the organic layers strongly increases the severity of back diode effects, which are known to decrease V_{oc} [48]. The measured V_{oc} values begin to decrease when films are deposited at temperatures over 180 °C. It is possible that this decrease in V_{oc} can be attributed to the onset of severe back diode effects, which arise because of the diffusion of Al atoms into the high temperature C_{60} films. The presence of the peak in V_{oc} is analyzed further during discussion of the parasitic resistances R_S and R_{SH}.

TABLE 3. Comparison of Bilayer Device to Other $ZnPc/C_{60}$ Bilayer Devices

T_{dep} (°C)	$ZnPc/C_{60}$ Thicknesses (nm/nm)	V_{oc} (V)	J_{sc} (mA/cm^2)	η (%)	FF (%)	Ref.
25	80/80	0.3(1)	0.07(1)	0.005(4)	25(5)	-
25	75/75	0.2	1	0.24	-	[56]
25	40/40	0.55	5.15	1.8	63	[25]
25	25/45	0.195	0.167	0.13	29.9	[57]

Maximum Power Density

A more comprehensive measure of device performance is the maximum power density P_{max}, which is equal to the area of the largest rectangle that can fit inside the I-V curve of each device. The dependence of P_{max} on the film deposition temperature is shown in figure 21. P_{max} exhibits a strong peak around 160 °C, which is close to the same temperature at which V_{oc} reaches a peak. This suggests that the P_{max} value measured here is influenced more strongly by V_{oc} than by J_{sc}, which does not exhibit a peak. Although P_{max} is closely related to V_{oc} and J_{sc}, it represents a better measure of
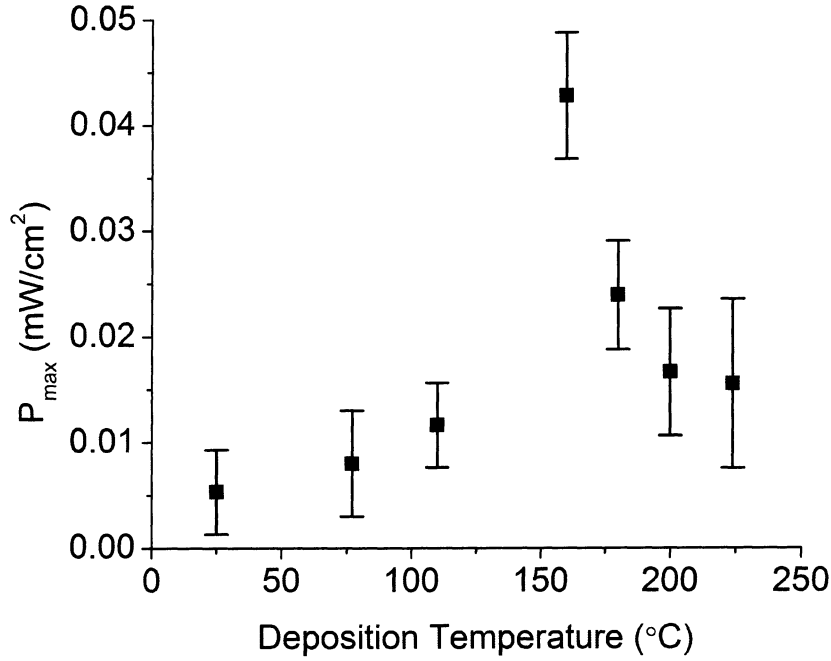
FIGURE 21. Dependence of P_{max} on film deposition temperature. P_{max} exhibits a peak near 160°C. This suggests that P_{max} is more strongly influenced by V_{oc}, which exhibits a similar peak, than by J_{sc}, which does not contain a peak.

overall device performance because its value includes both voltage and current characteristics. The peak in P_{max} suggests that although J_{sc} is not strongly dependent on deposition temperature, the general quality of the devices are.

Fill Factor

An even more comprehensive measure of device quality is the fill factor FF, which represents the degree to which a device produces J_{sc} and V_{oc} while operating at P_{max}. The FF dependence on deposition temperature is shown in figure 22. Like V_{oc} and P_{max}, FF exhibits a peak between 160°C and 180°C.

Although the dependence of FF on film deposition temperature has not been thoroughly investigated in bilayer devices, it is well-studied in $ZnPc/C_{60}$ bulk heterojunction devices. The results from three different bulk devices ([36, 37, 40]) are
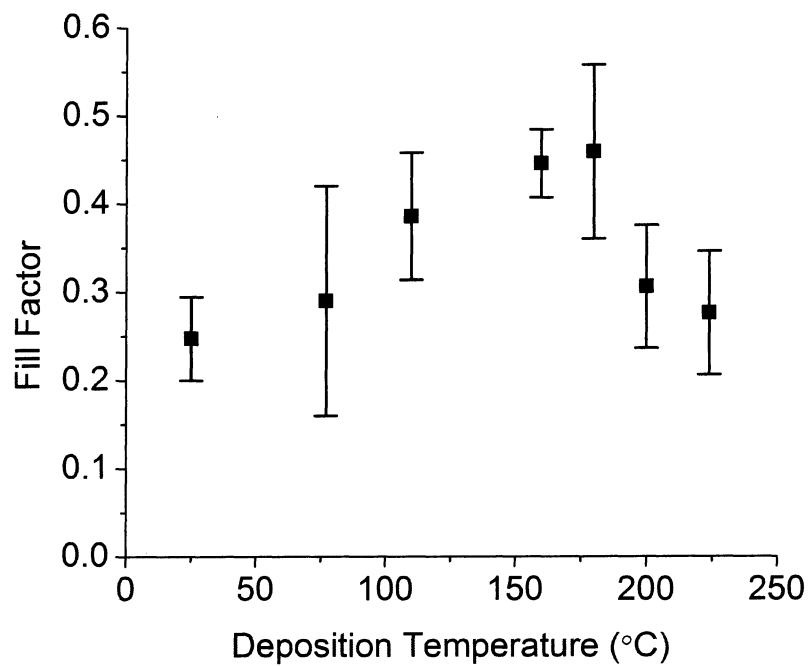
FIGURE 22. Dependence of FF on film deposition temperature. The fill factor FF
exhibits a peak near 180 °C, which is similar to the peaks measured in V_{oc} and P_{max}. The
peak suggests that the morphology leads to optimized device performance around this
temperature.

compared to the results found here in figure 23. The FF measurements made here are consistent with the results from the bulk heterojunction devices. In both bilayer and bulk devices, FF increases when the film deposition temperature is increased from 25 °C to 160 °C. Since the experiments on bulk devices did not include films at temperatures over 160 °C, it cannot be determined whether FF reaches a peak at higher temperatures for bulk devices, as the results found here indicate. However, several studies on ZnPc/C_{60} heterojunction structures agree that substrate heating is an effective method for the control of morphology and device performance, as indicated by the increase in FF between 25 °C and 160 °C [36, 37, 40].

Device Efficiency

The device efficiency η is shown in figure 24. Since P_{max} is measured in mW/cm^2 and the power of incident light on each device during testing was 100 mW/cm^2, the measured P_{max} values are equal to the values of η. The same peak in P_{max} is present in η when films are grown at 160 °C. Although the efficiencies measured here are around two orders of magnitude smaller than those reported in similar bilayer ZnPc/C_{60} devices (table 3, they are consistent with the low efficiencies measured in single layer phthalocyanine Schottky solar cells (table 2) [25, 36, 37, 40, 56, 57]. This suggests that the devices measured here behave more like single layer Shottky devices than bilayer heterojunction devices, which may be the result of pinholes in the organic films. The temperature dependence of ZnPc/C_{60} bulk heterojunction device efficiencies measured in other studies is shown in figure 25 [36, 37, 40]. Although no devices were fabricated at temperatures over 150 °C, it is clear that at temperatures below 150 °C, device efficiency increases as the deposition temperature is increased. This finding is consistent with the results reported here, in which efficiency increases from 25 °C to 160 °C. It has not been determined whether a peak in device efficieny in bulk heterojunction devices exists at temperatures over 150 °C. The increase in efficiency
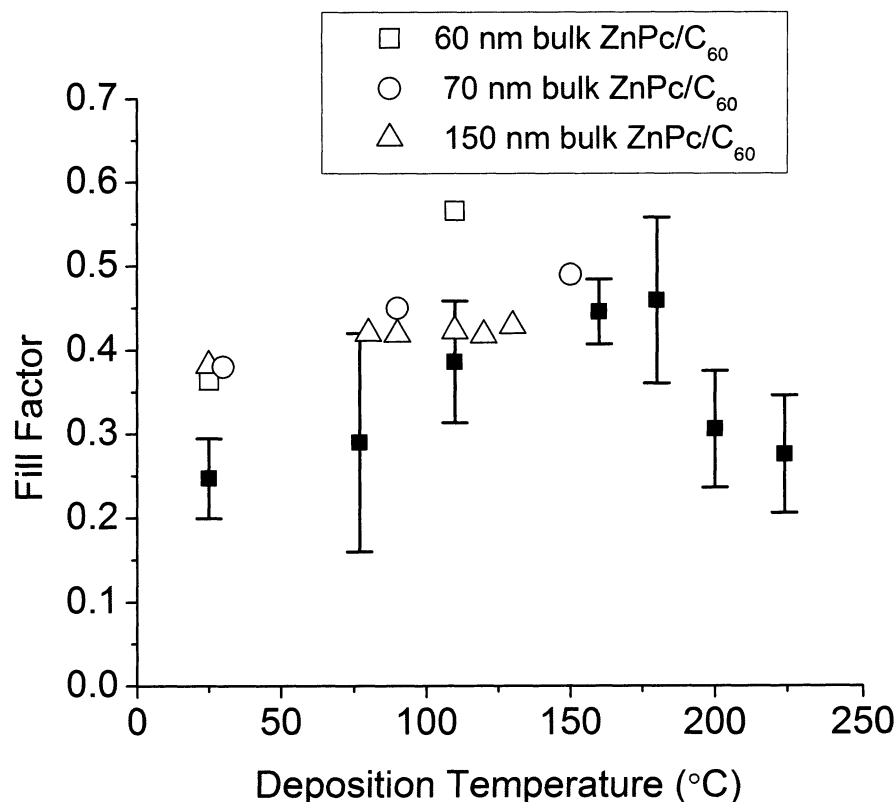
FIGURE 23. Comparison of FF results. The FF values measured here (black squares) are consistent with the results from studies on ZnPc/C$_{60}$ bulk heterojunction devices [36, 37, 40]. In both bilayer and bulk devices, FF increases when the film deposition temperature is increased from 25°C to 160°C. Since the experiments on bulk devices did not fabricate films at temperatures over 150°C, it cannot be determined whether FF exhibits a peak in bulk devices like the one measured in bilayer devices.

FIGURE 24. Dependence of η on film deposition temperature. The device efficiency η exhibits a peak near 160 °C, which is similar to the peaks measured in V_{OC} and FF. The peak suggests that optimized morphology occurs when films are deposited near this temperature.

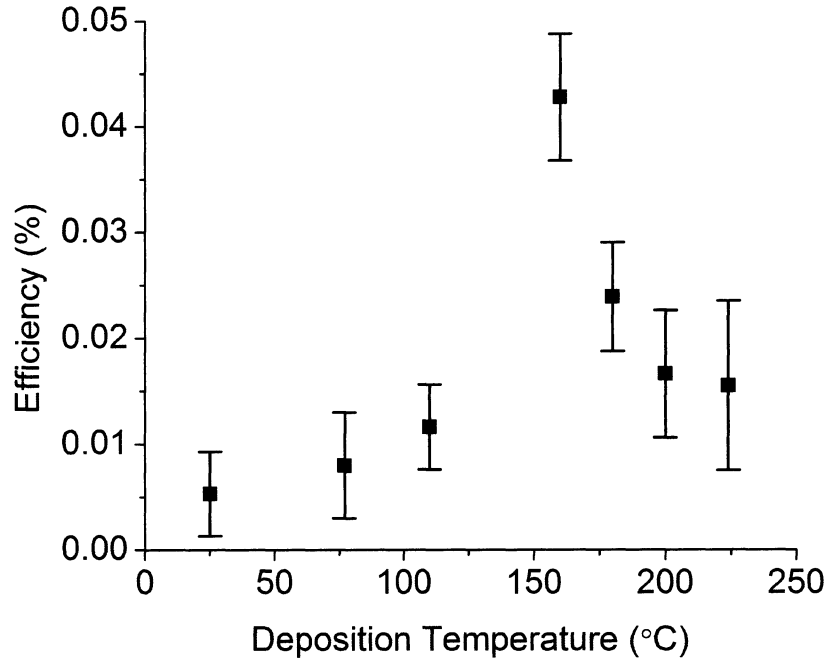with deposition temperature at temperatures below 150 °C has been attributed to improved η_{ED} and η_{CC} resulting from the presence of larger crystallites, and improved η_{CT} due to the increase in the surface area of the D-A interface, which is a result of higher film roughness [36, 37, 40].

Parasitic Resistances

In order to analyze device performance in terms of parasitic resistances, the values of the series and shunt resistances of each device were extracted from the I-V curves as outlined in figure 15. The series resistance R_S, which includes contributions from all of the internal device resistances, is shown plotted against the film deposition temperature in figure 26. As the deposition temperature is increased, R_S exhibits a
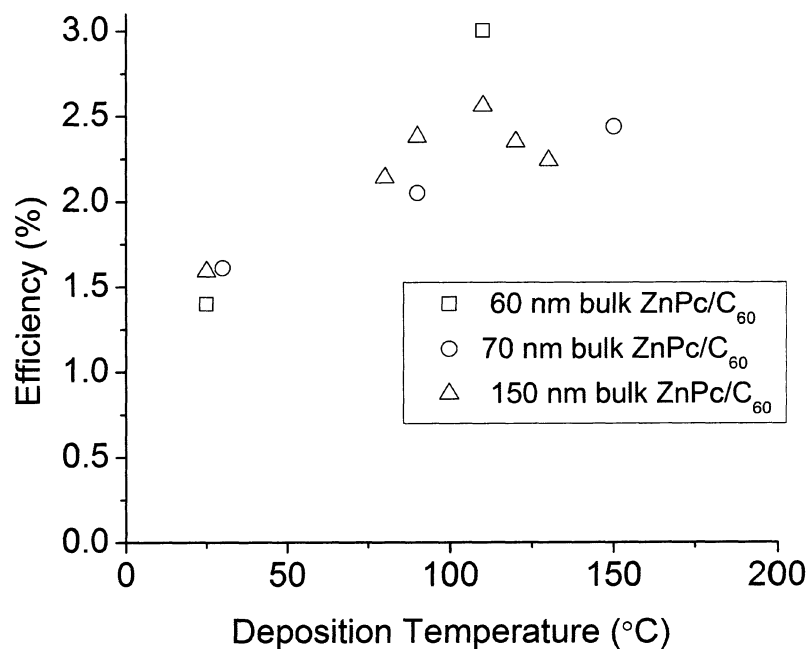
FIGURE 25. Dependence of η on film deposition temperature in bulk devices. The device efficiency η in bulk heterojunction $ZnPc/C_{60}$ devices generally increases when films are deposited at temperatures from 25 °C to 150 °C [36, 37, 40]. This result is consistent with the measurements performed here, in which η increases in films deposited from 25 °C to 150 °C. No data is available for bulk heterojunction devices deposited at temperatures over 150 °C.
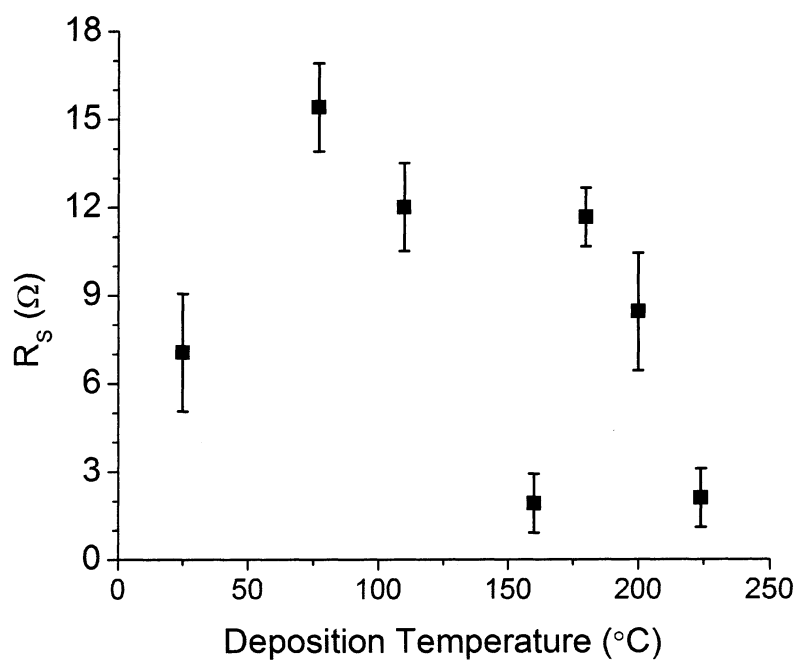
FIGURE 26. Dependence of R_S on film deposition temperature. The series resistance R_S generally decreases as the film deposition temperature is increased. Films grown at higher temperatures contain larger grains, which leads to improvement in charge carrier mobility [27, 35]. Larger grains also form rougher films, which increases the surface area of the D-A interface and the surface area of the contact between the organic materials and the electrodes, resulting in better charge migration.

general decrease. This is likely due to a decrease in the resistance contribution from the bulk organic materials, and a decrease in the resistance at the interface between the organic layers and the electrodes. As the film deposition temperature increases, the grains in the film become larger and more elongated [35]. The larger grains typically lead to increased charge carrier mobility because of the reduction in the number of grain boundaries that charge carriers must traverse [21]. The lower series resistance at higher temperatures may be a consequence of film roughness as well. Films deposited at high temperatures exhibit increased roughness because of the larger grains present. The increase in roughness increases the surface area of the D-A interface, which leads to higher η_{CT}. Increased film roughness also produces a larger surface area between organic materials and the electrodes, which improves charge carrier migration out of the organic layers. Although the general decrease in R_S can be used to explain the improvement in device performance at high temperatures, the values of R_S cannot explain the presence of peaks in the values of V_{oc}, η, and FF.

The values of the shunt resistance R_{SH} were also extracted from the I-V characteristics. Interestingly, R_{SH} exhibits a peak similar to those found in V_{oc}, η, and FF, as shown in figure 27. This is a significant result because it suggests that the peaks in V_{oc}, η, and FF may be correlated to the high R_{SH} found in films deposited near 160°C. The presence of the peak in R_{SH} will be discussed further in the next section.

Discussion of Back Diode Effects

Although the I-V characteristic curves of ideal PV devices intersect the current and voltage axes perpendicularly, the I-V measurements presented in figure 16 exhibit an unusually large (up to 0.02 mA) decrease in current density at low voltages (< 0.2 V). This phenomenon, known as a back diode effect, is undesirable because it can lead to a decrease in FF and device efficiency of up to 50% [46]. It is widely recognized that this effect originates at the interface between the top metal electrode and the organic
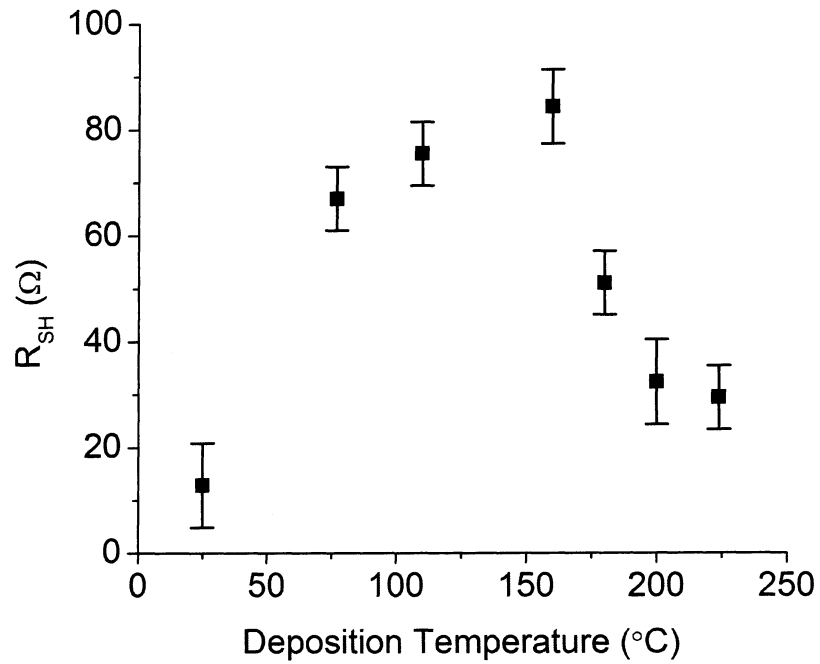
FIGURE 27. Dependence of R_{SH} on film deposition temperature. The shunt resistance R_{SH} exhibits a peak around 160 °C. This peak is similar to the peaks found in the values of V_{oc}, P_{max}, and FF, which suggests that the peaks in the performance parameters are correlated to the value R_{SH}.
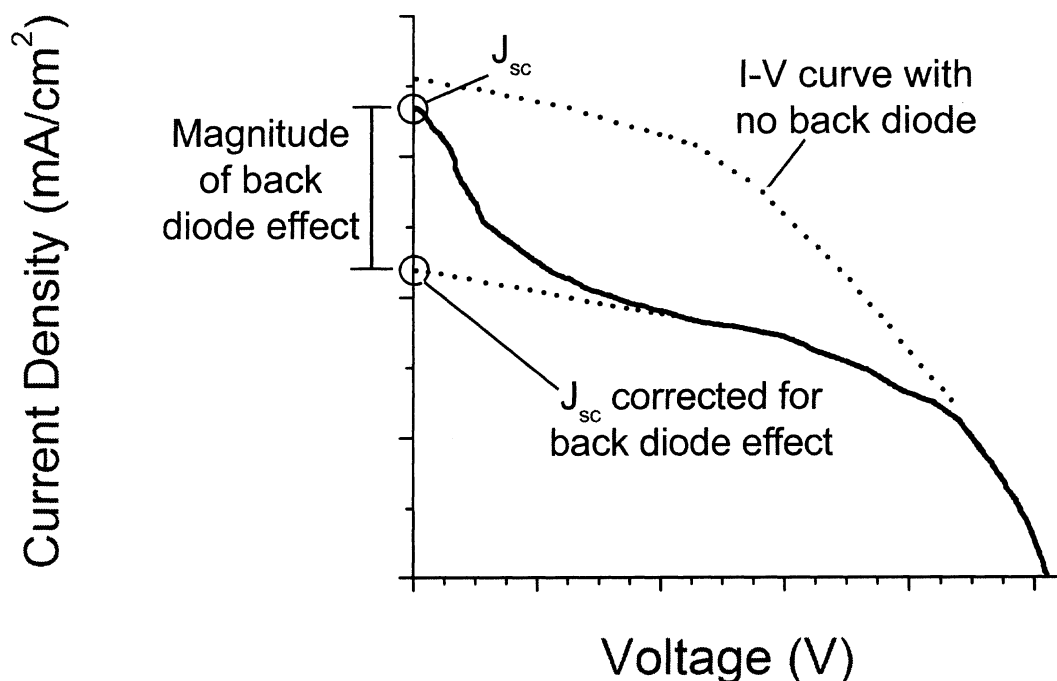
FIGURE 28. Removal of back diode effects. Extrapolation of each I-V curve to produce a linear intersection of the current density axis provides an estimate of the magnitude of the back diode effect. The value of J_{sc} can also be estimated in this way.

films [46, 48]. Degradation of the device materials can change the metal/semiconductor junction from an ohmic contact to a rectifying Schottky barrier. A device with this undesirable rectification behaves as if there are two diodes in the equivalent circuit that are oriented in opposite directions. As one diode produces the desirable non-linear I-V behavior of the device, the other works to block the production of photocurrent. The resultant I-V curve is a linear combination of the characteristics of the two competing diodes [56].

It is believed that the intrinsic instability of organic films, as well as the presence of oxygen, water, and other defects at the metal/semiconductor junction strongly contribute to the development of back diodes [46]. The diffusion of metal atoms from the top contact into the organic films can accentuate back diode effects, as well as
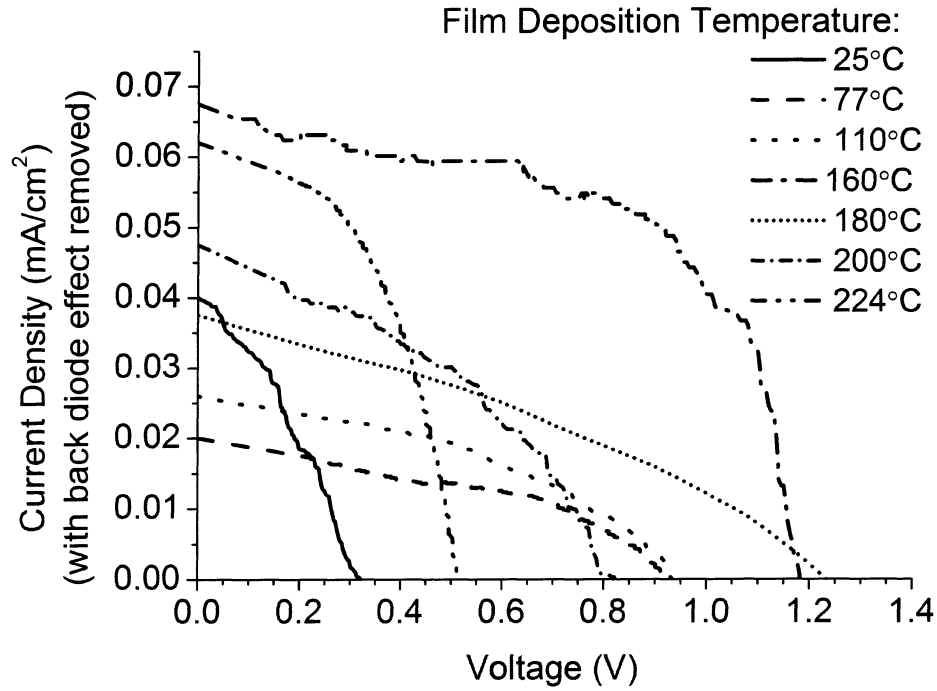
FIGURE 29. I-V characteristics in the absence of back diodes. The I-V curves without back diode effects exhibit higher FF and η.

increase electron-hole recombination rates, which leads to a drop in V_{oc} [48]. To prevent the oxidation of top contacts, devices are commonly fabricated and tested inside argon gloveboxes, or measures are taken to remove adsorbed oxygen before device testing [23, 28]. Lithium fluoride has been applied between Al electrodes and C_{60} films to improve electron injection into the electrode and prevent the diffsion of Al atoms into the organic materials [56]. It has also been shown that devices encapsulated with getter materials for absorbing oxygen and water are less susceptible to the development of back diode behavior [46].

It should be noted that the values of J_{sc} show in figure 17 and reported in tables 1, 2, and 3 include the presence of back diode effects. In order to investigate the temperature dependence of J_{sc} without the presence of back diodes, and to determine if

back diode effects are temperature dependent, the magnitude of the back diode effect can be estimated from the I-V characteristics of each device. The analysis of back diode effects is outlined in figure 28. Although I-V curves of real devices do not intercept the current density axis perpendicularly unless $R_{SH} = \infty$, the curves are linear at the y-intercept in the absence of back diodes. Using this guideline, the I-V curves can be extrapolated towards the y-axis and the values of J_{sc} can be estimated without back diode contributions. The I-V characteristics with back diode effects removed are shown in figure 29. The new J_{sc} values were extracted from the corrected I-V curves and their temperature dependence is plotted in figure 30. The removal of the back diode effects leads to an increase in the FF and η of every device, with some achieving as high as 50% improvement. However, the J_{sc} values show the same general increase with deposition temperature that they did before the back diode effects were removed. This suggests that the temperature dependence of J_{sc} is not strongly influenced by the presence of back diodes.

The difference between the value of the original measured J_{sc} and the value of J_{sc} with the back diode effect removed can be used to estimate the magnitude of the back diode present in each device. It has been experimentally verified that film morphology can influence the rate of device degradation and the severity of back diode development [53]. In order to investigate this, the magnitude of the back diode effect in each device was estimated (using the procedure illustrated in figure 28) and plotted against the film deposition temperature in figure 31. Although the back diode effect does not appear to be strongly dependent on deposition temperature, it does reach a minimum when films are deposited at temperatures between 100°C and 200°C. This is a significant result because it indicates that the severity of back diode effects is smallest in the temperature regime where the values of the device performance parameters V_{oc}, η, and FF are highest. The correlation between small back diode effects and high device
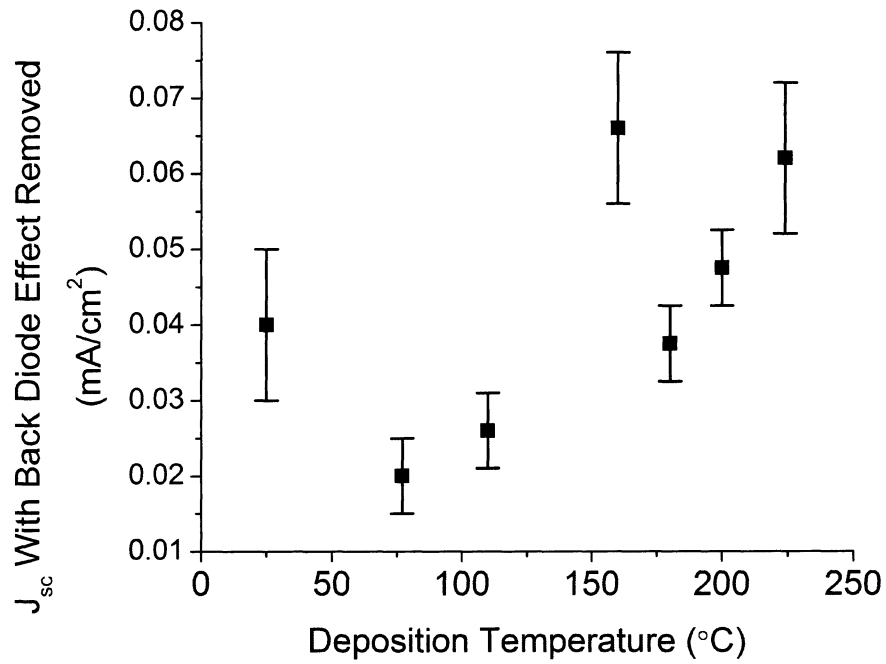
FIGURE 30. J_{sc} in the absence of back diodes. When the back diode effects are removed from the I-V curves, the J_{sc} values show the same general increase with deposition temperature that they did before the back diode effects were removed. This suggests that the temperature dependence of J_{sc} is not strongly influenced by the presence of back diodes.
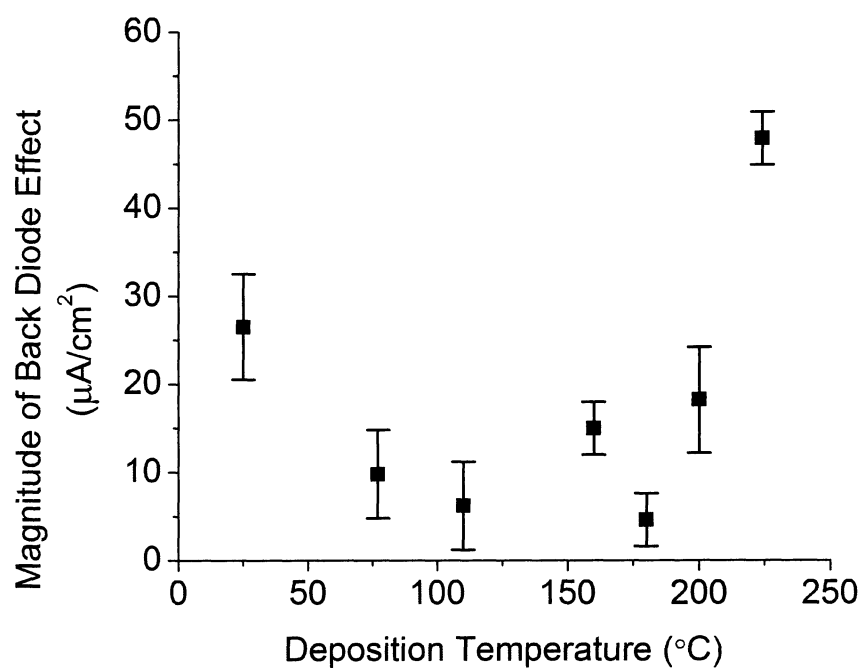
FIGURE 31. Magnitude of back diode effects. The severity of back diode effects reaches a minimum between 100 °C and 200 °C, which is the same temperature regime in which device performance reaches a peak. This result suggests that an increase in back diode effects is correlated to a decrease in device performance, which is consistent with the results of similar studies [23, 46, 48, 53].

performance suggests that the back diodes play a significant role in determining device performance. This result is consistent with the findings of many studies on device degradation and back diode effects [23, 46, 48, 53].

It is useful to note that the magnitude of the back diode effect reaches a minimum in the same temperature range at which R_{SH} is largest. It is possible that the presence of shunt currents in the organic films is correlated to the presence of back diodes. It has been observed that one of the causes of severe back diode effects is the diffusion of metal atoms from the top electrode into the organic films [48]. The diffusion of Al atoms from the top electrode into the C_{60} film can create strongly conductive pathways through the film. If Al atoms diffuse into the C_{60} layer near a pinhole in the film, an ITO/ZnPc/Al junction can be formed. The formation of this interface would result in both reduced R_{SH} and reduced device performance. Low density, porous organic films are more susceptible to diffusion from Al atoms. Since the C_{60} phase transition near 150°C results in a reduction in film density, there is a higher probability that Al atoms will diffuse into the C_{60} film and cause shunt currents at high temperatures. It is suspected that this phase transition is partly responsible for the increase in the severity of back diode effects and the decrease in R_{SH} at high temperatures. It is likely that the increase in the magnitude of the back diode effects and the decrease in R_{SH} at high temperatures is correlated to the decrease in V_{oc}, η, and FF at high temperatures.

X-Ray Diffraction Results

In order to determine the relative abundances of crystal phases present in the organic films, the X-ray diffraction spectra from two bilayer ZnPc/C_{60} thin films were examined. The spectrum of a film deposited at 77°C is compared to the spectrum of a film deposited at 224°C in figure 32. The peaks produced by well-known crystal phases are labeled with their Miller indicies [25, 37]. From the differences in the diffraction spectra, it is clear that the relative abundances of crystal phases in both ZnPc and C_{60} are
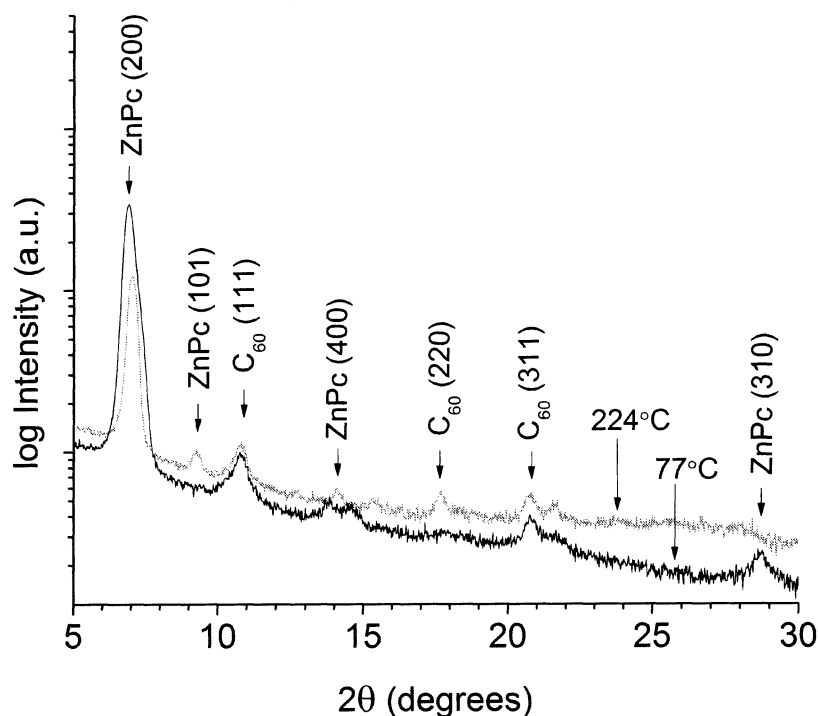
FIGURE 32. X-ray diffraction peaks in ZnPc/C_{60} bilayer films. The peaks in the X-ray diffraction spectra of ZnPc/C_{60} bilayer film structures deposited at 77 °C and 224 °C indicate that several crystal phase transitions occur inside this temperature regime. The types of crystal phases present in the organic films can strongly influence solar cell performance.

directly affected by the film deposition temperature. The properties of the observed diffraction peaks are displayed in tables 4 and 5, along with the lattice spacing corresponding to each peak. The difference in the deposition temperature of the two films is responsible for the differences in the sizes and positions of the peaks.

While the $C_{60}(111)$ and $C_{60}(311)$ peaks are present in films deposited at both 77 °C and 224 °C, the $C_{60}(220)$ peak is pronounced only in the high temperature film, which indicates that the $C_{60}(220)$ crystal phase appears when C_{60} is deposited at temperatures between 77 °C and 224 °C. It has been shown that C_{60} undergoes a 2nd or higher order phase transition at 150 °C [49]. This transition results in an 8.5% decrease in density of the C_{60} film [50]. The decrease in density of the high temperature C_{60} films

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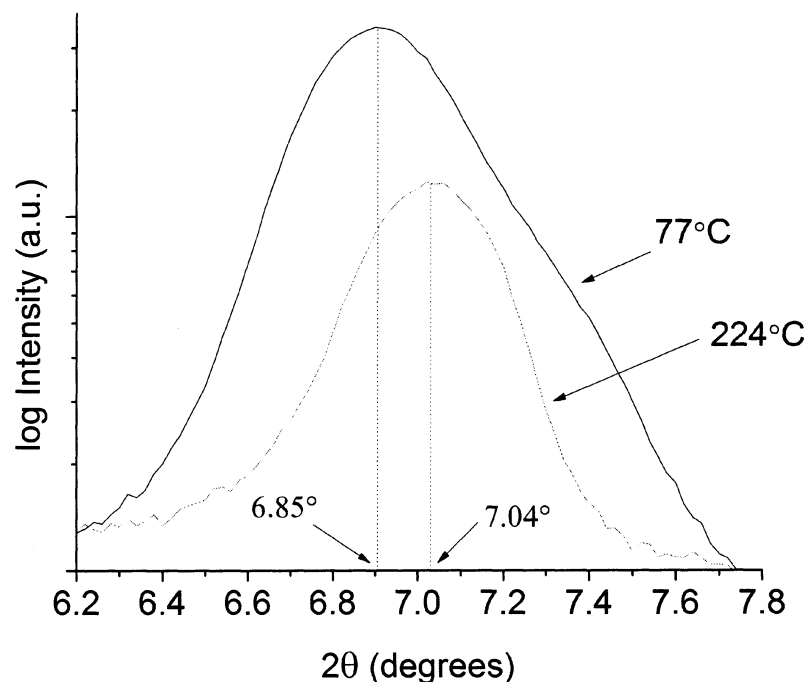
FIGURE 33. ZnPc α → β phase transition. The X-ray diffraction peaks produced by the α and β phase ZnPc crystals occur at $2\theta = 6.85°$ and $2\theta = 7.04°$, respectively. The shift of the peak indicates that a phase transition has occurred between 77 °C and 224 °C.

can negatively affect solar cell performance. Porous films can limit charge carrier migration, reduce the surface area of the D-A interface, and allow for an increase in pinholes, which can lead to shunt currents and the formation of back diode effects [48]. For these reasons, the reduction in device performance at temperatures near 160 °C may be at least partly attributed to the C_{60} phase transition at 150 °C.

The X-ray diffraction spectra suggest that a phase transition occurs in ZnPc somewhere between 77 °C and 224 °C as well. The prominent ZnPc(101) peak in the high temperature spectrum is not present at 77 °C. More importantly, the ZnPc(200) peak undergoes an important change, as shown in figure 33. In the film deposited at 77 °C, the ZnPc(200) peak occurs at $2\theta = 6.85°$, which corresponds to α phase crystallites with lattice spacing 12.9 Å [62]. The same peak occurs at $2\theta = 7.04°$ in the

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TABLE 4. X-ray Diffraction Peaks in ZnPc/C$_{60}$ Films Deposited at 77 °C

Peak Name	Peak Position (deg)	FWHM (deg)	Height (cps)	Lattice spacing (Å)
ZnPc(200)	6.85	0.462	21000	12.9
ZnPc(400)	13.91	0.534	62	6.4
ZnPc(310)	28.73	0.534	57	3.1
C$_{60}$(111)	10.81	0.669	254	8.2
C$_{60}$(311)	20.79	0.729	96	4.3

TABLE 5. X-ray Diffraction Peaks in ZnPc/C$_{60}$ Films Deposited at 224 °C

Peak Name	Peak Position (deg)	FWHM (deg)	Height (cps)	Lattice spacing (Å)
ZnPc(200)	7.04	0.341	5700	12.6
ZnPc(101)	9.23	0.311	93	9.6
ZnPc(400)	14.08	0.341	59	6.3
C$_{60}$(111)	10.78	0.503	202	8.2
C$_{60}$(220)	17.72	0.341	107	5.0
C$_{60}$(311)	20.72	0.536	74	4.3

film deposited at 224 °C, which corresponds to β phase ZnPc with lattice spacing 12.6 Å [25, 62]. These results confirm that the ZnPc α → β phase transition may occur at temperatures between 150 °C and 200 °C [25, 43].

The ZnPc α → β phase transition can have important consequences for solar cell performance. As mentioned previously, this phase transition increases the distance between adjacent zinc atom chains from 12.22 Å to 13.31 Å. In order to reach adjacent zinc chains in a ZnPc film, excitons must diffuse roughly 9% farther through β phase crystallites than α phase crystallites. Since exciton diffusion is strongly influenced by

intermolecular spacing [19], η_{ED} can be significantly diminished by the ZnPc $\alpha \rightarrow \beta$ transition. The temperature range at which the performance parameters V_{oc}, P_{max}, and FF reach a peak is consistent with the temperature of the $\alpha \rightarrow \beta$ phase transition. This suggests that as grains get larger, device performance improves until the phase transition occurs. At the phase transition, the presence of β phase crystallites reduces η_{ED} and η_{CC}. As the film deposition temperature is increased past the phase transition temperature, the abundance of β phase crystallites and lack of α phase crystallites leads to significant decreases in η_{ED} and η_{CC}.

The X-ray diffraction results can also be used to provide a rough estimate the size of crystallites in the organic films. The average grain size D is found from the Scherrer equation

$$D = \frac{k\lambda}{\beta \cos\theta},$$ (3.1)

where β is the FWHM of the diffraction peak, θ is the diffraction angle, λ is the X-ray wavelength ($\lambda = 1.5418$ Å for CuK$_\alpha$ radiation), and the shape factor $k = 0.95$ [45]. Ten different peaks in each spectrum were analyzed. The average grain size was calculated to be 15 nm in the film deposited at 77 °C and 23 nm in the film deposited at 224 °C. This result confirms that an increase in deposition temperature produces an increase in grain size, which can improve charge carrier migration and exciton diffusion, and increases the surface area of the D-A interface. The grain sizes found here are consistent with those reported in the literature [35, 45].

CHAPTER 4

CONCLUSION

Thin film organic solar cells are emerging as an attractive low-cost alternative to silicon-based photovoltaics. However, organic solar cell performance must improve before organic devices can become competitive with existing silicon-based systems. Organic thin films are commonly deposited by thermal evaporation. During the film deposition process, the temperature of the substrate can be used to control the morphology of the deposited film, with higher substrate temperatures resulting in rougher films with larger grains. The film morphology can affect exciton diffusion, exciton dissociation, and charge carrier migration, which strongly influence the electronic and photovoltaic properties of deposited films.

One well-studied organic thin film solar cell structure consists of a bilayer heterojunction between the organic semiconductors ZnPc and C_{60}. The influence of film morphology on the performance of ZnPc/C_{60} bilayer heterojunction solar cells is investigated here. Seven ZnPc/C_{60} devices were fabricated at different temperatures, ranging from 25 °C to 224 °C. The I-V characteristics of each device were measured, and important photovoltaic operating parameters were extracted from the I-V measurements and compared between devices fabricated at different temperatures.

The values of the open-circuit voltage V_{oc}, device efficiency η, and fill factor FF exhibit peaks when films are deposited at temperatures between 160 °C and 180 °C. The performance peaks can be largely attributed to the film morphology. As substrate temperatures are increased from 25 °C to 160 °C, the grain size and roughness of the films increases, which leads to improved exciton diffusion and charge carrier migration.

Between 150 °C and 200 °C, both ZnPc and C_{60} undergo crystalline phase transitions. The ZnPc $\alpha \rightarrow \beta$ phase transition results in larger spacing between zinc atom chains, which limits exciton diffusion and charge carrier migration. The C_{60} phase transition near 150 °C results in an 8.5% decrease in the C_{60} film density. This allows for the diffusion of metal atoms from the top electrode into the organic films, which leads to the formation of strong back diode effects and shunt currents, both of which decrease device performance. The presence of crystalline phase transitions in the same temperature range in which the device performance is highest suggests that V_{oc}, η, and FF are strongly influenced by the ZnPc and C_{60} phase transitions.

A strong correlation between film deposition temperature and short-circuit current density J_{sc} is not observed. This result is confirmed by similar experiments. However, the J_{sc} and η values measured here are more than an order of magnitude lower than those found in other studies on ZnPc/C_{60} bilayer devices. In addition, the V_{oc} values reported here are around twice as high as those reported in similar studies. The high V_{oc}, low J_{sc}, and low η values measured here are characteristic of single layer Pc-based Schottky diode solar cells. This suggests that pinholes in the C_{60} film allow for the formation of ITO/ZnPc/Al junctions, which effectively transform the bilayer heterojunction devices into single layer Schottky devices. While Schottky-type devices typically produce higher V_{oc}, they are undesirable because of their low J_{sc} and η.

The presence of back diode effects in all of the fabricated devices may be attributed to degradation of the organic material at the C_{60}/Al interface and diffusion of Al atoms into the C_{60} films. Device shunt resistance R_{SH} reaches a peak between 100 °C and 200 °C, which is the same temperature range in which devices exhibit the smallest back diode effects. This suggests that the strength of R_{SH} and the prevention of back diodes are strongly correlated. Furthermore, the peak in R_{SH} occurs at the same temperature range in which the performance parameters reach a maximum value. This

indicates that the device performance, which is related to the film morphology, is strongly linked to both R_{SH} and the presence of back diodes. This is a result that has been widely confirmed in the literature. The overall solar cell performance of ZnPc/C$_{60}$ bilayer devices is found to be optimized when devices are deposited at temperatures between 160 °C and 180 °C. As the film deposition temperature is increased, the increase in grain size leads to improved charge carrier mobility and exciton diffusion, which are responsible for higher device efficiencies. At temperatures near 160 °C, the increasing presence of back diode effects and the decrease in shunt resistance begins to limit device performance. The undesirable device characteristics become more dominant as films are deposited at temperatures over 180 °C, so the optimization of device performance occurs at film deposition temperatures between 160 °C and 180 °C. The morphology of films deposited in this temperature range leads to the highest ZnPc/C$_{60}$ bilayer heterojunction solar cell performance.

The results of this study have provided valuable insight into future possible avenues of research. Investigating the specific origin of the back diode effects can be accomplished by varying the top contact material, or by altering the interface between the C$_{60}$ and Al. The presence of pinholes in the C$_{60}$ layer can investigated using AFM or other microscopy techniques. It is also possible to create bulk heterojunction ZnPc/C$_{60}$ devices, and compare their film morphology dependence with that of the bilayer devices studied in this work. The research conducted here will hopefully serve as a useful foundation on which future studies of organic photovoltaics can take place.

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