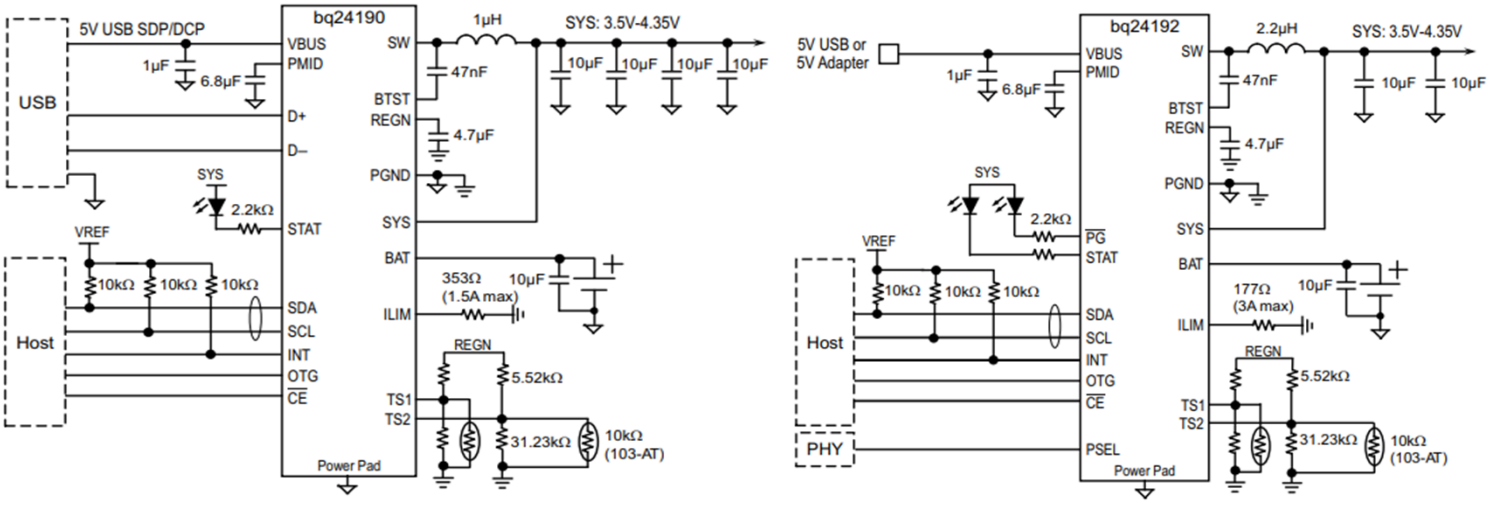
## BQ24190/2 TYPICAL SCHEMATIC




## BQ24190/2 SCHMATIC CHECKLIST

| PIN NAME | | REQUIREMENT | COMPONENT | MIN | TYP | MAX | DESCRIPTION | COMMENTS AND RELEVANT EQUATIONS |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | **USB data line pair** | |
| D+/D- BQ24190 ONLY | 2,3 | Optional | | | | | Positive line of the USB data line pair. | 1. D+/D- based USB host/charging port detection. The detection includes data contact detection(DCD), primary and secondary detection in BC1.2. |
| | | Optional | | | | | Negative line of the USB data line pair. | 2. If D+/D- based input current limit detection is not used, short D+/D- pins together. |
| PSEL BQ24192 ONLY | 2 | | | | | | **Power source selection input.** | |
| | | Required | | | | | | High indicates a USB host source and Low indicates an adapter source. Do not float. |
| /PG BQ24192 ONLY | 3 | | | | | | **Open drain active low power good indicator.** | |
| | | Optional | PG resistor | | 2.2 kΩ | 10 kΩ | Connect to the pull up rail via 10-kΩ resistor. | LOW indicates a good input source if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and current limit is above 30 mA. |
| STAT | 4 | | | | | | **Open drain charge status output** | |
| | | Optional | STAT resistor | | 2.2 kΩ | 10 kΩ | Connect to the pull up rail via 2.2-kΩ resistor. | 1. If not used, leave it float. 2. HIGH indicates charge complete or charge disabled. When any fault Digital condition occurs, STAT pin in blinks at 1 Hz. |
| SCL/SDA | 5-6 | | | | | | **I2C Interface clock and data** | |
| | | Optional | SCL resistor | | 10 kΩ | | Connect SCL to the logic rail through a 10-kΩ resistor. | If I2C communication is not used, leave it float. |
| | | Optional | SDA resistor | | 10 kΩ | | Connect SDA to the logic rail through a 10-kΩ resistor. | If I2C communication is not used, leave it float. |
| INT | 7 | | | | | | **Open-drain Interrupt Output** | |
| | | Optional | INT resistor | | 10 kΩ | | Connect the INT to a logic rail via 10-kΩ resistor. | 1. If not used, leave it float. 2. The INT pin sends active low, 256-µs pulse to host to report charger device status and fault. |
| OTG | 8 | | | | | | **Active high enable pin during boost mode.** | |
| | | Optional | | | | | USB current limit selection pin during buck mode, and active high enable pin during boost mode. | 1. If OTG boost mode is not used, short it to ground. 2. In buck mode with USB host (PSEL=High), when OTG = High, IIN limit = 500 mA and when OTG = Low, IIN Digital limit = 100 mA. 3. The boost mode is activated when the REG01[5:4] = 10 and OTG pin is High. |
| /CE | 9 | | | | | | **Active low Charge Enable pin.** | |
| | | Required | | | | | | 1. /CE pin must be pulled High or Low. 2. Battery charging is enabled when REG01[5:4] = 01 and CE pin = Low. |
| ILIM | 10 | | | | | | **Input current limit Input.** | |
| | | Required | ILIM resistor | | * Ω | | A resistor is connected from ILIM pin to ground to set the maximum limit as IINMAX = (1V/RILIM) × 530 | 1. The actual input current limit is the lower one set by ILIM and by I2C REG00[2:0]. 2.The minimum input current programmed on ILIM pin is 500 mA. 3. If ILIM pin is short, the input current limit is set by the register. 4. If ILIM pin is open, the input current is limited to zero |
| TS1, TS2 | 11,12 | | | | | | **Temperature qualification voltage inputs.** | |
| | | Required | TS resistors and thermistor | | | | Connect a negative temperature coefficient thermistors. Recommend 103AT-2 thermistors. |  1. If thermistor is not used, set TS pin voltage within normal range. 2. If thermistor is used, program temperature window with a resistor divider from REGN to TSx to GND. Charge suspends when either TS pin is out of range. |
| VBUS | 1,24 | | | | | | **Input source to the charger** | |
| | | Required | VBUS caps | 1uF | | | | 1. Place a 1-µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. 2. It is recommended to have a total of ~10uF capacitance at VBUS & PMID for USB input compliance. |
| PMID | 23 | | | | | | **Actual input source to the charger** | |
| | | Required | PMID caps | 6.8uF | | | | Given the total input capacitance, put 1 µF on VBUS to PGND, and the rest capacitance on PMID to PGND. |
| VBAT | 13-14 | | | | | | **Positive battery connection point** | |
| | | Required | VBAT caps | 10uF | 10uF | | | 1. Connect a 10 µF closely to the BAT pin. 2. Charger may operate normally when battery is not connected. |
| VSYS | 15-16 | | | | | | **System connection point.** | |
| | | Required | VSYS caps | 20uF | 20uF | 40uF | | Connect a 20 µF closely to the SYS pin. The preferred ceramic capacitor is 6V or higher rating, X7R or X5R. |
| SW | 19-20 | | | | | | **Switching node connecting to output inductor.** | |
| | | Required | Output inductor | 1uH | | 2.2uH | | The charger device has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 15 kHz and 25 kHz. With 2.2-µH inductor, the typical output capacitor value is 20 µF. |
| | | Optional | SW Resistor | | * Ω | | Switching converter snubber circuit | Snubber circuit values empirically determined if required. Recommend unpopulated footprint on new designs. |
| | | Optional | SW Cap | | * F | | | |
| BTST | 21 | | | | | | **PWM high side driver positive supply.** | |
| | | Required | BTST-SW cap | 0.047uF | 0.047uF | 0.047uF | | Connect the 0.047µF bootstrap capacitor from SW to BTST. |
| | | Optional | BTST resistor | | * Ω | | Bootstrap capacitor snubbing resistor | Help with EMI performance. Recommend unpopulated footprint on new designs. |
| REGN | 22 | | | | | | **PWM low side driver positive supply output.** | |
| | | Required | REGN cap | 4.7uF | 4.7uF | 4.7uF | | Connect a 4.7 µF (10 Vrating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS1 and TS2 pins. |
| PGND | 17-18 | | | | | | **Power ground connection for high-current power converter node.** | |
| | | Required | | | | | | On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin. |
| PowerPAD | | Required | | | | | | Always solder PowerPAD Pad to the board, and have vias on the PowerPAD plane star-connecting to PGND and ground plane for high-current power converter. |