Mpeg WebVC

ISO/IEC 14496-29 Web video coding
Open source hardware video encoder
May 2020 Update

Low Latency Hardware Video Encoder

- Author:
  - Field programmable gate array (FPGA) evangelist. Hw eng, spec video, codecs, imaging, crypto.
  - January tech dive on MPEG WebVC (ISO/IEC 14496-29 Web video coding). The LCD of H.264
- Open Source Project: Verilog source code.
  - 1080p hardware WebVC video encoder project on the AWS F1 fpga platform
  - Low latency, VQ less a diff at high bw. Col refresh with long-term grey reference entry stub.
  - Dev Platform: Laptop, Vivado and AWS r5.large 1$/day interactive synthesis. Github hosting, MIT license.
  - C Model encoder & Verilog block transform core (combinatorial) with sims. 27 cyc/MB
  - Synthesis: 30K Lut, 48 mult (5% of F1). Tpd: tbd.
  - Minimal viable 1080p encoder arch. Verilog coding support blocks: Word pack, and 2D DMA R/W.
- Ongoing: towards a functional 1mSec latency1080p encoder on F1,
  - Emulation Prevention 0x03 byte insertion
  - Rate Control: CVBR, C-model and Verilog,
  - Verilog top level integration and connection to AWS HDK Shell (pci, dma, dram)
  - Full chip synthesis. Hardware bring-up on AWS F1
  - Pipeline transform core. 15 Mhz → 16ms, 250 Mhz → 1mSec 1080p frame latency
  - Direct host memory access, 4:2:2 raster format conversion
- Roadmap:
  - Open source project quality, documentation, guides, scripts, release, Github, MIT …
  - ease-of-use: ffmpeg integration, AMI image, container …
  - Xilinx Vitis platform packaging. Enables rapid port to other clouds and … ex mining boards
  - AI inference (Vitis AI) based ROI Qp modulation.
  - VQ: Mode decision, motion estimation, adaptive quant, RDopt, RC

Codec Architecture