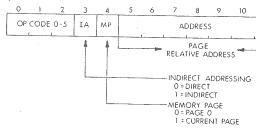
BASIC INSTRUCTIONS

AND TAD ISZ DCA JMS JMP IOT OPR	0000 1000 2000 3000 4000 5000 6000 7000	logical AND 2's complement add increment, and skip if zero deposit and clear AC jump to subroutine jump in/out transfer operate	2.6 2.6 2.6 2.6 2.6 1.2 —



Memory Reference Instruction Bit Assignments

GROUP 1 OPERATE MICROINSTRUCTIONS (1.2µsec)

GROUP 1 0 1 2 3 4 5 6 7 8 9 10 11 1 1 0 CLA CLL CMA CML RAR RAL 0 IAC	NOP CLA CLL CMA CML RAR RAL RTR RTL IAC BSW	7000 7200 7100 7040 7020 7010 7004 7012 7006 7001 7002		no operation clear AC clear link complement AC complement link rotate AC and link right one rotate AC and link right two rotate AC and link left two increment AC swap bytes in AC						Seq	uence 1 1 2 2 4 4 4 4 4 4
1 1 1 0 CLA CLL CMA CML RAR RAL 0 TAC											
	0 1	2	3	4	5	6	7	8	9	10	11
	1 1	1	0	CLA	CLL	СМА	CML			0	IAC

Logical Sequences:

BSW IF BITS 8 & 9 ARE 0

1—CLA, CLL 2—CMA, CML 3—IAC 4—RAR, RAL, RTR, RTL, BSW

Group 1 Operate Instruction Bit Assignments

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GROUP 2 OPERATE MICROINSTRUCTIONS (1.2µsec)

SMA SZA SPA SNA SNL SZL SKP OSR HLT CLA	. 2	7500 7440 7510 7450 7420 7430 7410 7404 7402 7600	skip on zero AC skip on plus AC skip on non-zero AC skip on non-zero Ink skip on zero link skip on zero link skip on zero link skip unconditionally inclusive OR, switch register with AC halts the program clear AC							Seq	uence 1 1 1 1 1 1 3 3 2
0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	SMA SPA	SZA SNA	SNL SZL	0	OSR	HLT	0

Logical Sequences:

1 (Bit 8 is Zero)—Either SMA or SZA or SNL 1 (Bit 8 is One)—Both SPA and SNA and SZL —CLA 3 —OSR, HLT

Group 2 Operate Instruction Bit Assignments

COMBINED OPERATE MICROINSTRUCTIONS (1.2µsec.)