Eric Tang

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EDUCATION

Cornell University, College of Engineering, Ithaca, NY **Expected May 2020**
Bachelor of Science, Electrical and Computer Engineering
Minor: Computer Science, Applied Mathematics
GPA: 3.88; Deans List, All semesters
Relevant Courses: Complex Digital ASIC Design, Distributed Computing, Computer Architecture, Digital Signal Processing, Large Scale Machine Learning, Numerical Analysis, Digital Communication

RESEARCH EXPERIENCE

Batten Research Group, Cornell University**,** *Undergraduate Researcher* **Aug. 2018-Present**

- Created 3 stage pipelined blocking cache generator parametrized by size of cache lines and total size
- Designed a custom energy and power characterization flow that utilizes Synopsys EDA tools (Primetime PX) to find performance metrics for custom ASIC designs
- Ran preliminary tests and created breakout board for computer architecture test chip (BRGTC1)

Computer Systems Laboratory, Cornell University**,** *Undergraduate Researcher* **Jun. 2017-Aug. 2017**

- Experimented with various forms of gradient descent on a GPU to filter spam emails more quickly
- Implemented stochastic gradient descent using multiple threads with asynchronous updates in C

ENGINEERING EXPERIENCE

Resistance Racing, Cornell University, *Electrical Subteam Lead* **Sep. 2017-Present**

- Designed and optimized an energy efficient BLDC motor controller using field-oriented control
- Designed, populated and tested a PCB for measuring power consumption (joulemeter)
- Tested and integrated battery management system, power converters, data acquisition, motor controller and automation systems onto the vehicle

MITRE, Bedford MA, *Position Navigation and Timing Intern* **May 2019-Aug. 2019**

- Identified spoofing in GPS signals from data collected during field tests
- Created plots and maps to visualize various aspects of GPS signals

Draper Laboratory, Cambridge MA, *Undergraduate Engineering Intern* **May 2018-Aug. 2018**

- Designed new test procedures and soldered custom test circuits to verify proper sensor functionality
- Automated tests utilizing oscilloscope, function generator, power sources and ammeters

ADDITIONAL EXPERIENCE

Non-Blocking Cache in 45nm ASIC, Complex ASIC Design Project **Jan. 2017-May. 2019**

- RTL design/synthesis of 3 stage pipelined non-blocking cache in Verilog and Synopsys, place and route in Cadence Innovus

Multi-Core Pipelined CPU, Computer Architecture Final Project **Oct. 2018-Dec. 2018**

- Designed quad-core pipelined processor with caches for RISC-V ISA using Verilog
- Performed cycle-level analysis and hardware/software co-design for multi-core parallel programs

OFDM System on Physical Wireline Channel, Digital Communications Final Project **Oct. 2018-Dec. 2018**

- Designed OFDM transmitter and receiver between PC soundcards with RLC filter that generates inter-symbol interference
- Explored time synchronization, channel estimation, modulation, power allocation, rate-adaptation, and channel coding

PUBLICATIONS & PRESENTATIONS

Y. Ou,.. **E. Tang**,… C. Batten (2019) *PyH2: A Property-Based Testing Framework for RTL Design Generators.* Manuscript submitted for publication

TEACHING

Teaching Assistant for Computer Architecture **Aug. 2019-Present**
ECE 2300 HKN Review Session **Apr. 2019**
Academic Excellence Workshop, Cornell University**,** *Multivariable Calculus* **Aug. 2017-Dec. 2017**

- Taught and created problem sets for a class of 15 students

CAMPUS INVOLVEMENT

Eta Kappa Nu (IEEE-HKN) **Nov. 2018-Present**
Tau Beta Pi **Nov. 2018-Present**
Club Swimming, Cornell University, *Member* **Sep. 2016-Present**

SPECIALIZED SKILLS

Programs: Altium, MATLAB, Python, Verilog, Java, Linux, C, C++, Verilator, VCS, PrimeTime, Autodesk