

Eric Tang

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5000 Forbes Ave, Hamerschlag Hall A313, Pittsburgh, PA 15213

EDUCATION	Carnegie Mellon University – Pittsburgh, PA Expected Graduation Dec. 2025 <i>Ph.D. Candidate in the Department of Electrical and Computer Engineering</i> <ul style="list-style-type: none">• Advisors: Prof. Franz Franchetti & Prof. James Hoe• Dean's Fellow, GPA 3.97• Relevant Coursework: Modern Computer Architecture & Design, Digital IC Design, Reconfigurable Computing, How to Write Fast Code
	Cornell University – Ithaca, NY May 2020 <i>Bachelor of Science in Electrical and Computer Engineering, Computer Science Minor</i> <ul style="list-style-type: none">• Dean's List, Magna Cum Laude, GPA 3.88• Honors: Eta Kappa Nu (IEEE-HKN), Tau Beta Pi• Relevant Coursework: Complex Digital ASIC Design, Distributed Computing, Computer Architecture, Large Scale Machine Learning, Digital Communication
SKILLS	Programming Languages: Verilog, C, C++, MATLAB, Python, Java, TCL, PyMTL3 Tools: Git, Altium, Verilator, VCS, Primetime PX, Cadence Innovus & Virtuoso
RESEARCH EXPERIENCE	Carnegie Mellon University – Pittsburgh, PA Aug. 2020 – Present <i>Graduate Student Researcher, Advised by Prof. Franz Franchetti and Prof. James Hoe</i> <ul style="list-style-type: none">• Exploring reactive programming model for near data processing on CPU-FPGA systems and other architectures with shared memory.• Prototyped this model with PageRank application on Intel DevCloud using DPC++ and on a local CPU-FPGA system in Verilog.• Working on creating hardware simulation of the end-to-end system to allow for faster exploration of other potential applications.
	Batten Research Group – Cornell University Aug. 2018 – May 2020 <i>Undergraduate Researcher Advised by Prof. Christopher Batten</i> <ul style="list-style-type: none">• Created 3 stage pipelined blocking cache generator parametrized by cache line size and total size.• Designed a custom energy and power characterization flow that utilizes Synopsys EDA tools (Primetime PX) to find performance metrics for custom ASIC designs.• Ran preliminary tests and created a breakout board for computer architecture test chip (BRGTC1).
	Computer Systems Laboratory – Cornell University Jun. 2017 – Aug. 2017 <i>Undergraduate Researcher Advised by Prof. Zhiru Zhang</i> <ul style="list-style-type: none">• Implemented a parallel stochastic gradient descent with asynchronous updates in C .
	Lawrence Berkeley National Laboratory – Berkeley, CA May 2023 – Aug. 2023 <i>Graduate Research Intern</i> <ul style="list-style-type: none">• Devised graph-centric RISC-V ISA extensions (GISA) for tiled architecture.• Implemented and tested GISA in Verilog for Triangle Counting with the SNAP dataset.
PROFESSIONAL EXPERIENCE	MITRE – Bedford, MA May 2019 – Aug. 2019 <i>Position Navigation and Timing Intern</i> <ul style="list-style-type: none">• Identified spoofing in GPS signals from data collected during field tests.• Created plots and maps to visualize various aspects of GPS signals.

Draper Laboratory – Cambridge, MA**May 2018 – Aug. 2018***Undergraduate Engineering Intern*

- Designed new test procedures and soldered custom test circuits to verify proper sensor functionality.
- Automated tests utilizing oscilloscope, function generator, power sources, etc.

PUBLICATIONS

A. Li, ... , **E. Tang**, ... , C. Batten, and D. Wentzlaff. "CIFER: A Cache-Coherent 12nm 16mm² SoC with Four 64-bit RISC-V Application Cores, 18 32-bit RISC-V Compute Cores, and a 1541 LUT6/mm² Synthesizable eFPGA." *IEEE Solid-State Circuits Letters (SSCL)*, Aug. 2023.

T. Chang*, A. Li*, ..., **E. Tang**, ..., C. Batten, and D. Wentzlaff. "CIFER: A 12nm, 16mm², 22-Core SoC with a 1541 LUT6/mm², 1.92 MOPS/LUT, Fully Synthesizable, Cache- Coherent, Embedded FPGA." *IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2023.

E. Tang, F. Franchetti. "Magic Memory: A Programming Model for Big Data Analytics." *IEEE High Performance Extreme Computing Conference (HPEC)*, 2022, Poster with extended abstract

Z. Gong, N. Zhu, M. Ngaw, J. Rivera, L. Tang, **E. Tang**, H. Mankad, F. Franchetti. "Interval Arithmetic-based FFT for Large Integer Multiplication." *IEEE High Performance Extreme Computing Conference (HPEC)*, 2022, Poster with extended abstract

TEACHING**Computational Problem Solving for Engineers [18-647]****Jan. 2024 –May 2024***Teaching Assistant*

- Led weekly recitations, graded homeworks, and held weekly office hours.

How to Write Fast Code [18-645]**Aug. 2023 – Dec. 2023***Teaching Assistant*

- Graded assignments and held weekly office hours.

Computer Architecture [ECE 4750]**Aug. 2019 – Dec. 2019***Teaching Assistant*

- Graded labs, problem sets, and quizzes and held weekly office hours.

Digital Logic & Computer Organization [ECE 2300]**Apr. 2019***HKN Volunteer*

- Led exam review session for over 20 students.

Multivariable Calculus [MATH 1920]**Aug. 2017 – Dec. 2017***Academic Excellence Workshop Facilitator*

- Taught and created problem sets for a class of 15 students.

ACTIVITIES**Cornell Electric Vehicles – Cornell University****Sep. 2017 – May 2020***Electrical Subteam Lead*

- Designed and optimized an energy-efficient BLDC motor controller using field-oriented control.
- Designed, populated, and tested a PCB for measuring power consumption (joulemeter)
- Tested and integrated battery management system, power converters, data acquisition, motor controller, and automation systems onto the vehicle