Large-Scale Reconfigurable Digital Neuromorphic Architecture

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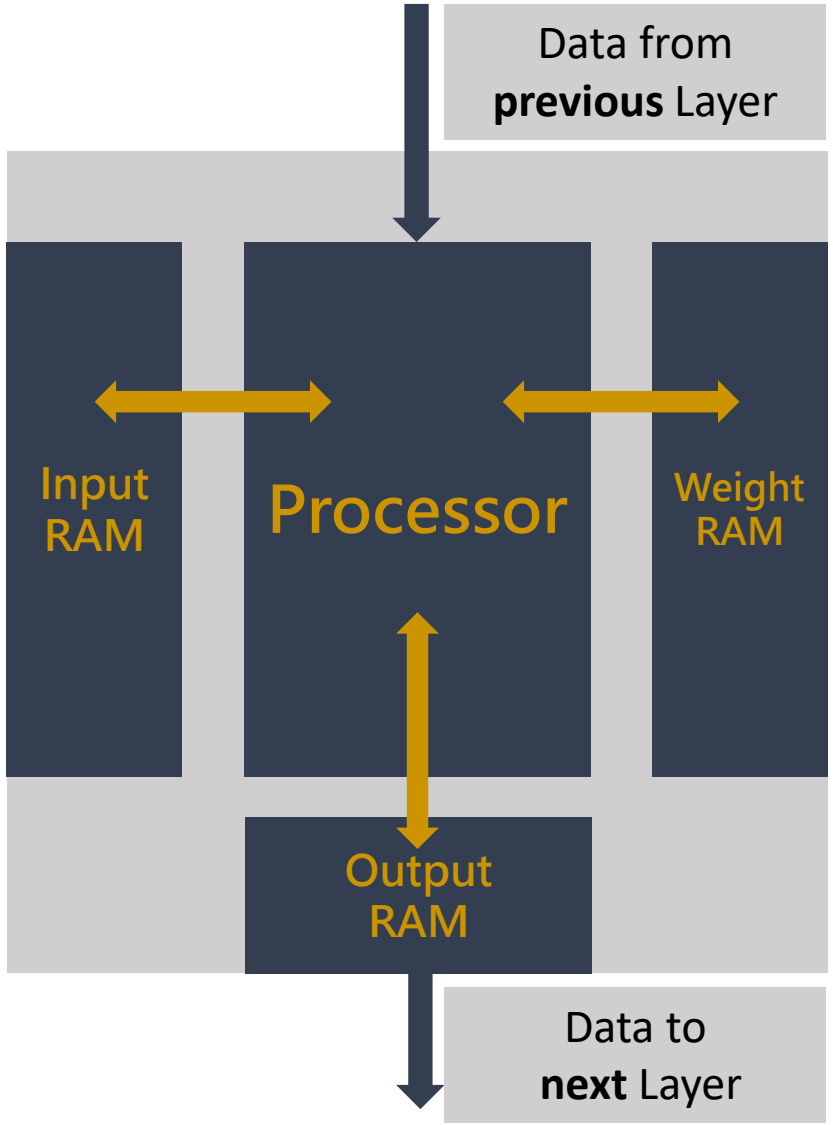
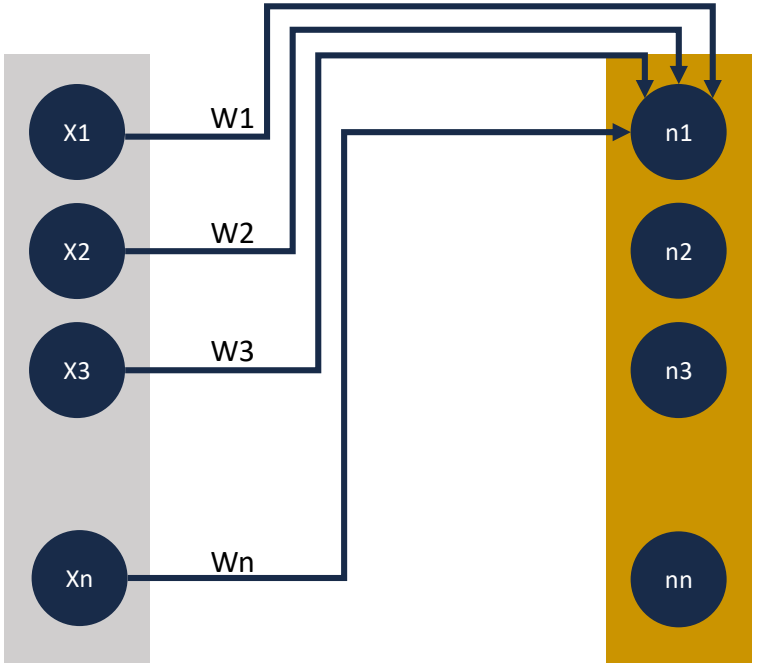
UCSD Summer Intern Research Program

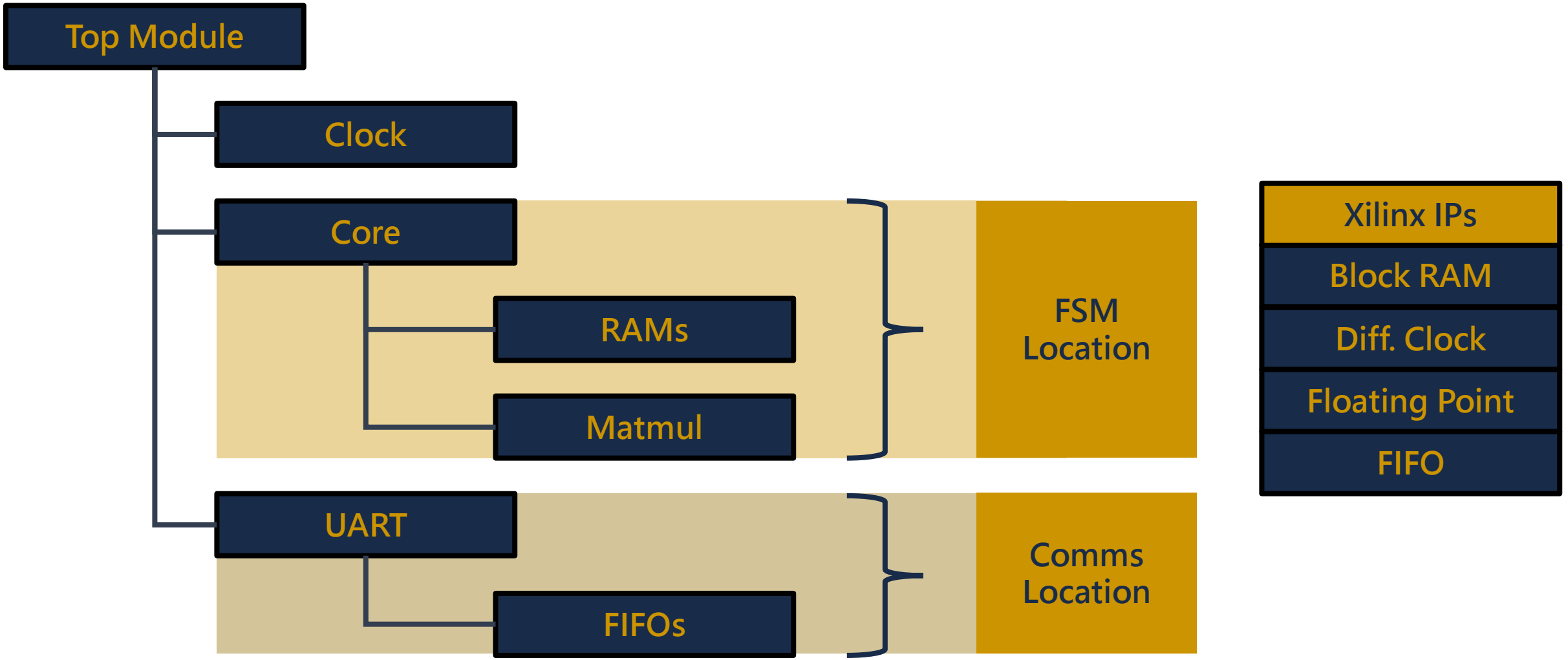
Core of the Project



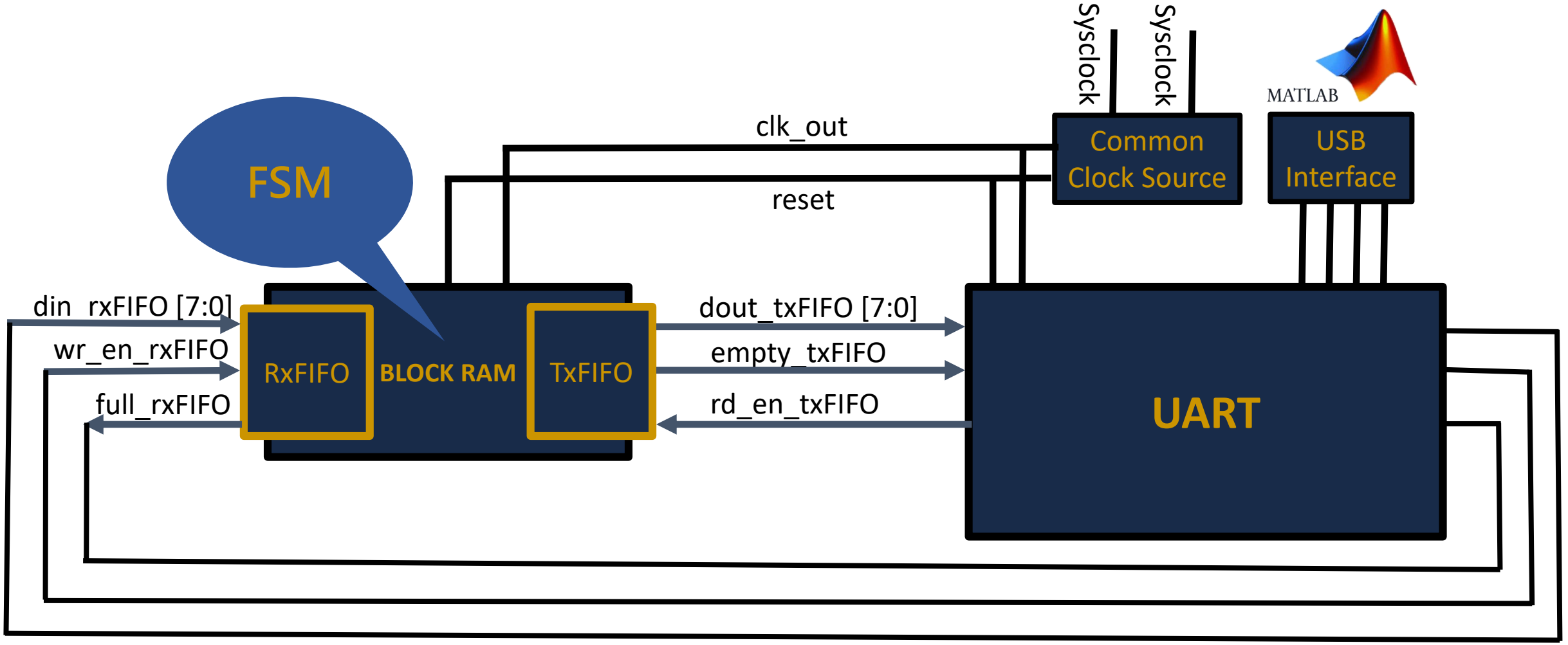


- Emulate layer of the network
  - Read Weight info from Weight RAM
  - Load input from Input Ram
  - Process data as perceptron

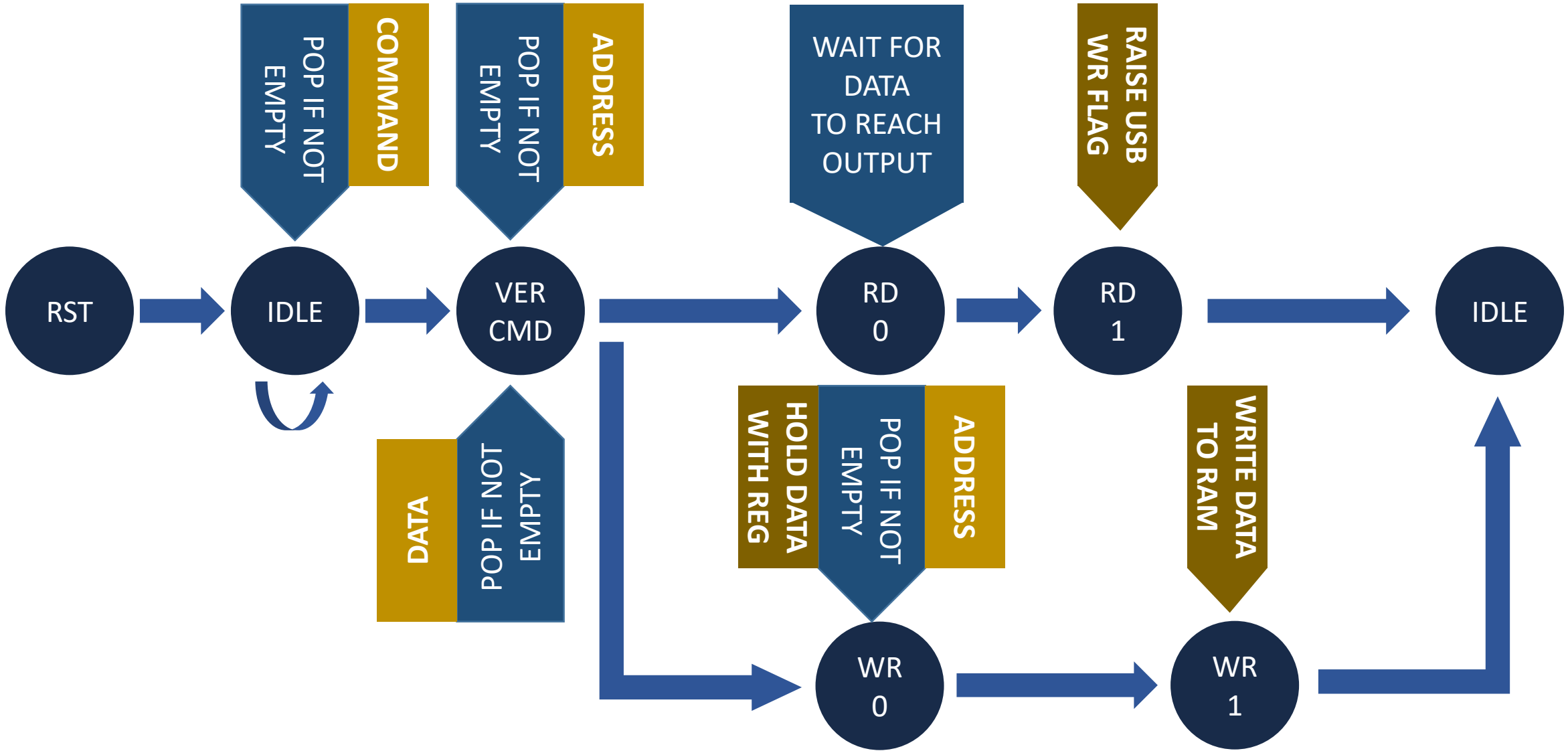
Project Hierarchy



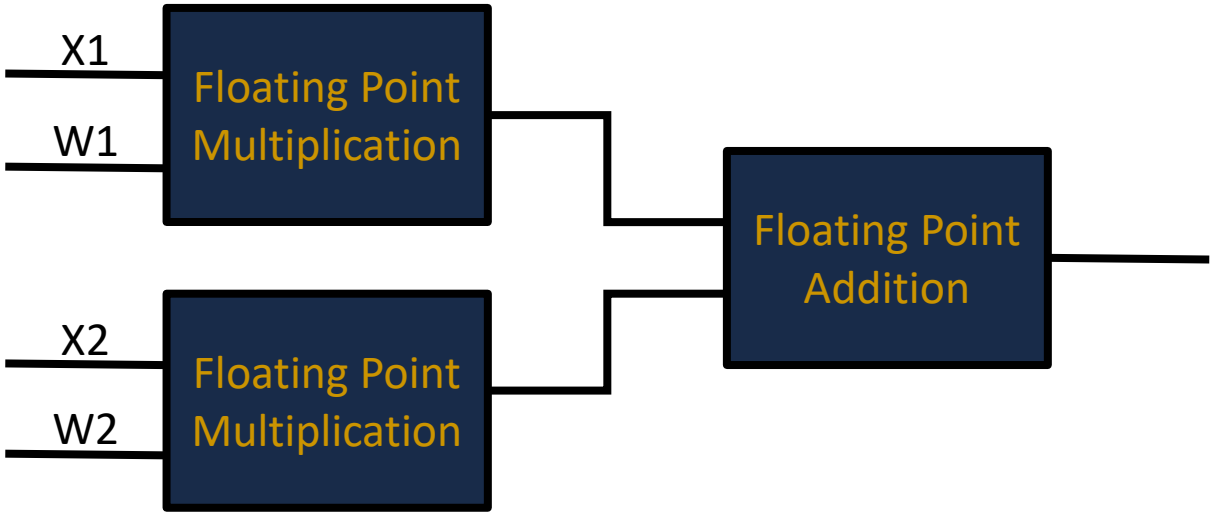
Submodule Read/Write Memory

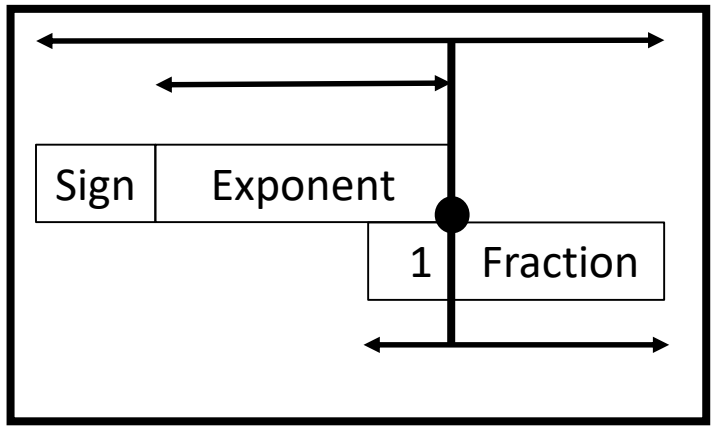


Topology of Read/Write Process

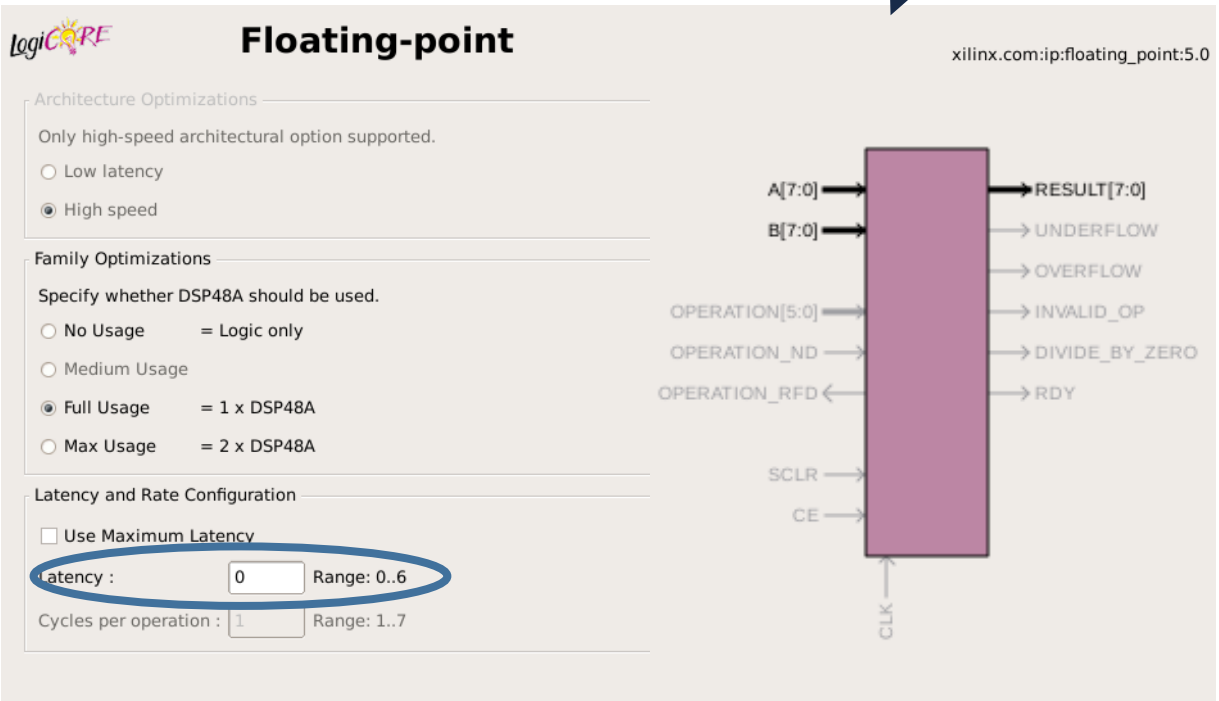


Submodule Dot Product Module/Process

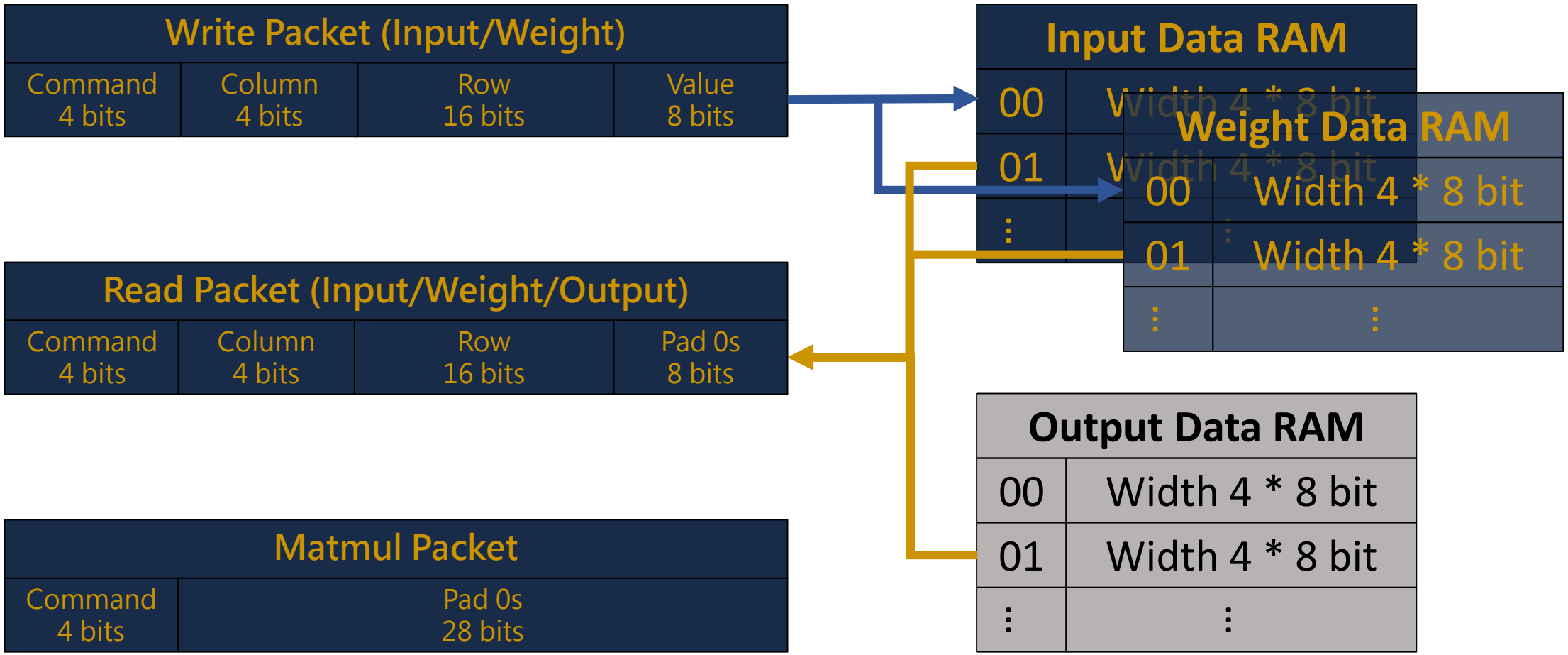




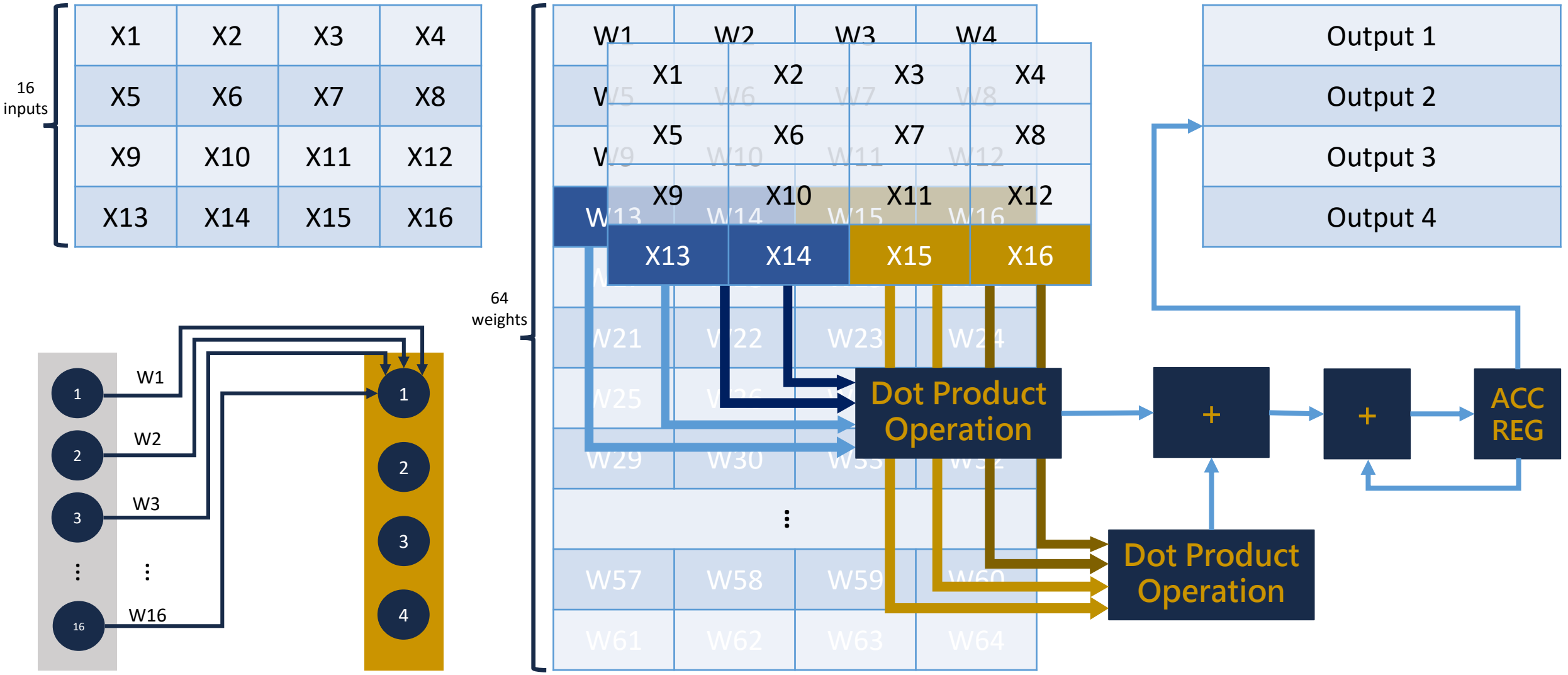
Xilinx IP Generator



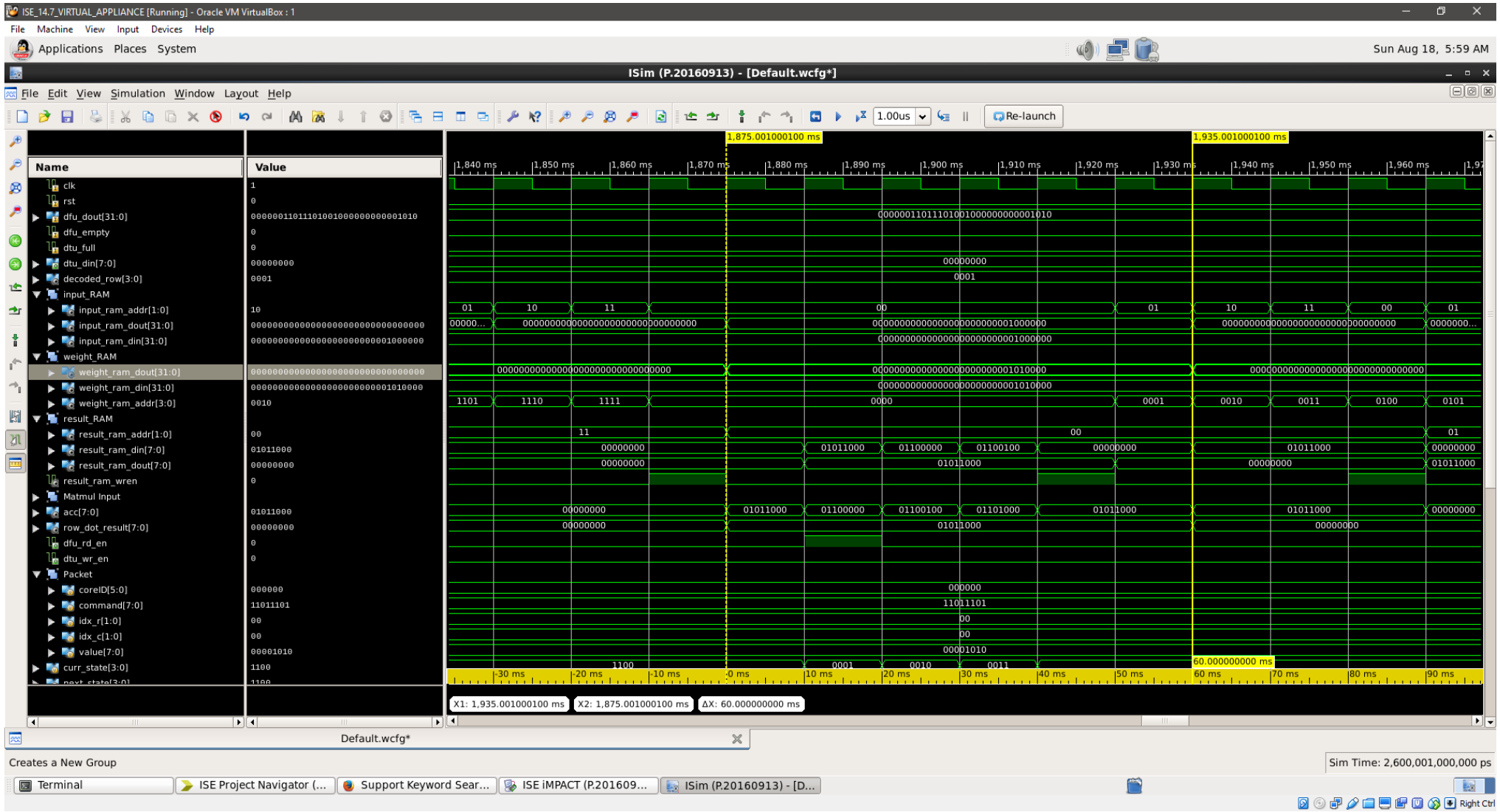
Information Transfer Packet



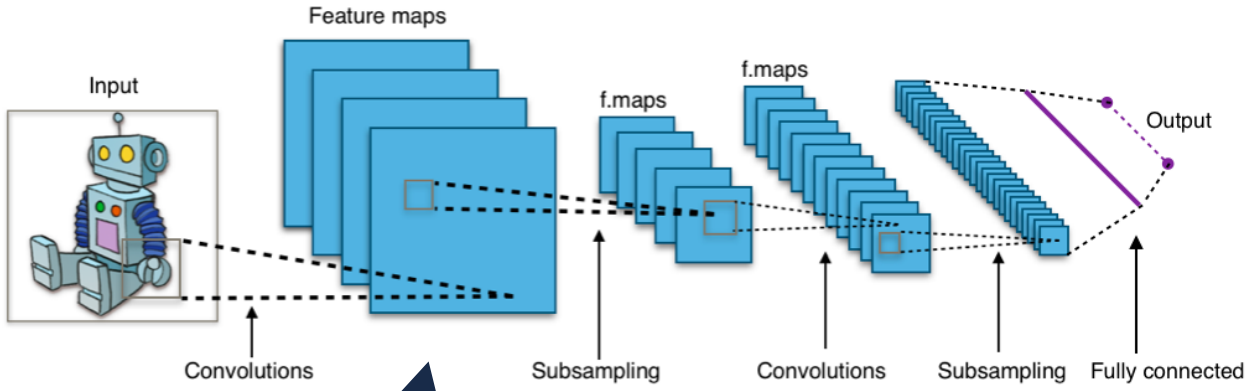
Simple Implementation



Simple Implementation Simulation

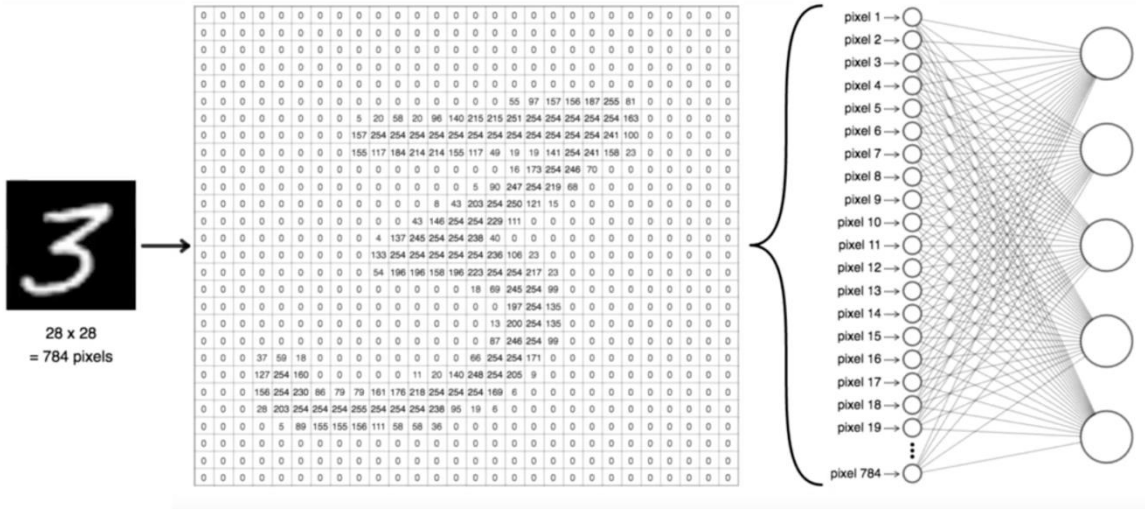


Future Extensions



Convolution Nets

Large Scale ANNs



Acknowledgments