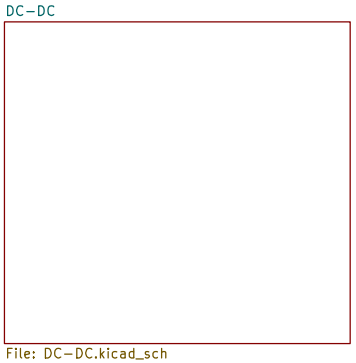
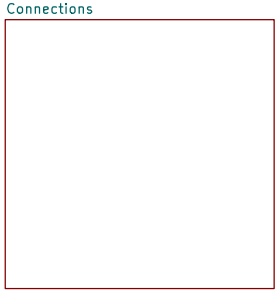
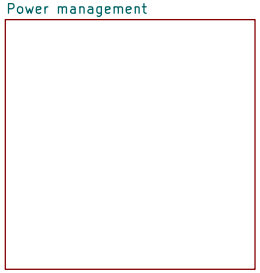
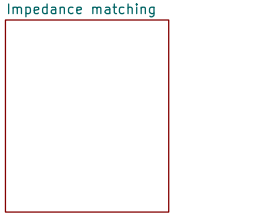

STM32
File: STM32.kicad_sch

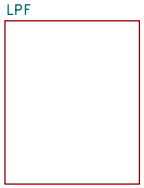

DC-DC
File: DC-DC.kicad_sch

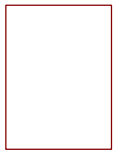

Connections
File: Connections.kicad_sch

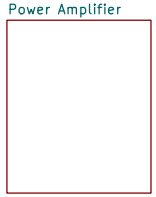

Power management
File: Power_Management.kicad_sch

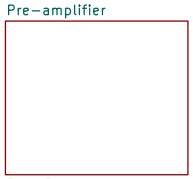

H1
MountingHole
H2
MountingHole
H3
MountingHole

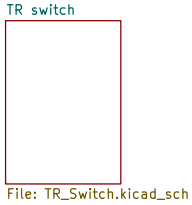

Impedance matching
File: Impedance_matching.kicad_sch

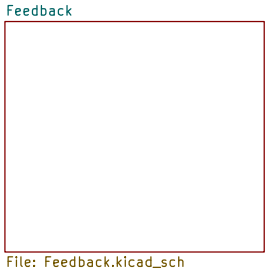

LPF
File: LPF.kicad_sch

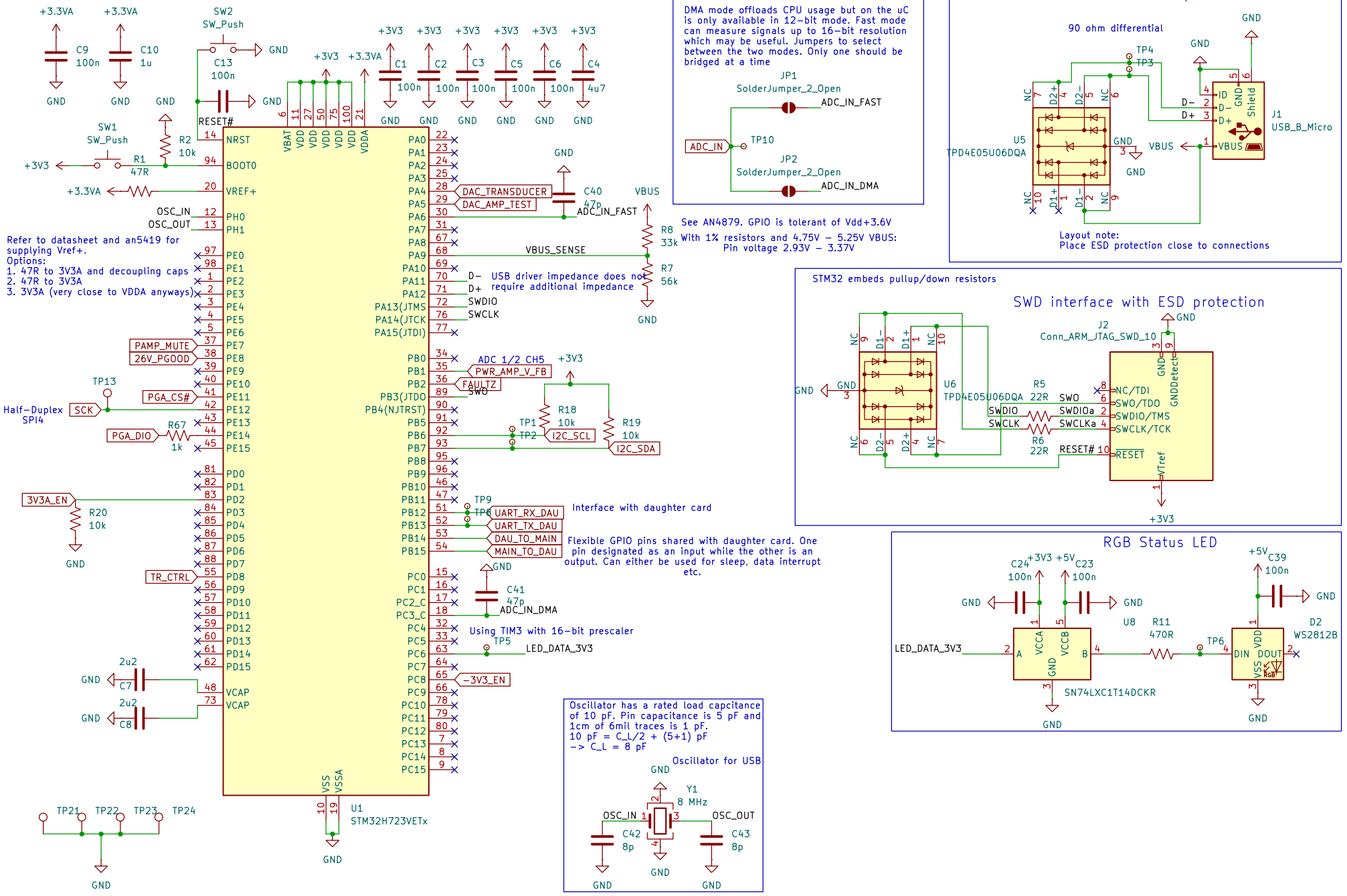

PGA
File: PGA.kicad_sch

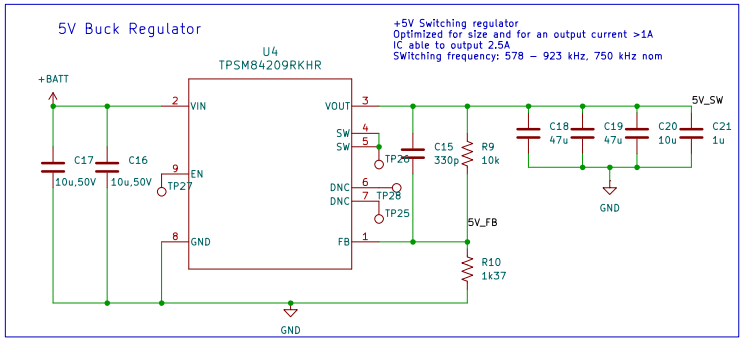

Power Amplifier
File: Power_amplifier.kicad_sch

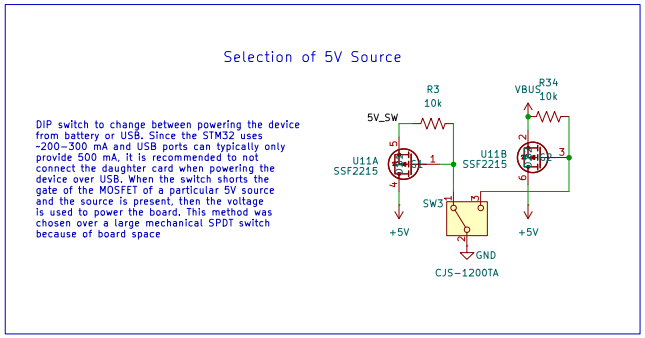

Pre-amplifier
File: Pre-amp.kicad_sch

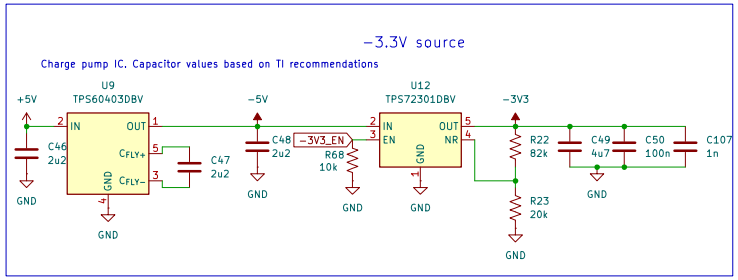

TR switch
File: TR_Switch.kicad_sch

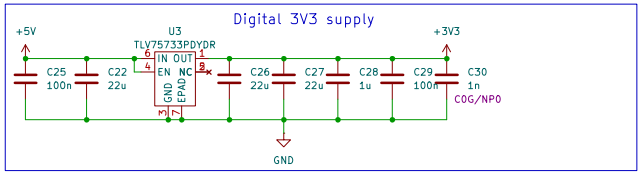

Feedback
File: Feedback.kicad_sch

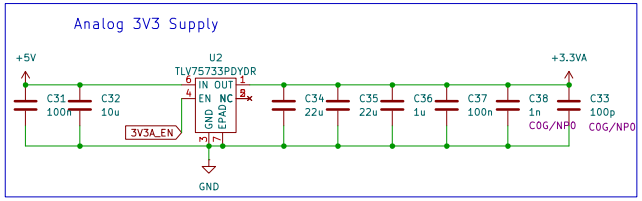

+3.3VA
C9
100n
C10
1u
GND
SW2
SW_Push
C13
100n
RESET#
SW1
SW_Push
R2
10k
R1
47R
+3V3
BOOT0
VREF+
+3.3VA
OSC_IN
OSC_OUT
PH0
PH1
Refer to datasheet and an5419 for supplying Vref+.
Options:
1. 47R to 3V3A and decoupling caps
2. 47R to 3V3A
3. 3V3A (very close to VDDA anyways)
PAMP_MUTE
26V_PGOOD
PGA_CS#
PGA_DIO
R67
1k
TP13
SCK
Half-Duplex SPI4
3V3A_EN
R20
10k
TR_CTRL
2u2
C7
C8
TP21
TP22
TP23
TP24
U1
STM32H723VETx
VBAT
VDD
VDDA
VSS
VSSA
NRST
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PA8
PA9
PA10
PA11
PA12
PA13(JTMS
PA14(JTCK
PA15(JTDI)
PB0
PB1
PB2
PB3(JTDO
PB4(NJTRST)
PB5
PB6
PB7
PB8
PB9
PB10
PB11
PB12
PB13
PB14
PB15
PC0
PC1
PC2_C
PC3_C
PC4
PC5
PC6
PC7
PC8
PC9
PC10
PC11
PC12
PC13
PC14
PC15
PE0
PE1
PE2
PE3
PE4
PE5
PE6
PE7
PE8
PE9
PE10
PE11
PE12
PE13
PE14
PE15
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PD8
PD9
PD10
PD11
PD12
PD13
PD14
PD15
VCAP
C1
C2
C3
C5
C6
C4
100n
4u7
C40
47p
ADC_IN_FAST
DAC_TRANSDUCER
DAC_AMP_TEST
VBUS
R8
33k
R7
56k
VBUS_SENSE
D-
D+
USB driver impedance does not require additional impedance
SWDIO
SWCLK
ADC 1/2 CH5
PWR_AMP_V_FB
FAULTZ
SWO
R18
10k
R19
10k
TP1
TP2
I2C_SCL
I2C_SDA
TP9
TP8
UART_RX_DAU
UART_TX_DAU
DAU_TO_MAIN
MAIN_TO_DAU
Interface with daughter card
Flexible GPIO pins shared with daughter card. One pin designated as an input while the other is an output. Can either be used for sleep, data interrupt etc.
C41
47p
ADC_IN_DMA
Using TIM3 with 16-bit prescaler
TP5
LED_DATA_3V3
-3V3_EN
DMA mode offloads CPU usage but on the uC is only available in 12-bit mode. Fast mode can measure signals up to 16-bit resolution which may be useful. Jumpers to select between the two modes. Only one should be bridged at a time
JP1
SolderJumper_2_Open
ADC_IN_FAST
ADC_IN
TP10
JP2
SolderJumper_2_Open
ADC_IN_DMA
See AN4879. GPIO is tolerant of Vdd+3.6V
With 1% resistors and 4.75V – 5.25V VBUS:
Pin voltage 2.93V – 3.37V
USB-B-Micro connection with ESD protection
90 ohm differential
TP4
TP3
U5
TPD4E05U06DQA
J1
USB_B_Micro
ID
D-
D+
Shield
VBUS
Layout note:
Place ESD protection close to connections
STM32 embeds pullup/down resistors
SWD interface with ESD protection
J2
Conn_ARM_JTAG_SWD_10
U6
TPD4E05U06DQA
R5
22R
R6
22R
SWO
SWDIO
SWCLK
RESET#
SWDIOa
SWCLKa
NC/TDI
SWO/TDO
SWDIO/TMS
SWCLK/TCK
RESET
VTref
GNDDetect
RGB Status LED
C24
100n
C23
100n
C39
100n
U8
SN74LXC1T14DCKR
R11
470R
D2
WS2812B
LED_DATA_3V3
TP6
DIN
DOUT
VDD
VSS
Oscillator has a rated load capcitance of 10 pF. Pin capacitance is 5 pF and 1cm of 6mil traces is 1 pF.
10 pF = C_L/2 + (5+1) pF
-> C_L = 8 pF
Oscillator for USB
Y1
8 MHz
C42
8p
C43
8p
OSC_IN
OSC_OUT





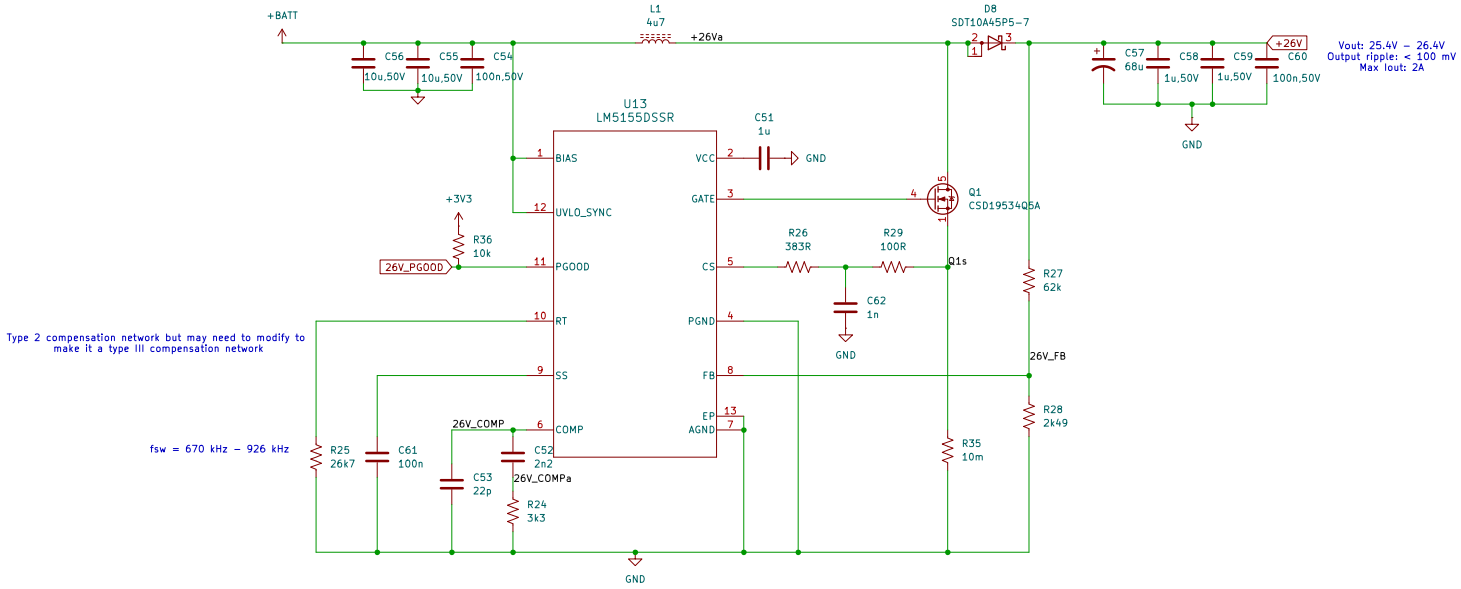




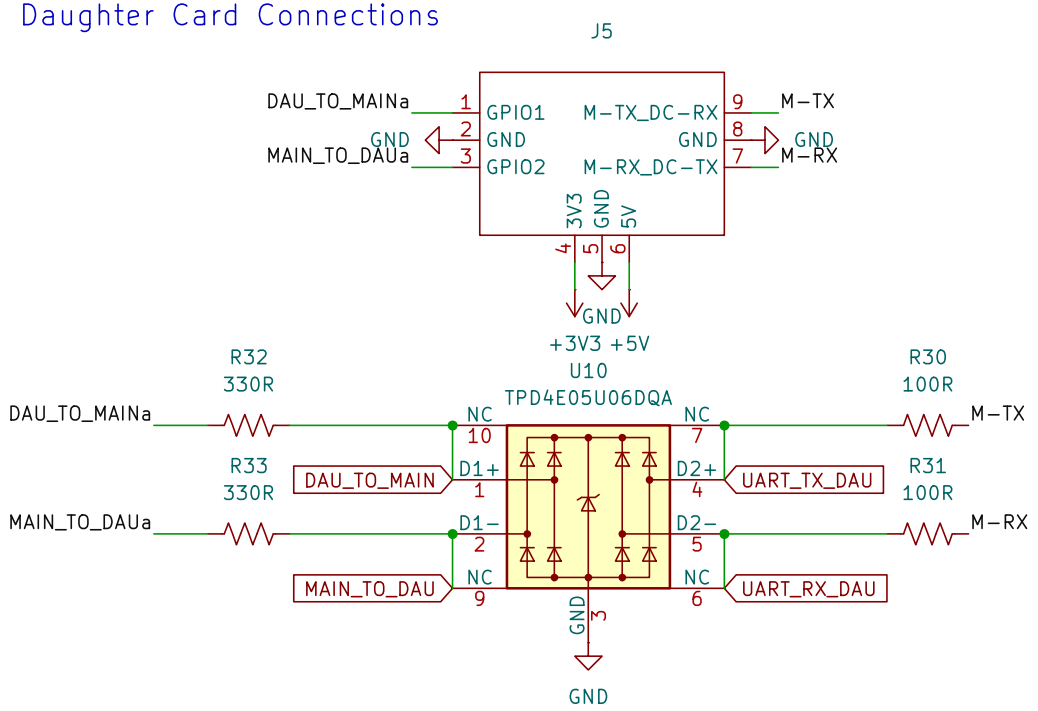


TLV75733 Specs:
Iout: 1A
Vout: 3.3V
Minimum input/output capacitance: 1 uF
Line regulation: 0.06%
Load regulation: 2.1% over 0.1mA – 1A. Since this is a linear relation (Fig 5–13) and the analog circuit uses < 50 mA I am not worried about this impacting analog performance.
PSRR: -40 dB @ 700 kHz, C_out=45 uF, Vin=5V
I am slightly concerned about temeprature performance at low temperatures, however, as the temperature will spike when transmitting which could cause fluctuations in the output voltage

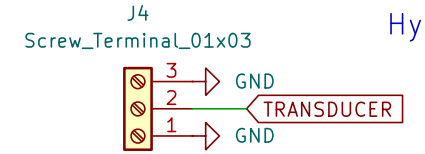
https://webench.ti.com/appinfo/webench/scripts/SDP.cgi?ID=53DFB0B1AD9BCCBB



Daughter Card Connections



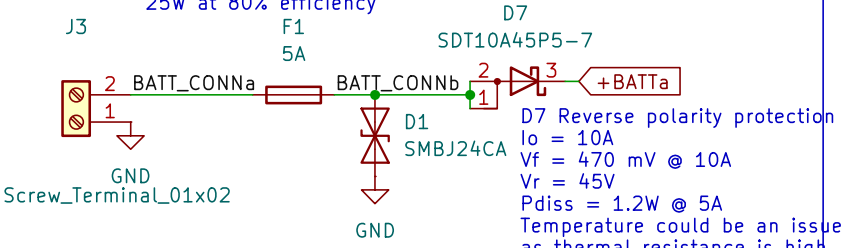
Hydrophone Connections



Hydrophone pinout:
1: Negative
2: Positive
3: Shield
https://geospectrum.ca/wp-content/uploads/2022/05/SP-M18C-1.5-R0.pdf

Battery Connection

5A fuse in case minimum voltage of 8V is applied and power amplifier outputs 25W at 80% efficiency



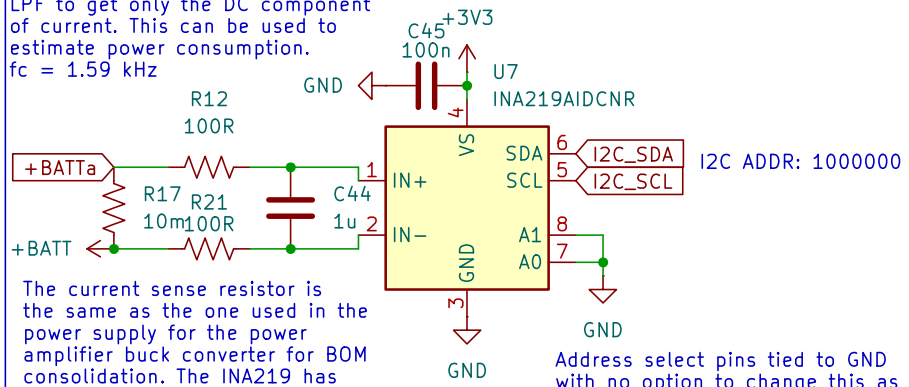
D7 Reverse polarity protection
Io = 10A
Vf = 470 mV @ 10A
Vr = 45V
Pdiss = 1.2W @ 5A
Temperature could be an issue as thermal resistance is high

D1 TVS protection in case of voltage spikes from inductive devices being disconnected since the battery is shared

Power Consumption

Voltage and current sense IC used to detect the amount of power used by all of the electronics. Not strictly necessary for any design requirements, but useful for debugging issues and for testing future implementations in low power applications.

LPF to get only the DC component of current. This can be used to estimate power consumption.
fc = 1.59 kHz

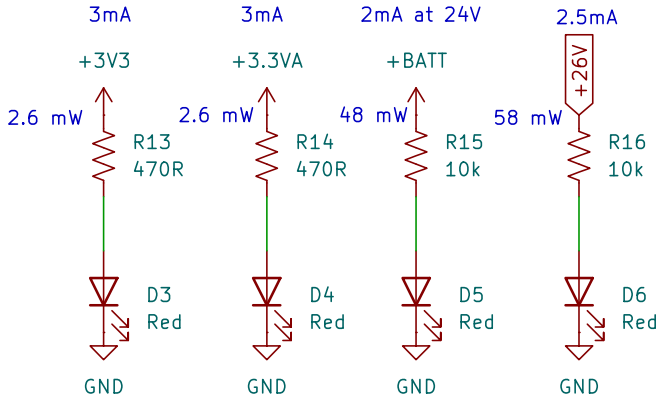


I2C ADDR: 1000000

The current sense resistor is the same as the one used in the power supply for the power amplifier buck converter for BOM consolidation. The INA219 has programmable gain which makes it flexible across different current loads.

Address select pins tied to GND with no option to change this as the I2C interface is not broken out outside of the PCB and this is the only I2C device

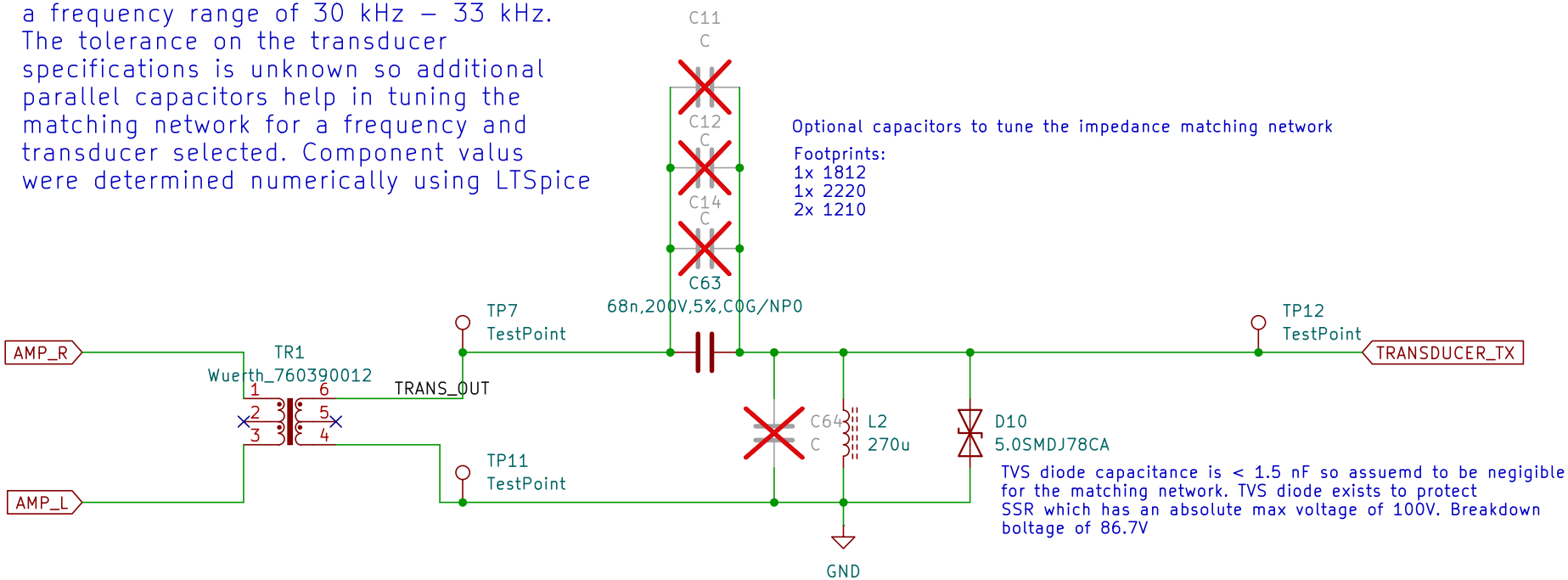
Power Good Indicators



If LEDs too bright, replace with 1k/20k resistors

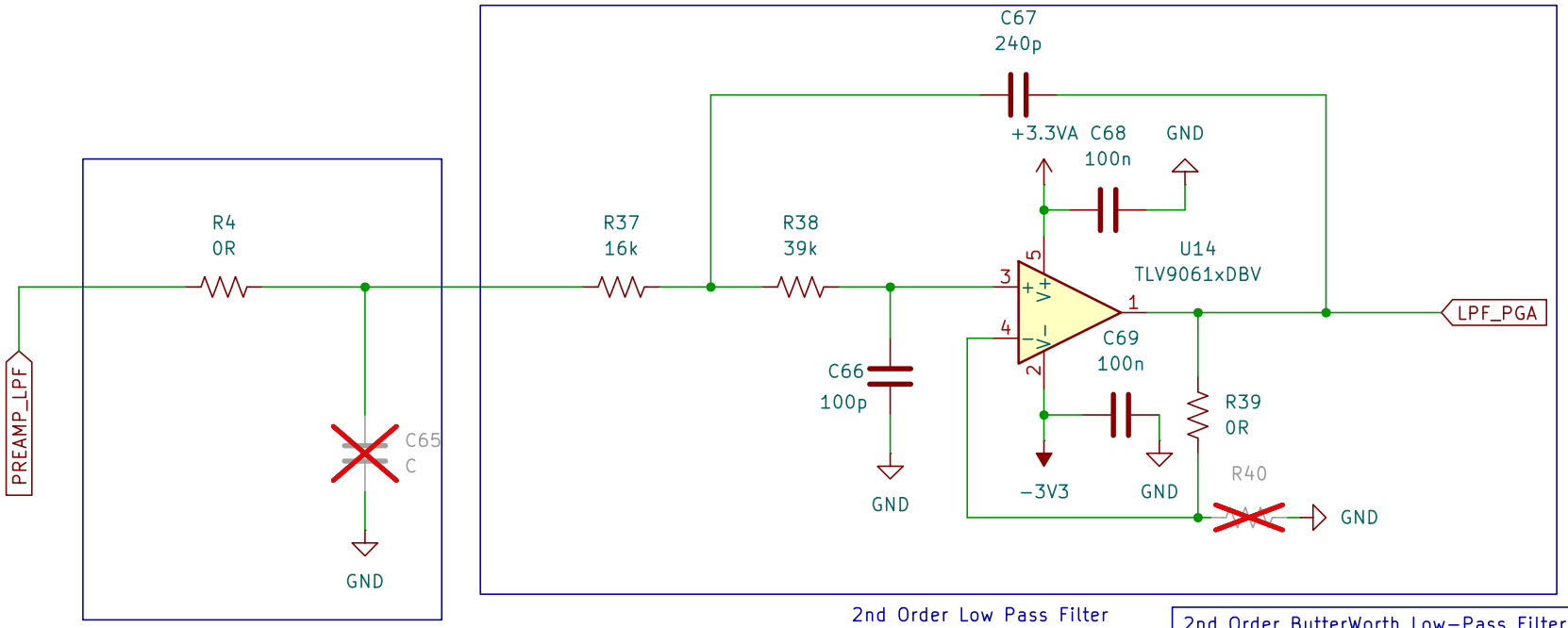
Impedance Matching Network Between Power Amplifier and Transducer

LTSpice simulations show a power factor > 0.75 across component tolerances and a frequency range of 30 kHz – 33 kHz. The tolerance on the transducer specifications is unknown so additional parallel capacitors help in tuning the matching network for a frequency and transducer selected. Component valus were determined numerically using LTSpice



Note:
Only use ceramic capacitors with a C0G/NP0 dielectric for stability over voltage and temperature as this is very sensitive to component values

Low-Pass Filter



High Pass Filter

2nd Order Low Pass Filter

Notes on High Pass:
- Not as effective at attenuation as 2nd order LPF
- Can be included, but only for keeping f >21kHz
- Can be easily replaced by an earlier Shunt Capacitor

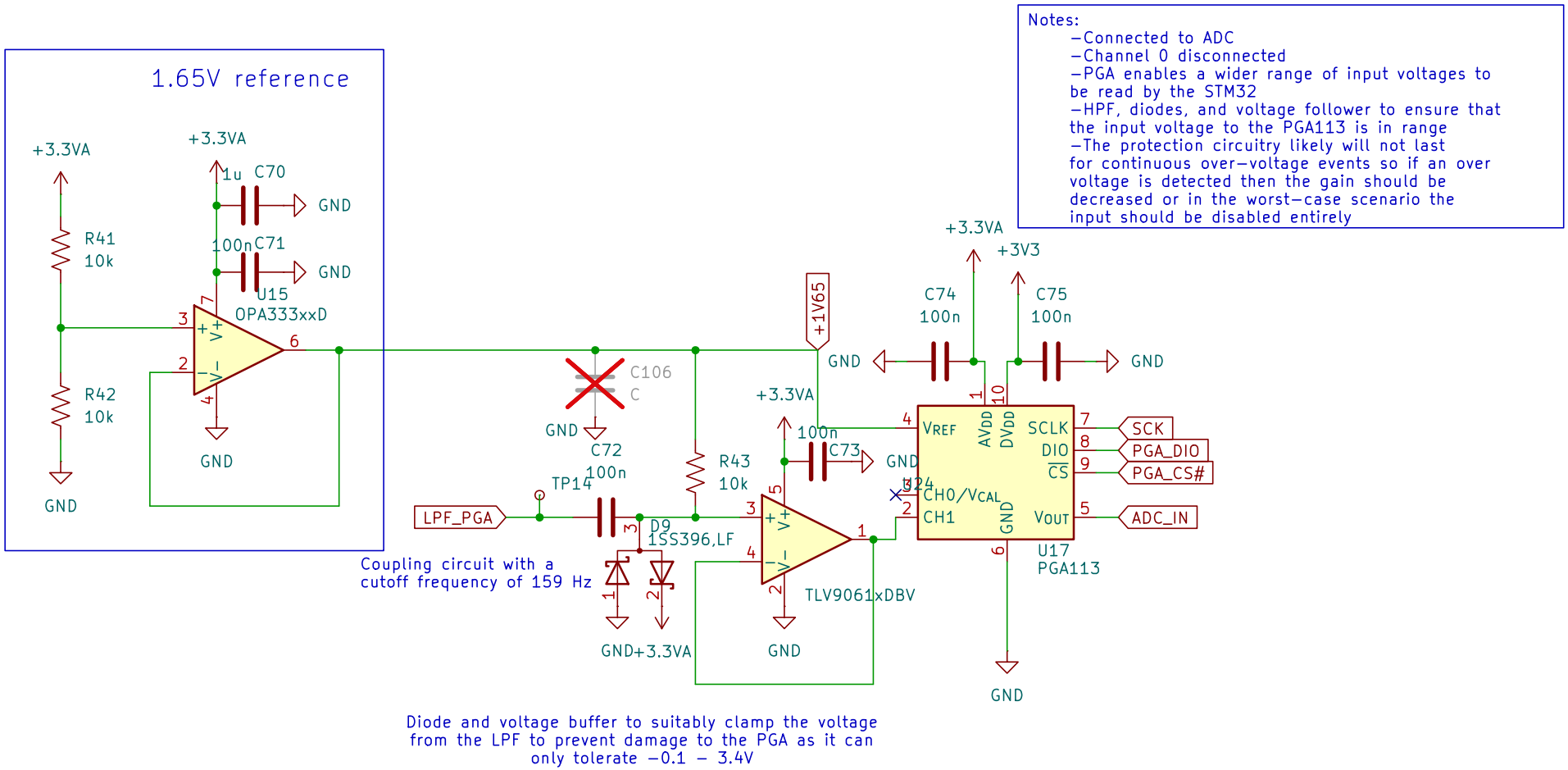
2nd Order ButterWorth Low-Pass Filter
Positive Feedback

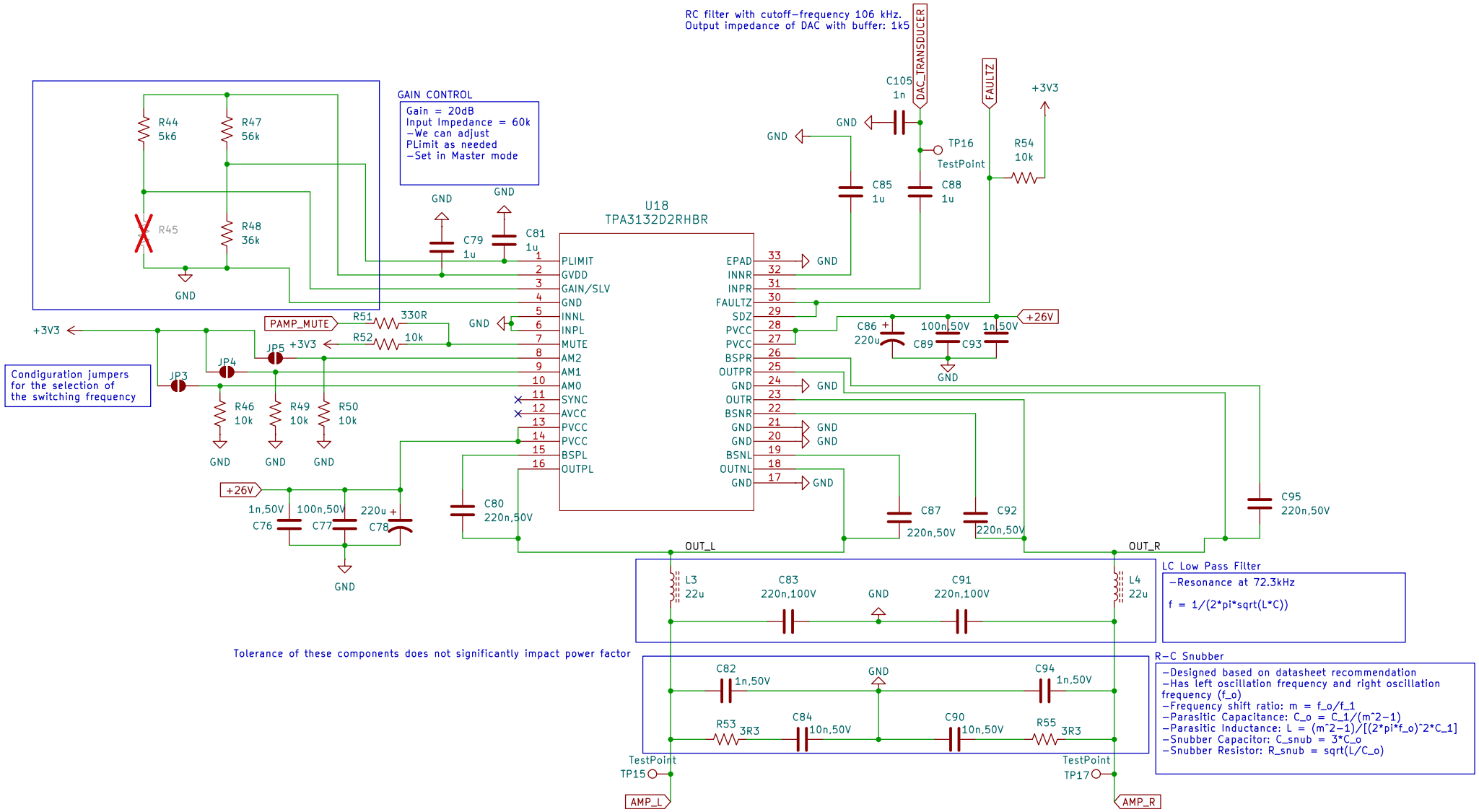
Gain: 0dB or 1 V/V
Works up to 5MHz

Set for 40kHz for frequency cutoff

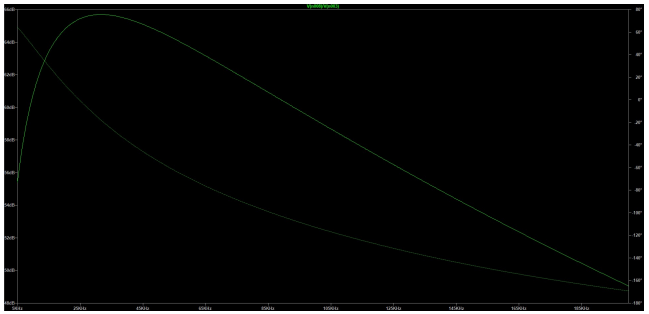
Means to cut off high frequency but not change the Gain

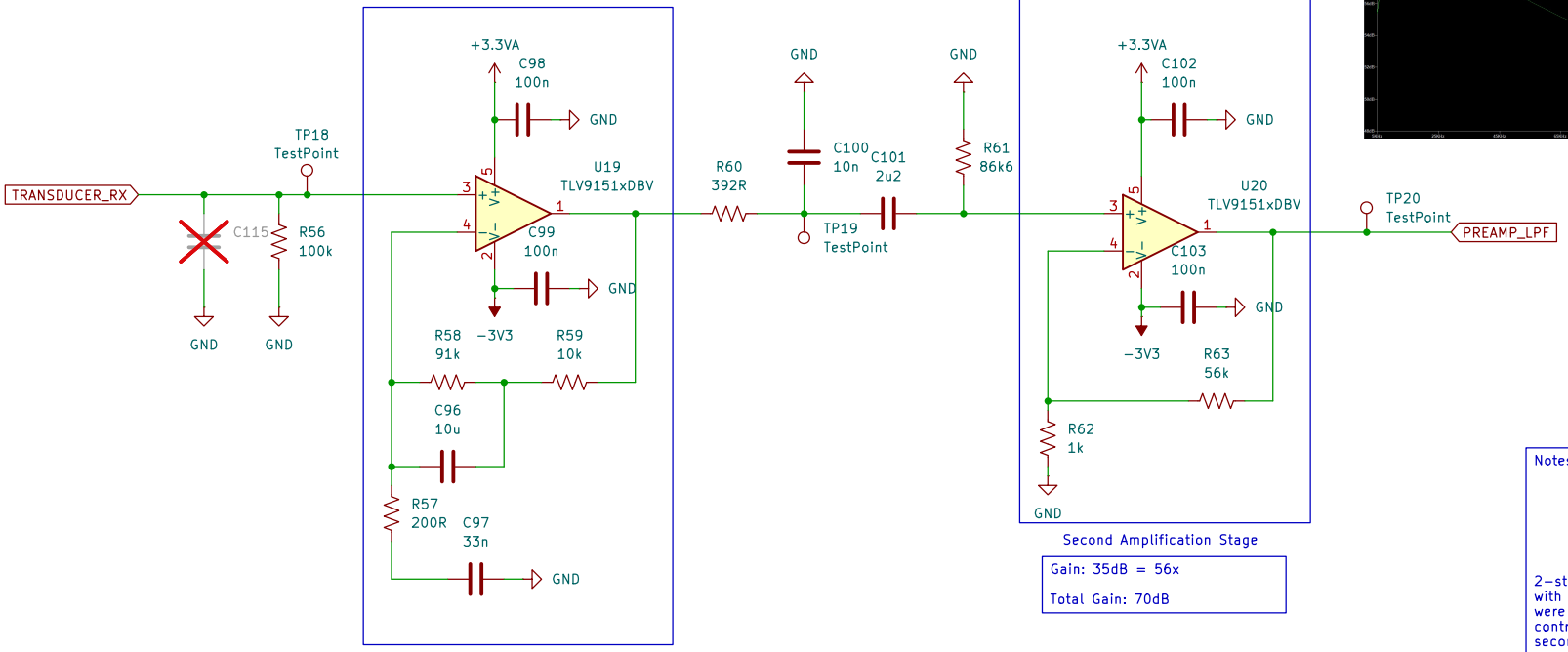
Calculations for Resistors and Capacitors:
https://k7mem.com/Fil_2nd_Active_LP_HP.html


Notes:
−Connected to ADC
−Channel 0 disconnected
−PGA enables a wider range of input voltages to be read by the STM32
−HPF, diodes, and voltage follower to ensure that the input voltage to the PGA113 is in range
−The protection circuitry likely will not last for continuous over−voltage events so if an over voltage is detected then the gain should be decreased or in the worst−case scenario the input should be disabled entirely
1.65V reference
+3.3VA
R41
10k
R42
10k
GND
+3.3VA
1u C70
GND
100n C71
GND
U15
OPA333xxD
GND
C106
C
GND
C72
100n
+1V65
GND
+3.3VA
C74
100n
+3V3
C75
100n
GND
+3.3VA
100n
C73
GND
R43
10k
TP14
LPF_PGA
D9
1SS396,LF
Coupling circuit with a cutoff frequency of 159 Hz
GND+3.3VA
GND
TLV9061xDBV
U24
CH0/VCAL
CH1
VREF
AVDD
DVDD
SCLK
DIO
CS
VOUT
GND
SCK
PGA_DIO
PGA_CS#
ADC_IN
U17
PGA113
GND
Diode and voltage buffer to suitably clamp the voltage from the LPF to prevent damage to the PGA as it can only tolerate −0.1 − 3.4V


RC filter with cutoff-frequency 106 kHz.
Output impedance of DAC with buffer: 1k5
DAC_TRANSDUCER
FAULTZ
+3V3
C105
1n
GND
TP16
TestPoint
R54
10k
C85
1u
C88
1u
GAIN CONTROL
Gain = 20dB
Input Impedance = 60k
-We can adjust
PLimit as needed
-Set in Master mode
R44
5k6
R47
56k
R45
R48
36k
GND
C79
1u
C81
1u
U18
TPA3132D2RHBR
PLIMIT
GVDD
GAIN/SLV
GND
INNL
INPL
MUTE
AM2
AM1
AM0
SYNC
AVCC
PVCC
PVCC
BSPL
OUTPL
EPAD
INNR
INPR
FAULTZ
SDZ
PVCC
PVCC
BSPR
OUTPR
GND
OUTR
BSNR
GND
GND
BSNL
OUTNL
GND
PAMP_MUTE
R51
330R
R52
10k
+3V3
JP5
JP4
JP3
Condiguration jumpers
for the selection of
the switching frequency
R46
10k
R49
10k
R50
10k
C86
220u
100n,50V
C89
1n,50V
C93
+26V
C80
220n,50V
C87
220n,50V
C92
220n,50V
C95
220n,50V
1n,50V
C76
100n,50V
C77
220u
C78
OUT_L
OUT_R
L3
22u
C83
220n,100V
C91
220n,100V
L4
22u
LC Low Pass Filter
-Resonance at 72.3kHz
f = 1/(2*pi*sqrt(L*C))
Tolerance of these components does not significantly impact power factor
C82
1n,50V
C94
1n,50V
R53
3R3
C84
10n,50V
C90
10n,50V
R55
3R3
R-C Snubber
-Designed based on datasheet recommendation
-Has left oscillation frequency and right oscillation frequency (f_o)
-Frequency shift ratio: m = f_o/f_1
-Parasitic Capacitance: C_o = C_1/(m^2-1)
-Parasitic Inductance: L = (m^2-1)/[(2*pi*f_o)^2*C_1]
-Snubber Capacitor: C_snub = 3*C_o
-Snubber Resistor: R_snub = sqrt(L/C_o)
TestPoint
TP15
TestPoint
TP17
AMP_L
AMP_R

Simulations show slightly less gain (65.5 dB at 30 kHz) than expected likely due to the filters on each stage



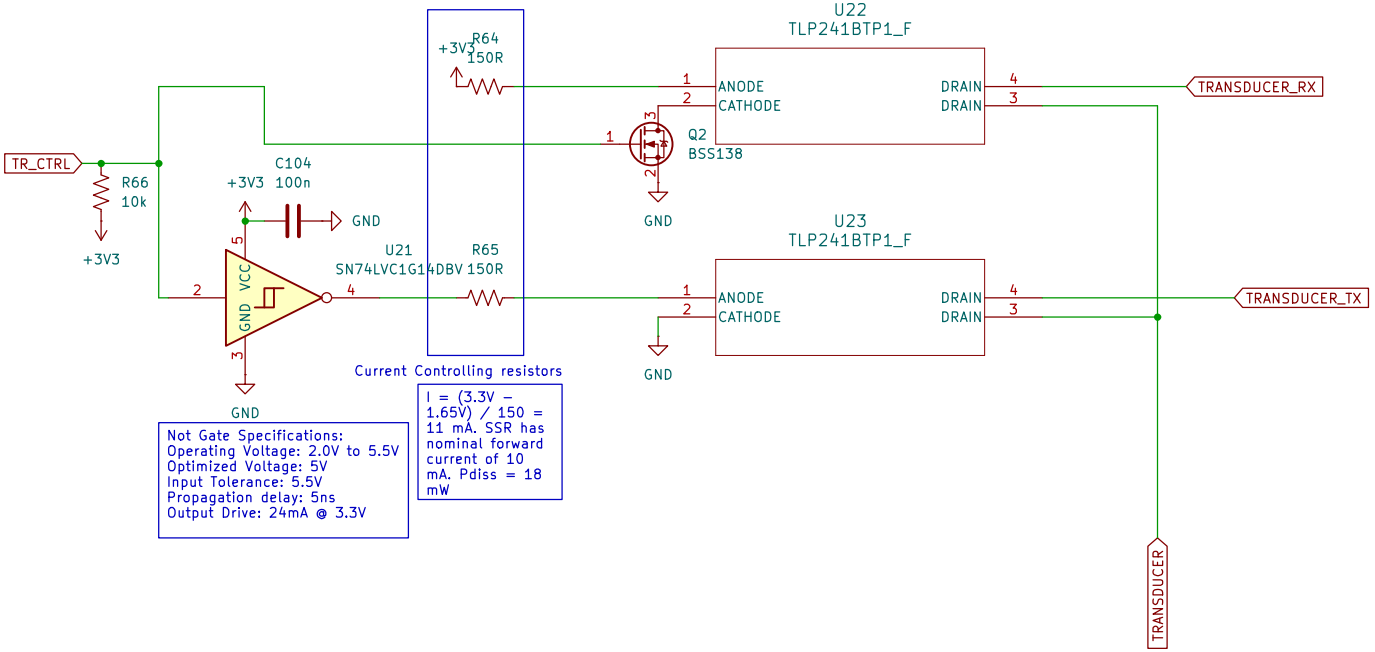


Notes:
- −Overall Low Circuit Noise
- −Some non−linearities
- −Potential Harmonic Distortion if freq too high
- −SNR ratio of ~84dB
- −Noise Voltage of ~0.3uV
- −RIAA curve within 0.1dB

2−stage pre−amplifier was chosen as single stage solutions with sufficient GBW and a sufficiently low input voltage offset were too expensive and a 2−stage amplifier allows for easier control of the gain through the feedback resistors in the second stage

Total Gain = 70dB

PDF for calculations:
https://www.ti.com/lit/an/snoa586d/snoa586d.pdf



Relay Control Voltage: 5V

LED Maximum Ratings:
Input Forward Current: 30mA
Input Reverse Voltage: 6V
Input Power Dissipation: 50mW
Junction temperature: 125C max

Detector Maximum Ratings:
OFF-state output terminal voltage: 100V
ON-State Current: 2A max
Output Power dissipation: 550mW
Junction temperature: 125C max

Common Maximum Rating:
Storage Temp: -55C to 125C
Operating Temp: -40C to 110C
Lead Soldering Temp: 260C
Isolation Voltage: 5000 Vrms

Recommended Operating Cond:
Supply Voltage: 80V max
Input Forward Current: 5ma to 25mA
ON-state current: 2A
Operating Temp: -20C to 85C

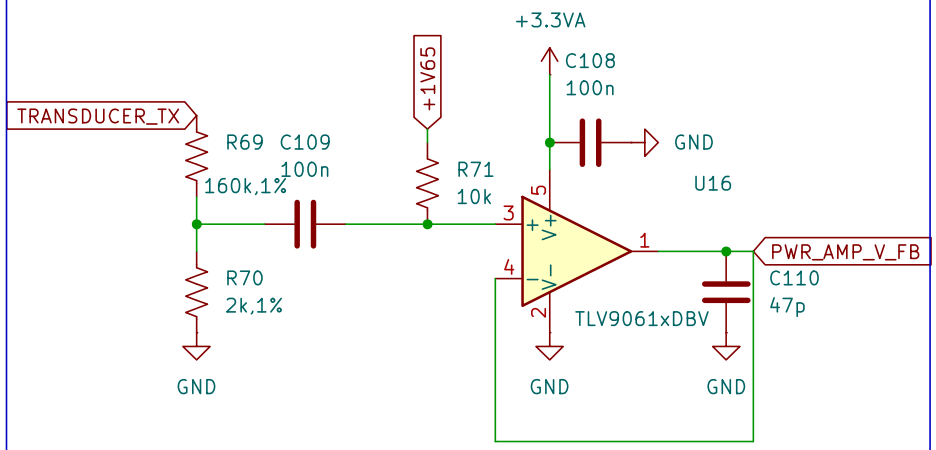
LED characteristics:
Input Forward Voltage: 80V
Input Reverse Current: 5mA to 25mA
Input Capacitance: 50pF

Detector:
OFF-State Current: 0.01uA (1uA max)
Output Capacitance: 300pF

Switching Characteristics:
Turn-ON time: 0.8ms (3ms max)
Turn-OFF time: 0.2ms (0.5ms max)

Using Relay control, we can activate one of the SSRs and make the circuit switch between the transmission and the receiver digitally
Since t_on ~= ~3*t_off across a range of drive currents, there is no need to add additional delay as long as there is not significant capacitance on the transducer

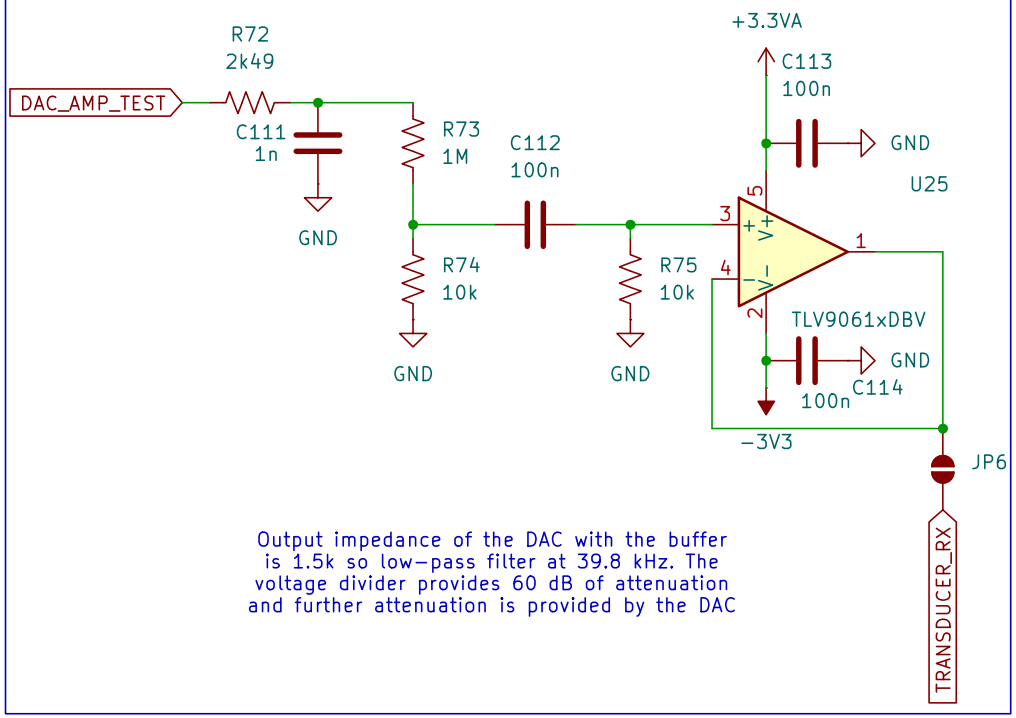
Output voltage feedback network



Feedback network from the transmission since the voltage can exceed the maximum rating of the SSR (100V) if not controlled properly. There is also a TVS diode with a breakdown voltage of 86.7V. This network ensures the TVS is not constantly working during transmission. Voltage divider set to a ratio of 81 to read +/− 80V on microcontroller 3.3V ADC

Feedback network for the pre−amplifier to determine if the gain is working properly

Sets the DC offset to 0V to be more realistic



Output impedance of the DAC with the buffer is 1.5k so low−pass filter at 39.8 kHz. The voltage divider provides 60 dB of attenuation and further attenuation is provided by the DAC