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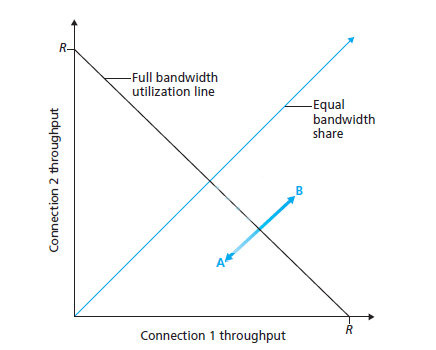
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CS 118

Dis 1A

Homework 5

41. If both the increase and decrease were linear, then the resulting algorithm would not converge to an equal share algorithm. Instead, if connect 1 and 2 have the same linear decrease, then their throughput would just go back and forth between points A and B.



If the linear decrease of connections 1 and 2 is not equal, then the bandwidth utilization will shift towards the one with less loss.

45. a. L = , 1 packet lost from W/(2 \* RTT) to W/RTT so packets lost = 1

Packets sent =

L =

b. L becomes when W is a large number. The average throughput is stated to be so we solve for W which is . This gives

1. a. Datagram architecture would be better as the effects of a failed router can be kept to a small area around that router. Also, there would not be any need for signaling between routers to avoid the failed router as the routers can just update their tables.

b. VC would be better as it can keep states. Using this, the routers can know how much traffic is passing from every active session.

c. VC would be preferred as the circuits will be constant while the datagram architecture requires constant transmitting of headers.

|  |  |
| --- | --- |
| Dest Addr | Outgoing Link |
| H3 | 3 |

4. a.

b. Not possible, we can’t have one dest addr with two outgoing links since this is using datagram architecture

|  |  |  |  |
| --- | --- | --- | --- |
| Incoming Inter | Incoming VC # | Outgoing Inter | Outgoing VC# |
| 1 | 20 | 3 | 40 |
| 2 | 30 | 4 | 50 |

c.

d.

B:

|  |  |  |  |
| --- | --- | --- | --- |
| Incoming Inter | Incoming VC # | Outgoing Inter | Outgoing VC# |
| 1 | 40 | 2 | 60 |

C:

|  |  |  |  |
| --- | --- | --- | --- |
| Incoming Inter | Incoming VC # | Outgoing Inter | Outgoing VC# |
| 1 | 50 | 2 | 70 |

D:

|  |  |  |  |
| --- | --- | --- | --- |
| Incoming Inter | Incoming VC # | Outgoing Inter | Outgoing VC# |
| 1 | 60 | 3 | 80 |
| 2 | 70 | 3 | 90 |

7. a. No, only one packet can go through at a time for a shared bus

b. Maybe, if both have the same destination then it is not possible; but if both have different destinations, it is possible.

c. No, output port can only send one packet at a time so it is impossible for them to be both sent out at the same time

6. It takes 750ms for the sender to receive the ack for the segment with sequence number 12.