Rare Event Diagnosis by Iterative Failure Region Locating and Elite Learning Sample Selection

Hosoon Shin*, Sheldon X.-D. Tan* ,Guoyong Shi† and Esteban Tlelo-Cuautle‡,
*Department of Electrical and Computer Engineering, University of California, Riverside, CA 92521
†School of Microelectronics, Shanghai Jiao Tong University, Shanghai, 200240, China
†Institute National Astrophysics, Optical and Electrics (INAOE), Puebla, Mexico

Abstract—Accurately estimating the failure region of rare events for nanoscale analog circuit blocks under process variations is a challenging task. In this paper, we propose a new statistical rare event analysis method. The new method is based on the iterative failure region locating scheme to reduce the sample counts while still maintains estimation accuracy. We derive the complete formulation for failure probability calculation in each iterative step. In addition, the new approach applies an elite learning sampling scheme, which considers both effectiveness of samples and well-coverage for process parameter search space, to further reduce number of samples after the gradual failure region locating at each iteration. As a result, the sample counts for simulation can be significantly reduced while sufficient representative samples are still kept for accurate failure probability analysis. Experiments were performed on the rise and fall time balancing failure analysis with Vth-NMOS, Vth-PMOS process parameters and the 4-gates logic circuit with 48 process parameters. The proposed method can deliver 228x faster than the conventional MC method with only 0.02-0.2% estimation errors. Furthermore, the new method estimates 20x more accurately with only 1.2x additional simulation costs than a recently published approach.

I. Introduction

With aggressive technology scaling, the performance uncertainties due to process variation have become a major concern for today's integrated circuits (ICs) [1]. Many IC components such as SRAM bit-cells need to be extremely robust as they need to be duplicated in millions [2]. Failure probability analysis of such robust modules requires statistical rate event analysis or high-sigma analysis, which posts challenges to the traditional Monte Carlo (MC) based statistical analysis [3] as it may require million or hundreds of millions of simulations.

To mitigate this problem, a large body of statistical algorithms have been developed in the literature [3]–[10]. The first avenue for improving MC is importance sampling (IS). [10] applied the mixture IS to predict failure region. For more dense samples in rare event failure region, the bounded condition for importance sampling is proposed to generate new distribution for failure region [5]. This approach shifts mean value of the initial distribution and re-calculate the standard deviation. However, IS can only estimate single performance metric. To estimate more metrics, multiple important sample runs are required for each metric. Moreover, it cannot rebuild a failure region distribution correctly with high-dimensional statistical parameters.

Another effective method is so-called "blockade method" [3]. The method first builds "classifier" from some samples. The classifier decides likely-to-fail samples before running the real circuit simulation. However, linearly shifted samples cannot describe well in case of the discontinuous and nonlinear failure regions. This method has been further

improved for heavy-tailed region in performance metric distribution using iterative estimation method [4]. This approach, which called the recursive statistical blockade (RSB), repeatedly forms the classifier and simulates samples in extremely rare event regions close to 5 or 6 sigma region. The main advantage of this method is that it can improve the accuracy of the classifier iteratively by increasing the number of samples in the rare failure region of interests. However, this approach used linear support vector machine (LSVM) as the classifier so it can lead to large errors to determine pass or fail samples in the nonlinear result space. Furthermore, the simulation cost from added samples from iterative process can be significant. Recently Wu et al. [6] applied nonlinear SVM classifier to model nonlinear circuit behavior and multiple disjoint failure regions. Parameter pruning based on initial samples simulation was also applied for reducing the dimension of parameters so samples can only focus on sensitive parameters. However, this approach cannot investigate further failure region without massive additional simulation costs. Furthermore, the pruned parameters acquired by the initial samples can be wrong as they may be the real sensitivities of parameters in updated failure region.

In this paper, we propose a new statistical rare event analysis method. The new method is based on the iterative failure region locating scheme, which is similar to the recursive statistical blockade method, to reduce the sample counts while still maintains estimation accuracy. We derive the precise mathematical formula to calculate the failure probabilities of updated region in the iterative process. This formulation allow iterative or recursive updating of the probabilities of targeted failure regions. Second, the new approach applies an elite sampling scheme, which considers both effectiveness of samples and well-coverage for process parameter search space, to further reduce the number of sample after the gradual failure region locating at each iteration. Experimental result on the critical delay of 4-gates logic circuit with 48 dimensional process parameters, show that the proposed method can deliver 228x faster than the conventional MC method. Furthermore, the new method estimates 10x more accurately with only 1.2x additional simulation costs than the recently published approach [6].

The rest of this paper is organized as follows. Section 2 discusses essential background for sample-based failure analysis and revisits some major techniques for improving MC performance. In Section 3, we explain the proposed algorithm with an overall flow and detailed description of the elite sampling and mathematical formulation for iteratively relocated failure region. Section 4 shows the experimental result for verifying the accuracy and efficiency of the proposed method. Section 5 provides conclusions of this paper.

II. BACKGROUND

A. Importance sampling

In sample-based statistical analysis, importance sampling (IS) is a general technique to estimate properties of rare event region using the samples generated from the initial distribution. Fig.1 shows the generated distribution $g(x)$ by IS with two parameters. As we can see in the figure, the property of the failure region can be captured as more samples are obtained in the failure region. Therefore, the proper sampling scheme is needed to build the right distribution representing the rare event region. One of IS-based approaches is focusing on quasi-random sampling to explore the parameters space more uniformly. The samples can be selected by the initial MC sampling, so that more regular space filling makes the initial samples to cover large variety combinations of parameters [11]. Another well-known approach is the mean shifting and variance reconstructing, which the initial distribution is centered around the failure region [9], [10]. However, all these approaches assume a linear relation between the reconstructed and the initial distributions, so the generated samples cannot reflect the nonlinear rare event region correctly.

B. Classification

The classification is a step that the samples can be classified into likely-to-fail samples for circuit simulation. Building a classifier needs a training step with initial samples to render real shapes of the failure region. The classifier can shrink the number of samples, thus the simulation cost is reduced. However, it is not capable of fully replacing the simulator due to its accuracy. So, a marginal filtering approach is used to improve the accuracy of classification [3]–[6]. This method uses relaxed threshold bounds instead of a real failure criterion to capture more samples to minimize classification error. Meanwhile, it is not sufficient to use a simple and linear classifier due to the nonlinearity of the failure region [3]–[5]. So, Gaussian radial basis function kernel (GRBF) and neural networks methods are available for nonlinear classifiers [6], [12]. Fig. 2 shows the accuracy of classification in a 2-dimensional search space example. Even the solution space is separated with non linear relation, GRBF can recognize patterns properly while the LSVM draws a wrong boundary between two categories.

C. Failure probability calculation

The failure samples should be fitted to a particular distribution form in order to calculate the probability of the failure region in the distribution of circuit performance metric. Suppose that the probability density function (PDF) of the metric can be fitted to Gaussian distribution. If there are some threshold value x_t which separates a tail from the body of
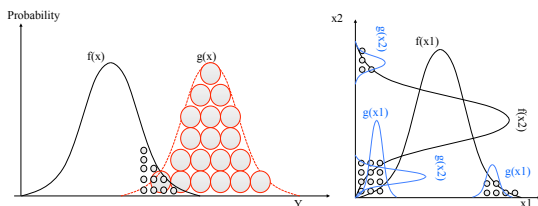

Fig. 1. Generated PDF by importance sampling in 2-D random variables
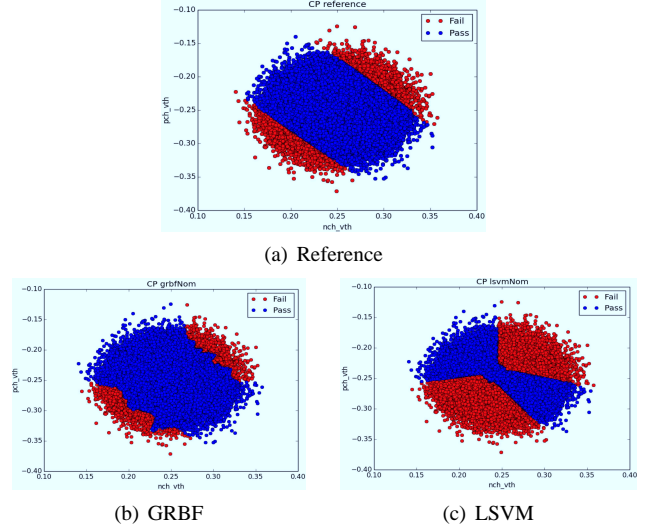

(a) Reference

(b) GRBF

(c) LSVM

Fig. 2. The classification accuracy of two different methods

the PDF function, the conditional cumulative density function (CDF) of the tail can be written as follows:

$$F_t(x) = P(X > x \mid X > x_t) = \frac{F(x) - F(x_t)}{1 - F(x_t)} \quad (1)$$

where $F_t(x)$ means the failure probability decided by x. Once we have a suitable fitting model for the CDF of the failure region with a failure criterion x_c, the failure probability of given value can be calculated as:

$$P(x > x_c) = [1 - F(x_t)][1 - F_t(x_c)] \quad (2)$$

According to the extreme value theory, the generalized Pareto distribution (GPD) is the most accurate model with particular failure threshold [13]. Therefore, the CDF of the failure region is written as follows.

$$
\begin{aligned}
F_t(x) &= G_{(\xi,\mu,\sigma)}(x) \\
&= \begin{cases} 1 - \left(1 + \dfrac{\xi(x - \mu)}{\sigma}\right)^{-1/\xi} & \text{for } \xi \neq 0 \\ 1 - e^{\frac{-(x-\mu)}{\sigma}} & \text{for } \xi = 0 \end{cases}
\end{aligned} \quad (3)
$$

The CDF with the threshold x_c can be obtained by initial samples simulation to capture the circuit behavior. Consequently, the failure probability can be computed as follows.

$$P(x > x_c) = [1 - P(X \leq x_t)][1 - G_{(\xi,\mu,\sigma)}(x_c)] \quad (4)$$

To approximate parameters for the GPD fitting, we use maximum likelihood estimation [14].

III. NEW STATISTICAL FAILURE RARE EVENT ANALYSIS METHOD

In this section, we present the proposed method, which is called, "SmartERA" (Smart Extremely Rare event Analysis). SmartERA performs accurate failure region analysis and failure probability calculation using iterative region locating and elite sample selection schemes. The overall flow of the proposed method is illustrated in Fig. 3. First of all, initial MC sampling is performed for simulation using SPICE. The result of the initial simulation is used for capturing overall circuit performance metrics. With this result, the first relaxed bound on the threshold t_1 can be obtained with a given percentile bound p. The initial classifier C_1 is then built by training with initial simulation results. A GRBF nonlinear
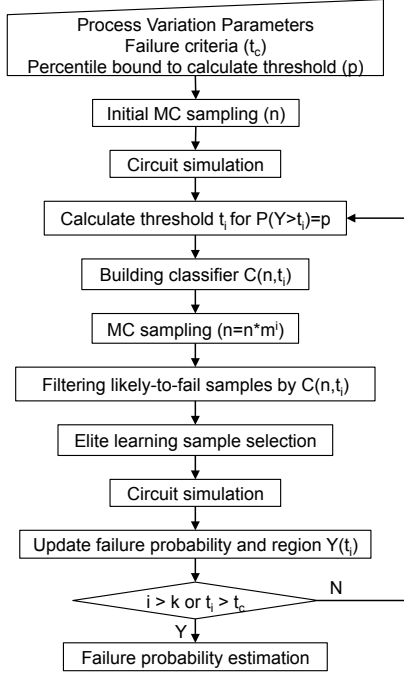
Fig. 3. Proposed iterative statistical failure region analysis flow

classifier is used to recognize nonlinear and disjointed failure regions. After building classifier, the algorithm generates m^i MC samples and C_1 filters out these samples to likely-to-fail samples based on t_1. Next, the elite sample selection method is employed to further reduce the number of samples for actual simulation. Using this simulation result, a failure probability and region Y_i are updated by GPD fitting. Our method calculates the probability of updated region using proposed mathematical model. Our algorithm repeats all the mentioned steps again based on newly updated failure region Y_i and threshold bound t_i. The algorithm finishes when either the threshold bound meets the given failure criterion t_c or the number of iterations exceeds the maximum number of iterations allowed k. The rest of this section explains the two major contributions of the proposed method: (1) Iterative computing of failure probability; (2) Elite learning sample selection.

A. Iterative computing of failure probability

It is typically difficult task to choose right threshold bound in the failure analysis for an extreme rare event region. For instance, the failure region is decided by the failure criterion t_c and the probability of this region is around 99.9999%. Suppose that we use single threshold method, then we can choose a very loose threshold t as $P(Y > t)$ around 99% to safely cover whole failure region even though the threshold can be quite far away t_c. Moreover, the number of MC samples for filtering will be determined at once. If the number of MC samples is relatively enormous, a classifier will select too many likely-to-fail samples, which will significantly increases simulation cost. Meanwhile, if the selected likely-to-fail samples is so small, this will cause the inaccurate analysis of the failure region and thus the failure probability.

To mitigate this problem, our method applied gradually locating of the failure region in an iterative way based on

RSB method. Unlike the single threshold method that calculates a failure probability at once, our approach updates a failure region $Y_1(> 99\%)$ and the probability by GPD fitting after the first iteration. With this updated failure region, the threshold bound is re-computed for a newly updated region $Y_2(> 99.99\%)$. The GRBF classifier is trained by failure samples in the first iteration so that it can capture likely-to-fail samples more precisely in the updated failure region. In the second iteration, the number of MC samples increases from $10n$ to $10^2 n$ as the increasing ratio is 10, so more MC samples will lead to capture more samples in the failure region. Consequently, the updated classifier based on relocated threshold bound allows more samples only placed on the interesting failure region.

As the algorithm iterates, a failure region is scoped continuously close to the given failure criterion t_c based on the re-computed t_i and likely-to-fail samples are converged on the updated failure region. Therefore, the proposed method achieves accurate failure analysis than a single threshold method with relatively less additional simulation cost. Fig.4 shows an iterative locating procedure for finding the failure region.

To deal with the proposed iterative method, the probability for updated failure region should be repeatedly calculated. As discussed in Section 2, the CDF with given a threshold t and a failure criterion t_c can be calculated as

$$P_{IS}(Y \geq t_c) = P_{MC}(Y \geq t) \cdot P(Y \geq t_c | Y \geq t)$$
$$P(Y \geq t_c | t \geq t) = \frac{P(Y \geq t_c, Y \geq t)}{P(Y \geq t)} \quad (5)$$

The conditional probability part in (5) can be estimated by GPD fitting using simulated failure samples. Therefore, (5) can be rewritten as

$$P_{IS}(Y > t_c) = P_{MC}(Y \geq t) \cdot P_{MIS}(Y \geq t_c | Y \geq t) \quad (6)$$

where P_{MIS} represents the conditional probability in updated distribution by GPD fitting. If the proposed method iterates twice with t_1 and t_2 as threshold bounds, the second failure probability can be calculated based on the first failure region. So, the failure probability in each step can be calculated as

$$P_{IS}(Y \geq t_c) = P_{IS(2)}(Y \geq t_c)$$
$$P_{IS(1)}(Y \geq t_2) = P_{MC}(Y \geq t_1)$$
$$\cdot P_{MIS(1)}(Y \geq t_2 | Y \geq t_1)$$
$$P_{IS(2)}(Y \geq t_c) = P_{MC}(Y \geq t_1) \cdot P_{MIS(1)}(Y \geq t_2) \quad (7)$$
$$\cdot P_{MIS(2)}(Y \geq t_c | Y \geq t_2)$$
$$P_{MIS(i)}(Y \geq t_c | Y \geq t_i) = \frac{P_{MIS(i)}(Y \geq t_c)}{P_{MIS(i)}(Y \geq t_i)}$$

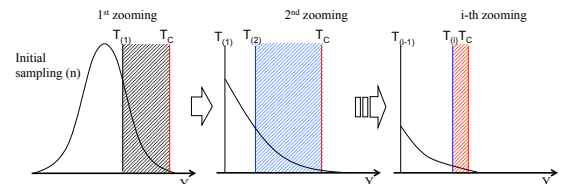Without the loss of generality, we can formulate the iterative

Fig. 4. Iterative locating of failure region by changing thresholds

failure probability calculation as follows.

$$P_{IS(i)}(Y \geq t_c)$$
$$= \begin{cases} P_{MC}(Y \geq t_i) \cdot P_{MIS(i)}(Y \geq t_c | Y \geq t_i) & \text{for } i = 1 \\ P_{MC}(Y \geq t_i) \cdot \prod_{i=1}^{k-1}(P_{MIS(i)}(Y \geq t_{i+1})) \\ \quad \cdot P_{MIS(k)}(Y \geq t_c | Y \geq t_k) & \text{for } i > 1 \end{cases} \tag{8}$$

where k is the number of iterations. Finally, the failure probability can be obtained by combining all calculated probabilities in each iteration.

B. Elite learning sample selection

The simulation cost is a major bottleneck in the failure analysis of the circuit. Furthermore, the proposed iterative failure region location method can lead to more samples in each iterations. To mitigate this problem, we propose an elite sampling scheme, which significantly reduce the number of samples required.

Two factors can be considered for the sample selection process. The effectiveness of the sample group is the first factor. Each sample is composed with a diverse combination of high-dimensional parameters as there are the huge number of parameters in the statistical circuit failure analysis. Each parameter has a different impact on simulation results. Therefore, each sensitivity of parameter should be considered for the sample selection. The proposed selection method calculates the correlation coefficient between parameters and simulation results for the sensitivity analysis. Suppose that $\mathbf{x}$ is a process parameter vectors with m dimension, y is the simulation result, and n is the number of samples. The correlation coefficient can be calculated as

$$x_n \in R^m, y_n \in R$$
$$\rho_{x_n, y_n} = corr(x_n, y_n) = \frac{cov(x_n, y_n)}{\sigma_{x_n} \sigma_{y_n}} \tag{9}$$
$$\rho_{x_n, y_n} \in R^m$$

The second factor is the search space coverage by selected samples. The diversity of samples can be calculated by Euclidean distance with a reference sample, which is the median of the simulation result. The samples around the median should be chosen because the median is located on the highest probability region in the distribution of simulation results. Simultaneously, the samples found in the boundary region of the search space should be selected because these samples represent the combinations of maximum and minimum parameters. These combinations can construct the right or left tail failure region from the resulting distribution. The proposed sampling method calculates two distance factors to cover both central and boundary regions of the search space as follows:

$$\tilde{y} = median(y_n)$$
$$x_{ref} = x : \tilde{y} = f(x), x \in R^m$$
$$D_{central}(x) = \frac{1}{\left| \frac{x - x_{ref}}{max(x_n) - min(x_n)} \right|} \in R^m \tag{10}$$
$$D_{boundary}(x) = \left| \frac{x - x_{ref}}{max(x_n) - min(x_n)} \right| \in R^m$$

We calculate the weight of each sample to consider both the effectiveness and the coverage by multiplying the correlation coefficient to distance factors of each sample as

$$W_{central}(x) = \rho_{x_n, y_n}^T \cdot D_{central}(x)$$
$$W_{boundary}(x) = \rho_{x_n, y_n}^T \cdot D_{boundary}(x) \tag{11}$$

The final set of sample selection can be obtained as

$$E(n, r) = S(\frac{nr}{2}, W_{central}(x_n)) \cup S(\frac{nr}{2}, W_{boundary}(x_n)) \tag{12}$$

where $S(n, W(x_n))$ is the set of n samples x_n sorted by $W(x_n)$ and r is the selection ratio, which determines the number of selected samples.

IV. EXPERIMENTAL RESULTS

The proposed method has been tested on the failure analysis of two test cases : the rise and fall time balancing of the CMOS inverter and the critical path delay of the 4-gates logic circuit. All of the test circuits were designed with the BSIM4 transistor model and simulated by NGSPICE [15]. Table. I presents the list of process parameters of MOSFET used for test circuits. The proposed methods (SmartERA : without sample selection, SmartERA2: with sample selection) were implemented in Python. We performed the three different methods (MC, REscope [6], SmartERA, SmartERA2) to compare their accuracy and performance.

TABLE I
PROCESS PARAMETERS OF MOSFET

Variable name	Std(σ/μ)	Unit
Flat-band voltage(V_{fb})	0.1	V
Gate oxide thickness(t_{ox})	0.05	m
Mobility (μ_0)	0.1	m^2/Vs
Doping concentration at depletion N_{dep})	0.1	cm^{-3}
Channel-length offset (ΔL)	0.05	m
Channel-width offset (ΔQ)	0.05	m
Source/drain sheet resistance(R_{sh})	0.1	Ohm/mm^2
Source-gate overlap unit capacitance(C_{gso})	0.1	F/m
Drain-gate overlap unit capacitance(C_{gdo})	0.1	F/m

A. The rise and fall time balancing of the CMOS inverter

The rising and falling delays of the well-designed CMOS inverter are nearly equal (e.g. VDD=1.8V, then the ideal crossing point is 0.9V). The threshold voltages (V_{th}) of NMOS and PMOS are considered as the process parameters to demonstrate the accuracy of the GRBF method and the performance of the elite sample selection. The MC run with one million samples is performed to generate the reference data. For the building classifier, 1,000 random samples are used for the initial training and 100,000 samples are used for the classification test. Fig. 5 shows the case that the number of selected samples is 1/5. The V_{th} of NMOS is more dominant than PMOS to balance rising and falling delays in the inverter as the NMOS current discharging rate is higher than PMOS. As a result, The elite sample selection is strongly impacted by V_{th} of NMOS than PMOS depend on the sensitivity analysis of process parameters. Moreover, the samples can be evenly found in the both central and boundary regions of the search space of V_{th} of NMOS.
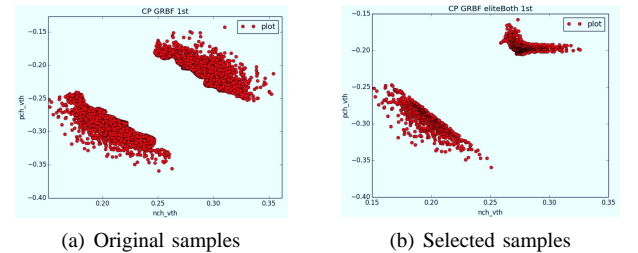

(a) Original samples   (b) Selected samples

Fig. 5. Sample selection result of likely-to-fail samples
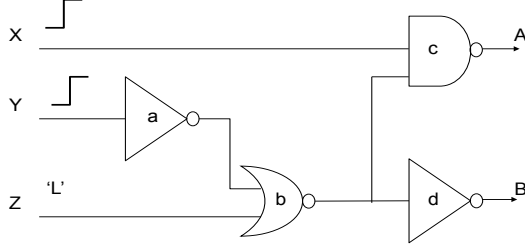
Fig. 6. The schematic of 4-gates logic circuit

	Failure region	Prob. est.(%)	# Sim. runs	Speed -up(x)	Error (%)
Monte Carlo	$P(Y < t_c)$ =0.95	9.500E+01	600K	-	-
REscope		9.465E+01	4531	132.4	0.3649
SmartERA2		9.482E+01	2632	228.0	0.1846
Monte Carlo	$P(Y < t_c)$ =0.999875	9.999E-01	600K	-	-
REscope		9.994E+01	4531	132.4	0.0475
SmartERA2		9.997E+01	2632	228.0	0.0205
SmartERA(2nd)		9.999E+01	12369	48.5	0.0024
SmartERA2(2nd)		9.998E+01	5620	106.8	0.0025

B. The critical path delay of the simple circuit

The test logic circuit consists of four gates (2 INVs, 1 NOR, and 1 NAND) as shown in Fig 6 [16]. The critical path delay in the circuit is $max(fall\_A, fall\_B)$ (X,Y is rising and Z is 0). Two critical paths can be found, and the total number of process parameter is 48. The failure criterion is $P(Y < t_c)$=0.999875, thus, the failure region is located under the 4-sigma range in the distribution of the critical path delay. Two iteration threshold bounds are $P(Y < t_1)$=0.93 and $P(Y < t_2)$=0.9951, respectively. As we can see that from Table. II, SmartERA2 can estimate the failure probability in 228x faster than the traditional MC method with 0.02-0.2% errors. Also, SmartERA2 is about 20x more accurate only with 1.2x additional simulation cost than REscope in the estimation of the failure region under 4-sigma range. The CDF of the failure region is more correlated to the reference than REscope as shown in Fig. 7.

V. CONCLUSION

This paper presented a novel statistical analysis for rare failure events. The proposed method is based on recursive statistical blockade scheme to reduce the number of samples while still maintain sufficient estimation accuracy. We show how the failure probabilities are calculated at each iterative step. In addition, the new approach applies the elite sampling scheme, which considers both effectiveness of samples and well-coverage for process parameter search space, to further reduce number of samples. Experimental results showed that the proposed method can deliver 228x faster than the Monte Carlo approach with only 0.02-0.2% errors in the estimation of the failure region. Furthermore, the new method evaluates the probability of the failure region 20x more accurately with only 1.2x additional simulation costs than the recently published approach.

Fig. 7. The failure distribution $P(Y < t_c)$=0.999875 of the critical path delay of the simple circuit

REFERENCES

[1] B. Calhoun, Y. Cao, X. Li, K. Mai, L. Pileggi, R. Rutenbar, and K. L. Shepard, "Digital circuit design challenges and opportunities in the era of nanoscale cmos," *Proceedings of the IEEE*, vol. 96, pp. 343–365, Feb 2008.

[2] H. Masuda, S. Ohkawa, A. Kurokawa, and M. Aoki, "Challenge: variability characterization and modeling for 65- to 90-nm processes," in *Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005*, pp. 593–599, Sept 2005.

[3] A. Singhee and R. Rutenbar, "Statistical blockade: Very fast statistical simulation and modeling of rare circuit events and its application to memory design," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 28, pp. 1176–1189, Aug 2009.

[4] A. Singhee, J. Wang, B. Calhoun, and R. Rutenbar, "Recursive statistical blockade: An enhanced technique for rare event simulation with application to sram circuit design," in *VLSI Design, 2008. VLSID 2008. 21st International Conference on*, pp. 131–136, Jan 2008.

[5] W. Wu, F. Gong, G. Chen, and L. He, "A fast and provably bounded failure analysis of memory circuits in high dimensions," in *Design Automation Conference (ASP-DAC), 2014 19th Asia and South Pacific*, pp. 424–429, Jan 2014.

[6] W. Wu, W. Xu, R. Krishnan, Y.-L. Chen, and L. He, "Rescope: High-dimensional statistical circuit simulation towards full failure region coverage," in *Design Automation Conference (DAC), 2014 51st ACM/EDAC/IEEE*, pp. 1–6, June 2014.

[7] S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Statistical design and optimization of sram cell for yield enhancement," in *Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Conference on*, pp. 10–13, Nov 2004.

[8] K. Agarwal and S. Nassif, "Statistical analysis of sram cell stability," in *Design Automation Conference, 2006 43rd ACM/IEEE*, pp. 57–62, 2006.

[9] M. Qazi, M. Tikekar, L. Dolecek, D. Shah, and A. Chandrakasan, "Loop flattening & spherical sampling: Highly efficient model reduction techniques for sram yield analysis," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2010*, pp. 801–806, March 2010.

[10] S. N. R. Kanj, R. Joshi, "Mixture important sampling and its application to the analysis of sram designs in the presence of rare failure events," in *Proc. IEEE/ACM Design Automation Conference (DAC)*, pp. 69–72, 2006.

[11] D.Montgomery, *Design and Analysis of Experiments*. Wiley, 2013.

[12] T.Hastie, *The Elements of Statistical Learning: Data Mining, Inference, and Prediction*. Springer, 2009.

[13] J. J.R.Hosking, "Parameter and quantile estimation for the generalized pareto distribution," *Technometrics*, vol. 29, no. 3, pp. 339–349, 1987.

[14] J.R.Hosking, "Algorithm as 215: Maximum-likelihood estimation of the parameters of the generalized extreme-value distribution," *Journal of the Royal Statistical Society. Series C (Applied Statistics)*, vol. 34, no. 3, pp. 301–310, 1985.

[15] P. Nenzi and V. Holger, "Ngspice users manual," *Version 25plus*, 2010.

[16] J. Kim, K. Jones, and M. Horowitz, "Fast, non-monte-carlo estimation of transient performance variation due to device mismatch," in *Design Automation Conference, 2007. DAC '07. 44th ACM/IEEE*, pp. 440–443, June 2007.