AMBA AXI 3 Protocol Overview:

FROM SPECIFICATION:

The AMBA AXI protocol is targeted at high-performance, high-frequency system designs and includes a number of features that make it suitable for a high-speed submicron interconnect.

The AXI protocol is burst-based. Every transaction has address and control information on the address channel that describes the nature of the data to be transferred. The data is transferred between master and slave using a write data channel to the slave or a read data channel to the master. In write transactions, in which all the data flows from the master to the slave, the AXI protocol has an additional write response channel to allow the slave to signal to the master the completion of the write transaction.

The AXI protocol enables:

- address information to be issued ahead of the actual data transfer
- support for multiple outstanding transactions
- support for out-of-order completion of transactions.

FOR OUR PROJECT:

Basic transactions:

1. Read burst:
    a. Command Signals
        i. Master:
            1. ARID: Read address ID. This signal is the identification tag for the read address group of signals
            2. ARADDR: Read Address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
            3. ARLEN: Burst length. The burst length gives the exact number of transfers in a burst.
            4. ARSIZE: Burst size. This signal indicates the size of each transfer in the burst.
            5. ARBURST: The burst type, coupled with the size information details how the address for each transfer within the burst is calculated.
            6. ARVALID: Read address valid. This signal when high indicates that the read address and control information is valid and will remain stable until the address acknowledge signal ARRREADY is high.
            7. RREADY: Read ready. This signal indicates that the master can accept the read data and response information.
        ii. Slave:
            1. ARRREADY: Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
            2. RID: Read ID tag. This signal is the ID tag of the read data group of signals. The RID value is generated by the slave and must match the ARID value of the read transaction to which it is responding.

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3. RLAST: Read last. This signal indicates the last transfer in a read burst.
4. RVALID: Read valid. This signal indicates that the required read data is available and the read transfer can complete.

b. Key points to check
   i. Handshaking Protocol: Source generates the valid signal to indicate when the data or control information is available. Destination generates the ready signal to indicate that it accepts the data or control information. Transfer occurs when both signals are high on positive edge of clock. No requirement that one particular signal goes high before the other.
   ii. Burst length: Determine if an operation in the queue receives the correct number of bursts, in addition to the final transfer including the rlast signal.
   iii. Overlapping reads enabled: Need to be able to drive a read immediately after the previous read is
   iv. Out of order transactions enabled: The master needs to be able to accept data from the slave out of order.

2. Write burst:
   a. Command Signals
      i. Master:
         1. AWID:Write address ID. This signal is the identification tag for the write address group of signals.
         2. AWADDR:Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
         3. AWLEN:Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
         4. AWSIZE:Burst size. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
         5. AWBURST:Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated.
         6. AWVALID:Write address valid. This signal indicates that valid write address and control information are available.
         7. WID: Write ID tag. This signal is the ID tag of the write data transfer. The WID value must match the AWID value of the write transaction.
         8. WLAST:Write last. This signal indicates the last transfer in a write burst.
         9. WVALID:Write valid. This signal indicates that valid write data and strobes are available:
         10. BREADY:Response ready. This signal indicates that the master can accept the response information.
      ii. Slave:
         1. AWREADY: Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals:
         2. WREADY: Write ready. This signal indicates that the slave can accept the write data:
         3. BID: Response ID. The identification tag of the write response. The BID value must match the AWID value of the write transaction to which the slave is responding.

4. BVALID: Write response valid. This signal indicates that a valid write response is available.

b. Key points to check
   i. Handshaking protocol: Source generates the valid signal to indicate when the data or control information is available. Destination generates the ready signal to indicate that it accepts the data or control information. Transfer occurs when both signals are high on positive edge of clock. No requirement that one particular signal goes high before the other.
   ii. Burst length: The Master needs drive the correct number of bursts to the slave
   iii. Out of order transactions enabled: The master needs to be able to accept write responses from slave out of order.