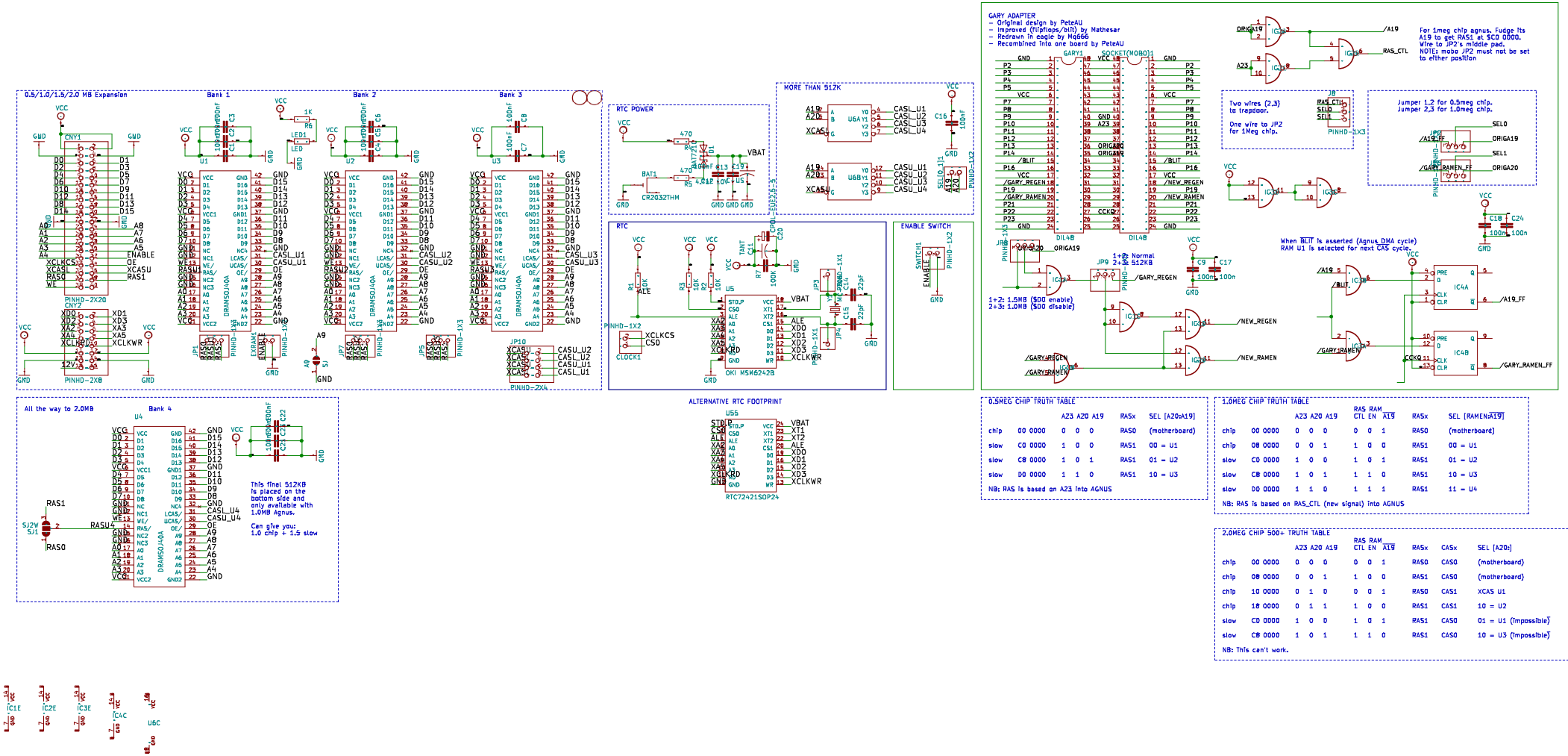

0.5MEG CHIP TRUTH TABLE

		A23	A20	A19	RASx	SEL [A20:A19]
chip	00 0000	0	0	0	RAS0	(motherboard)
slow	C0 0000	1	0	0	RAS1	00 = U1
slow	C8 0000	1	0	1	RAS1	01 = U2
slow	D0 0000	1	1	0	RAS1	10 = U3

NB: RAS is based on A23 into AGNUS

1.0MEG CHIP TRUTH TABLE

		A23	A20	A19	RAS RAM CTL	EN	A19	RASx	SEL [RAMEN:A19]
chip	00 0000	0	0	0	0	0	1	RAS0	(motherboard)
chip	08 0000	0	0	1	1	0	0	RAS1	00 = U1
slow	C0 0000	1	0	0	1	0	1	RAS1	01 = U2
slow	C8 0000	1	0	1	1	1	0	RAS1	10 = U3
slow	D0 0000	1	1	0	1	1	1	RAS1	11 = U4

NB: RAS is based on RAS_CTL (new signal) into AGNUS

2.0MEG CHIP 500+ TRUTH TABLE

		A23	A20	A19	RAS RAM CTL	EN	A19	RASx	CASx	SEL [A20:]
chip	00 0000	0	0	0	0	0	1	RAS0	CAS0	(motherboard)
chip	08 0000	0	0	1	1	0	0	RAS1	CAS0	(motherboard)
chip	10 0000	0	1	0	0	0	1	RAS0	CAS1	XCAS U1
chip	18 0000	0	1	1	1	0	0	RAS1	CAS1	10 = U2
slow	C0 0000	1	0	0	1	0	1	RAS1	CAS0	01 = U1 (impossible)
slow	C8 0000	1	0	1	1	1	0	RAS1	CAS0	10 = U3 (impossible)

NB: This can't work.