EECS 142

Integrated Circuits for Communication
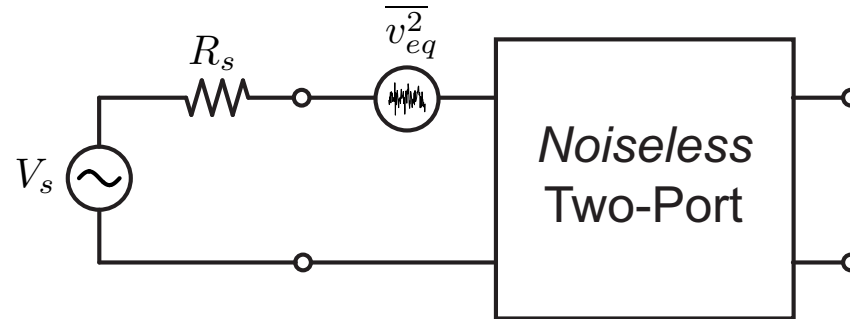
Lecture 13: Amplifier Noise Calculations

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Recap from Last Lecture

- Last lecture we calculated the total output noise from a two-port by ignoring the correlation of the input noise generators.

- The equivalent noise *voltage* is given by

$$v_{eq} = v_n + Z_S i_n$$

- Last lecture we assumed uncorrelated noise sources, so $\overline{v_{eq}^2} = \overline{v_n^2} + |Z_S|^2 \overline{i_n^2}$

- If we take the correlation into account, our results will be true for a general circut.

Correlated Noise Sources

- Let's partition the input noise current into two components, a component correlated ("parallel") to the noise voltage and a component uncorrelated ("perpendicular") of the noise voltage

$$i_n = i_c + i_u$$

- where we assume that $< i_u, v_n >= 0$ and

$$i_c = Y_C v_n$$

- We can therefore write

$$v_{eq} = v_n(1 + Y_C Z_S) + Z_S i_u$$

Noise Figure of Two-Port

- Which is a sum of uncorrelated random variables. The variance is thus the sum of the variances

$$\overline{v_{eq}^2} = \overline{v_n^2}|1 + Y_C Z_S|^2 + |Z_s|^2\overline{i_u^2}$$

- This allows us to immediately write the noise figure as

$$F = 1 + \frac{\overline{v_n^2}|1 + Y_C Z_S|^2 + |Z_s|^2\overline{i_u^2}}{\overline{v_s^2}}$$

- Let $\overline{v_n^2} = 4kTBR_n$, $\overline{i_u^2} = 4kTBG_u$, and $\overline{v_s^2} = 4kTBR_s$. Then

$$F = 1 + \frac{R_n|1 + Y_C Z_S|^2 + |Z_s|^2 G_u}{R_s}$$

Optimum Source Impedance

- If we let $Y_c = G_c + jB_c$, $Y_s = Z_s^{-1} = G_s + jB_s$, it's not to difficult to show that the optimum source impedance to minize F is given by

$$B_{opt} = B_s = -B_c$$

$$G_{opt} = G_s = \sqrt{\frac{G_u}{R_n} + G_c^2}$$

- The minimum acheivable noise figure is

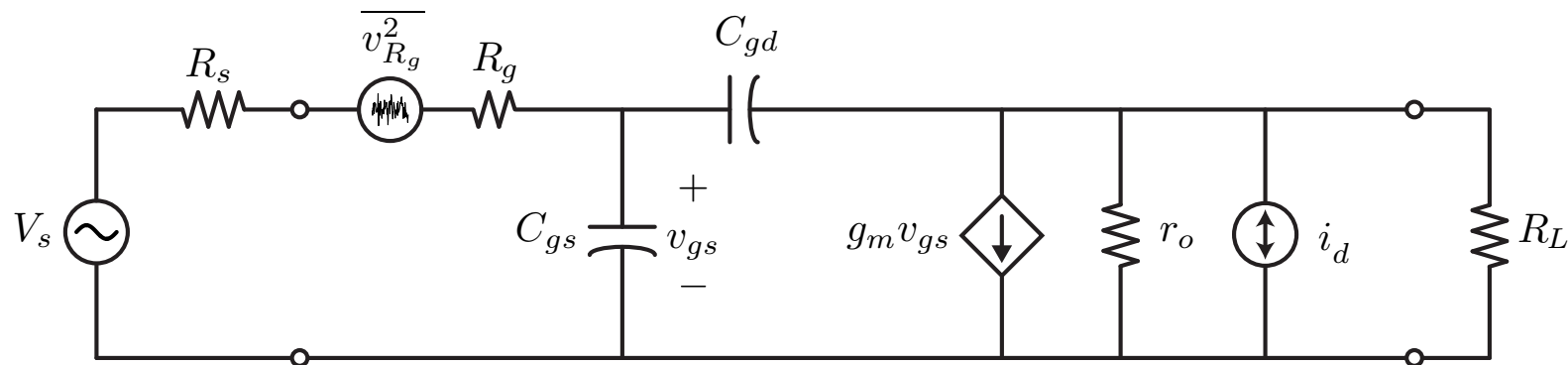$$F_{min} = 1 + 2R_n \left[\sqrt{\frac{G_u}{R_n} + G_c^2} + G_c \right]^2$$

Minimum Noise F_{min}

- Very similar to last lecture, we have

$$F = F_{min} + \frac{R_n}{G_s}|Y_s - Y_{opt}|^2$$

- This equation stats that if the source impedance $Y_s \neq Y_{opt}$, the noise figure will be larger by a factor of the "distance" squared times the factor R_n/G_s.

- A good device should have a low R_n so that the noise match is not too sensitive.

FET Common Source Amplifier

- Consider the following noise sources:

$$R_s \qquad \overline{v_s^2} = 4kTBR_s$$

$$R_g \qquad \overline{v_g^2} = 4kTBR_g$$

$$R_{ch} \qquad \overline{i_d^2} = 4kTBg_{d0}\gamma B$$

$$R_L \qquad \overline{i_L^2} = 4kTBG_L$$

Total FET Drain Noise

- Summing all the noise at the output (assume low frequency)

$$\overline{i_o^2}^2 = \overline{i_d^2} + \overline{i_L^2} + (\overline{v_g^2} + \overline{v_s^2})g_m^2$$

- Which results in the noise figure

$$F = 1 + \frac{\overline{v_g^2}}{\overline{v_s^2}} + \frac{\overline{i_d^2} + \overline{i_L^2}}{g_m^2 \overline{v_s^2}}$$

$$= 1 + \frac{R_g}{R_s} + \frac{g_{d0}\gamma + G_L}{R_s g_m^2}$$

FET Noise Figure (low freq)

- Assume $g_m = g_{d0}$ (long channel)

$$= 1 + \frac{R_g}{R_s} + \frac{\gamma}{g_m R_s} + \frac{G_L G_S}{g_m^2}$$

- If we make g_m sufficiently large, the gate resistance will dominate the noise.

- The gate resistance has two components, the physical gate resistance and the induced channel resistance

$$R_G = R_{poly} + \delta R_{ch} = \frac{1}{3} \frac{W}{L} R_\square + \frac{1}{5} \frac{1}{g_m}$$
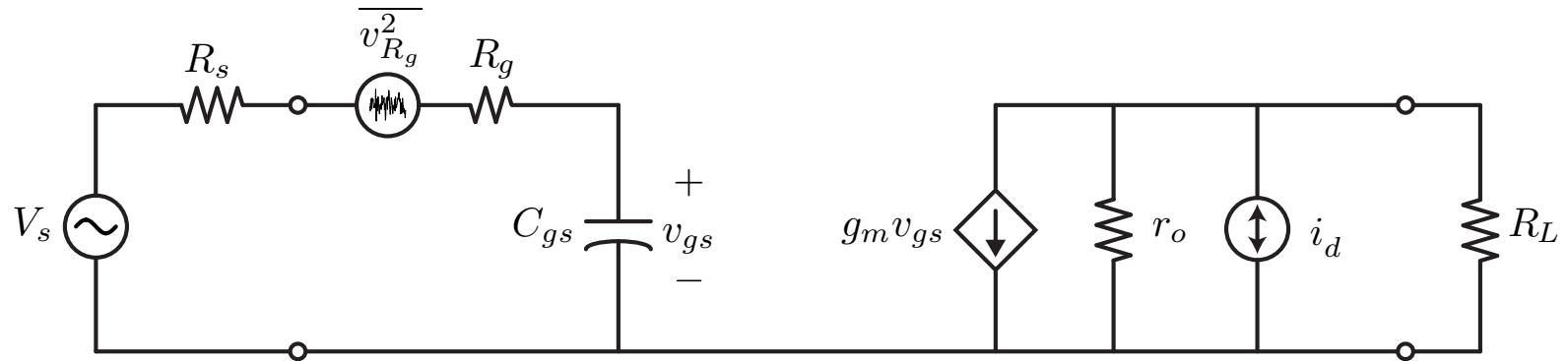
- The factors $1/3$ and $1/5$ come from a distributed analysis (EECS 117). They are valid for single-sided gate contacts.

FET Layout
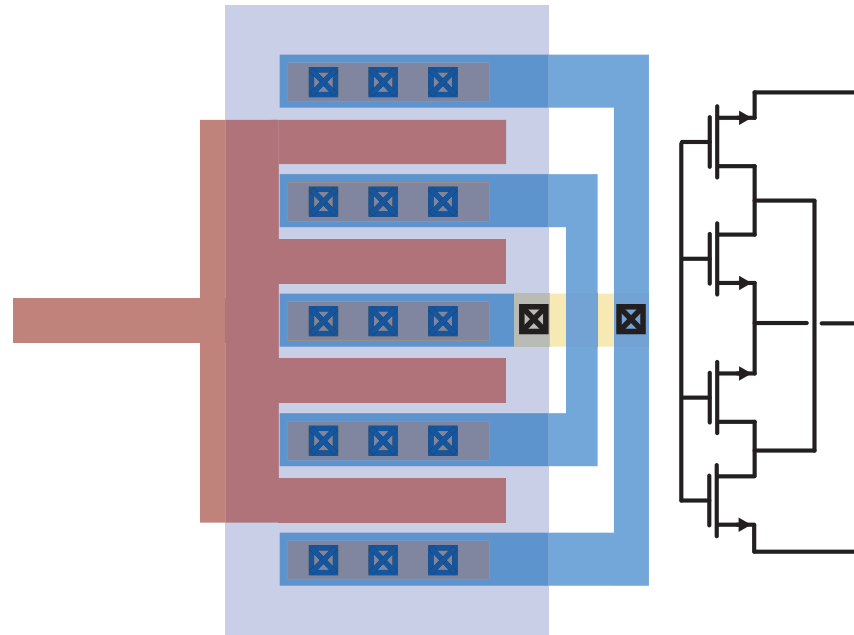
🔴 To reduce the gate resistance, a multi-finger layout approach is commonly adopted. As a bonus, the junction capacitance is reduced due to the junction sharing.

CS Noise at Medium Frequencies

- If we repeat the calculation at medium frequencies, ignoring C_{gd}, we simply need to input refer the drain noise taking into account the frequency dependence of G_m

$$G_m = \frac{1/(j\omega C_{gs})}{1/(j\omega C_{gs}) + R_s + R_g}$$

$$= \frac{1}{1 + j\omega C_{gs}(R_s + R_g)}$$

CS Noise (cont)

- The drain noise is input referred by the magnitude squared

$$|G_m|^{-2} = 1 + \omega^2 C_{gs}^2 (R_s + R_g)^2$$

- So the noise figure is simply given by (neglect the noise of R_L)

$$F = 1 + \frac{R_g}{R_s} + \frac{\gamma}{\alpha} \left(1 + \omega^2 C_{gs}^2 (R_S + R_g)^2\right)$$

- Assume that $g_m R_S \gg 1$ and $R_s \gg R_g$ (good layout). The "high" frequency noise is given by

$$F_\infty = 1 + \frac{\gamma}{\alpha} \frac{\omega^2 C_{gs}^2 R_s^2}{g_m R_S} = 1 + \frac{\gamma}{\alpha} \left(\frac{\omega}{\omega_T}\right)^2 g_m R_s$$

MOSFET LNA Design

- Two important specifications for an LNA are a power impedance match and low noise figure. We see that the noise figure of an LNA using MOSFETs can be made low by increasing the g_m of the device and with proper layout (multi-finger device).

- But the gate of a MOSFET is predominantly capacitive which presents a bad match to 50Ω

- Do we really need to do a power match? We may be willing to give up some gain. Is this a wise decision?

To Match or Not to Match?

$Z_{in} = ?$

Z_0

$Z_{in} \neq Z_0$
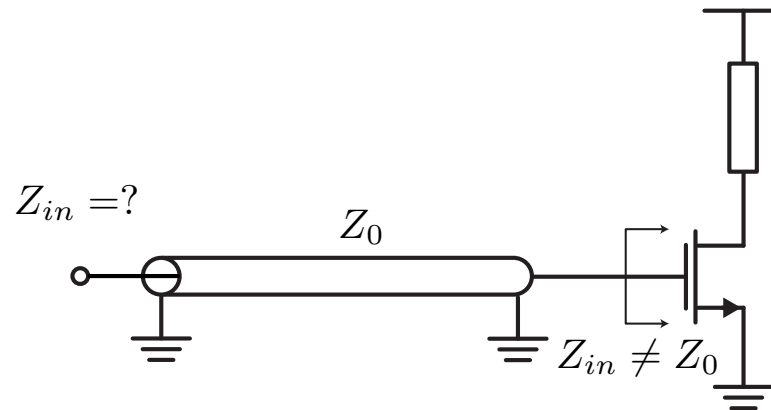
- An age old question in RF is the requirement to match. Is it necessary?

- Imagine that the input impedance is not matched. Now imagine the path from the antenna to the amplifier. It will usually go through a transmission line, either a cable or through PCB traces, before reaching the LNA.

To Match or Not to Match? (cont)

- If the LNA input is not matched, the impedance seen by the antenna depends on the length of this transmission line (EECS 117). This is a bad situation because we cannot predict how much power will reach the LNA !

- But if we match, then you're certain that regardless of the length of the T-line, the input power is well known and fixed. Furthermore, if a filter precedes the LNA (very common), the filter must be terminated properly to operate with low insertion loss.

- How about simply terminating the input gate with a resistor equal to R_s? If the capacitance of the gate is low, the input impedance will be mostly 50Ω.

Input Termination

- Let's take the most optimistic situation where the MOSFET noise is negligible. Then the noise figure due to the input termination resistor is bounded by
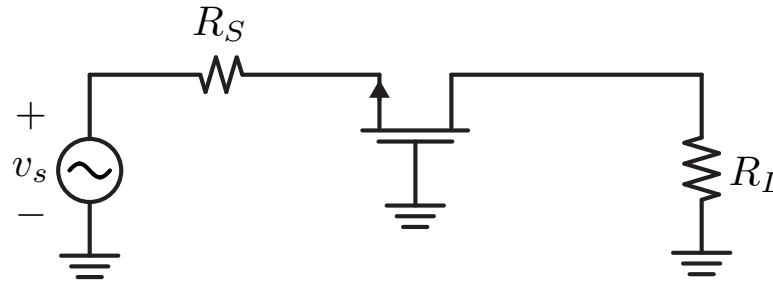
$$F > 1 + \frac{\overline{v_{eq}^2}}{\overline{v_s^2}} = 2$$

- The termination adds $3\,\mathrm{dB}$ of noise figure! In sub-dB applications this is totally intolerable. In other applications, though, this may be a cheap and simple solution.

Z_L

$Z_{in} \approx Z_0$

Z_0
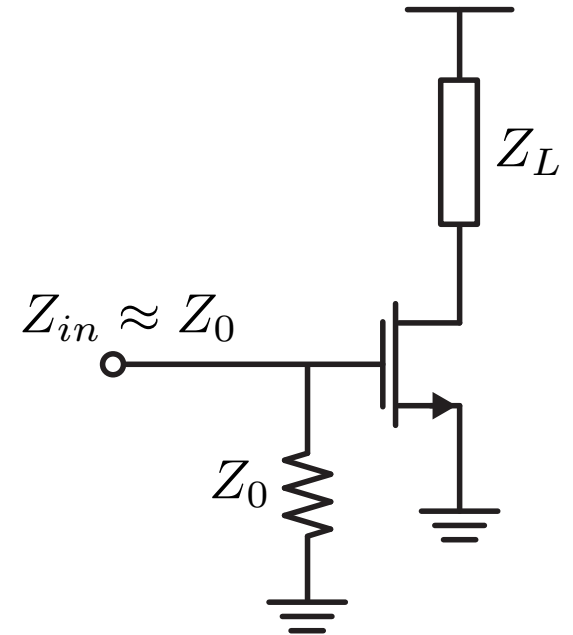
Common Gate LNA

- A common gate LNA can impedance match by choosing $g_m = G_s$. For a FET this requires a high current (due to lower g_m) for $R_s = 50\Omega$.

- Let's calculate the noise figure by just considering the effect of the drain current. Since the drain current is injected into the input, it adds noise in shunt with the input noise current

$$F > 1 + \frac{\overline{i_d^2}}{\overline{i_s^2}}$$

Common Gate LNA (cont)

- Substitute $\overline{i_s^2} = 4kTBG_s$ and $\overline{i_d^2} = 4kT\gamma g_{ds0} = 4kT\frac{\gamma}{\alpha}g_m$ and further note that $g_m = G_s$
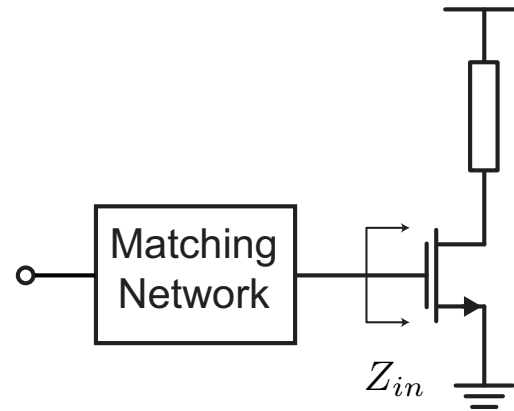
$$F > 1 + \frac{\gamma g_m}{\alpha G_s} = 1 + \frac{\gamma}{\alpha}$$

- $\gamma/\alpha = 2/3$ for a long channel device. For short channel devices, this is about 2.

$$F \geq 1 + \frac{\gamma}{\alpha} \approx 2 - 3$$

- The noise figure is large relative to F_{min}. The common source amplifier is attractive since it's noise can be made close to the F_{min} of the device.

LC Matched LNA

- We can always match the input impedance of an LNA to 50Ω using one of the matching circuits we studied earlier.

- But the matching network will also transform R_s and it may worsen the noise figure (by moving R_s further away from $R_{S,opt}$.

LC Match (cont)

- Another issue is that the input resistance of the FET is quite small (series resistance). Recall that

$$Z_g = \frac{1}{j\omega C_{gs}} + R_i + R_G \approx R_i + \frac{1}{j\omega C_{gs}}$$

- where for a good layout we have minimized the gate resistance R_G. The intrinsic channel resistance is related to the device g_m

$$Z_g = \frac{1}{5g_m} + \frac{1}{j\omega C_{gs}}$$

- Since the real part is typically rather small, the Q factor of the matching network may be quite large.