Low power Radio Circuits

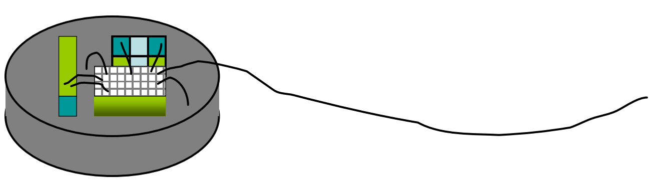
EE 142 Guest Lecture

Alyosha Molnar

Overview: Smart Dust Radio

Goal: A radio for sensor nodes which contain: sensors, ADC, μP and ~1kB RAM

- **Cost: <$1, so few off-chip components:**
  - Battery (3V Li coin cell)
  - Crystal (for network sync)
  - Antenna
  - High-Q inductor
  - 0.25μm



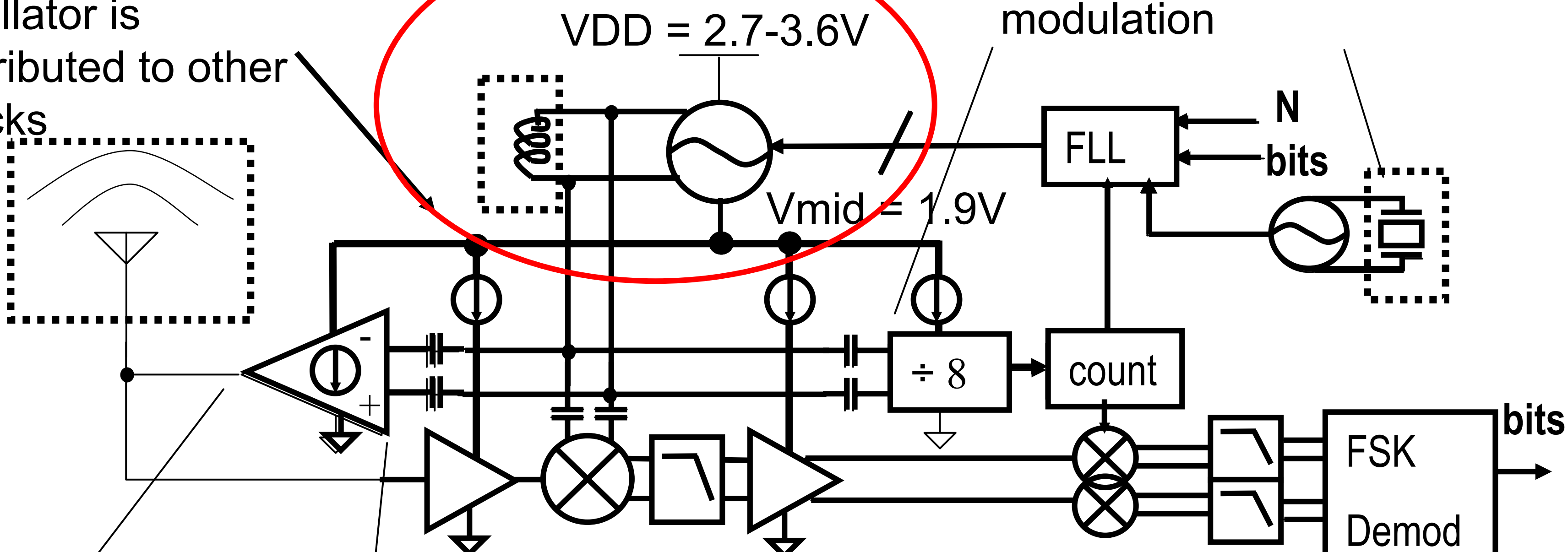
- **Performance**:
  - range ≤10m
  - data rate: ~100kb/s
  - <1% duty cycle
  - Battery life ~5yrs
- **Low power:1mW**
  - Stack circuits to reuse current
  - Drive RF gates from high-Q LC oscillator

Top level

Bias stacking: current from oscillator is distributed to other blocks

900MHz RF oscillator:
Tunes out all RF gates
Sets minimum current

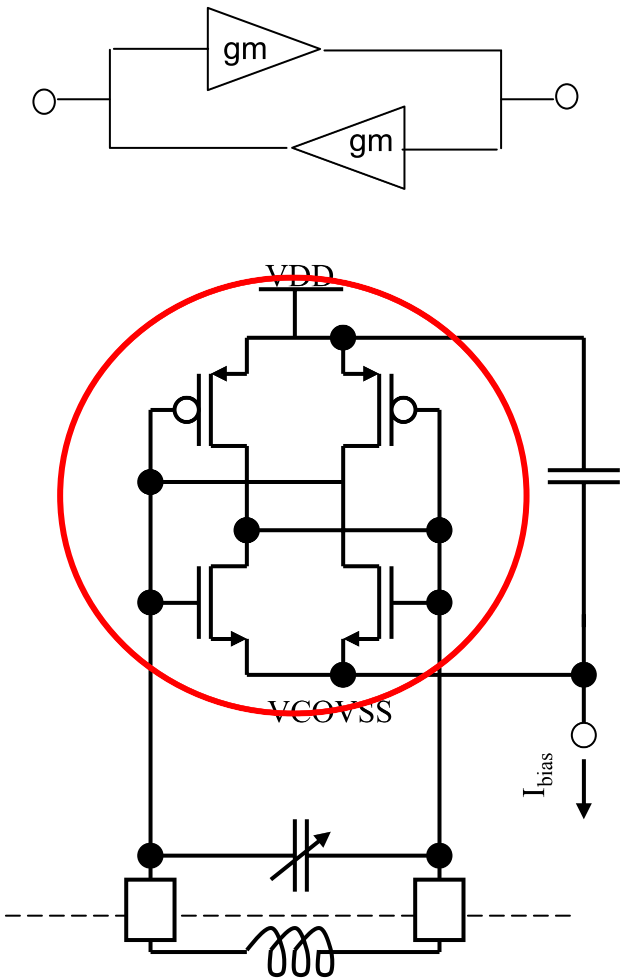
Frequency control: sets channel, FSK modulation



Transmitter: drives ~200µW signal to antenna

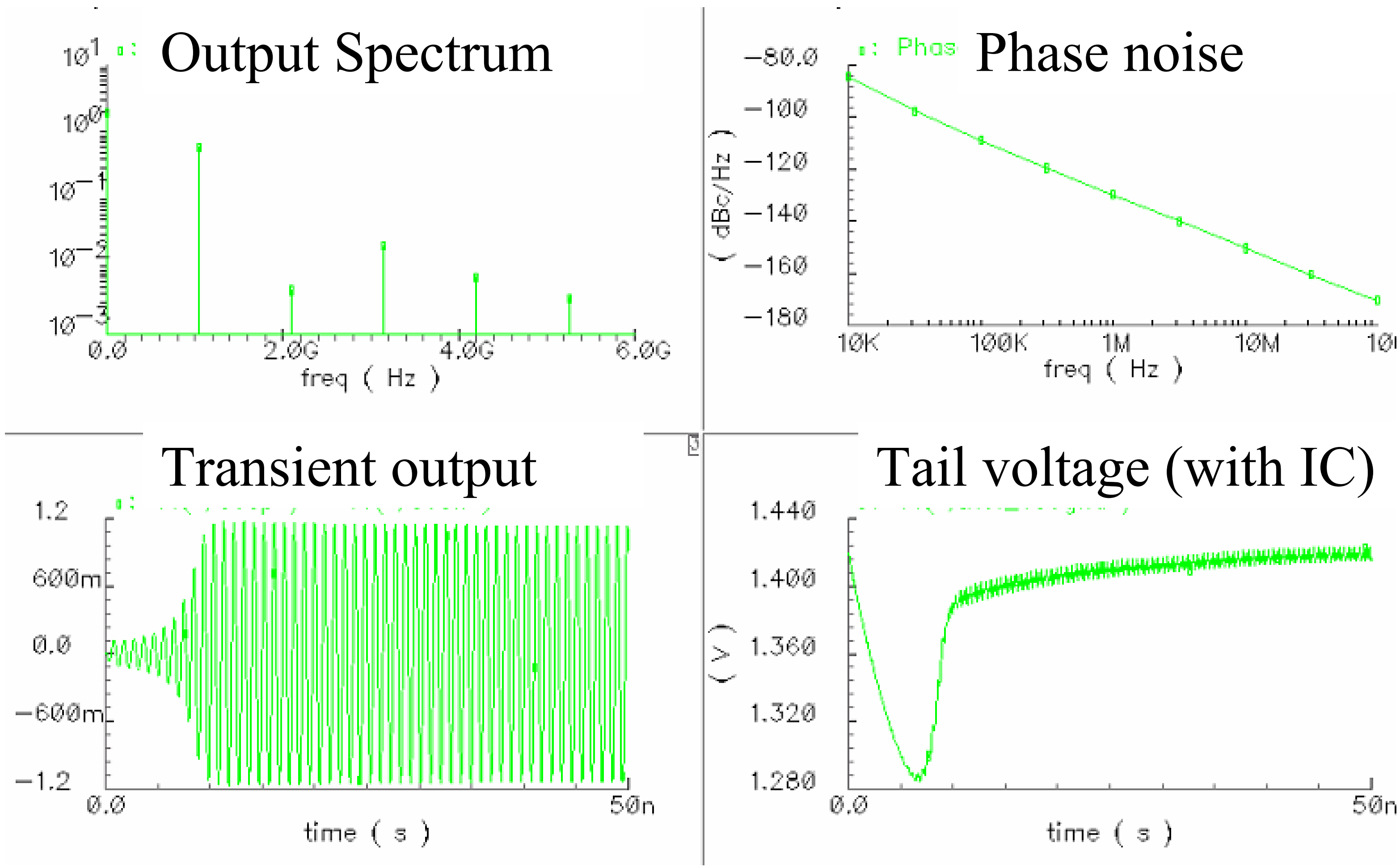
Receiver: detects, down-converts and demodulates RF signals from antenna

Oscillator

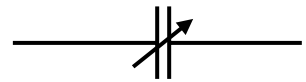


- Cross-coupled inverters form a negative resistance.
- Tuning:
  - 902MHz-928MHz
  - ± 5% for process
  - ± 2.5% for inductor
- L = 17nH, Q = 30
- Swing = 1Vpeak
- Ibias = 200-300μA

Simulations (unloaded)

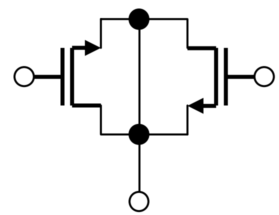


Capacitor array



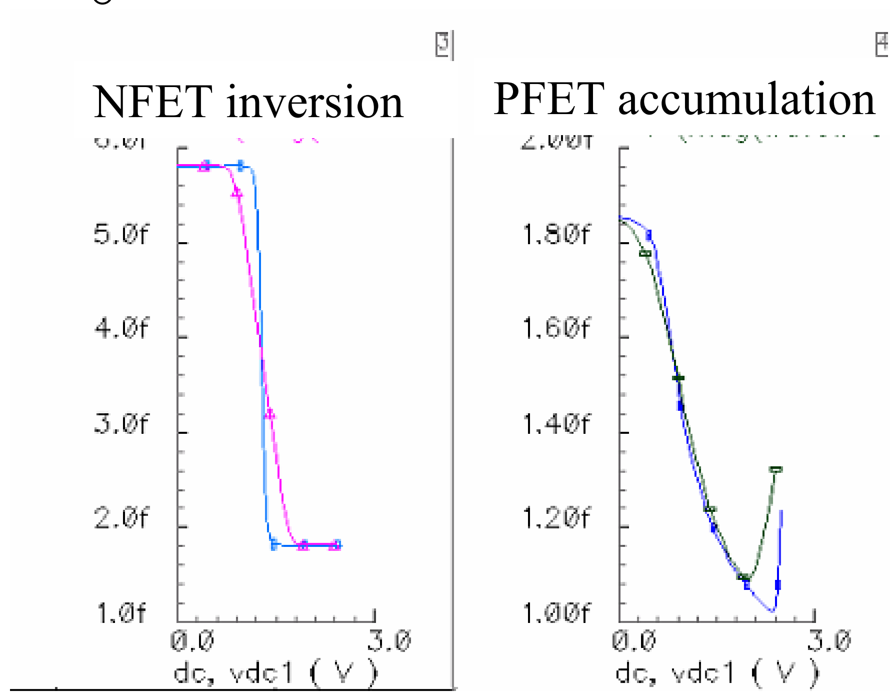
Made up of :

- Three 4-bit binary arrays of inversion capacitors
- An extra MSB
- A 4-bit DAC driving a near-minimum PFET varactor

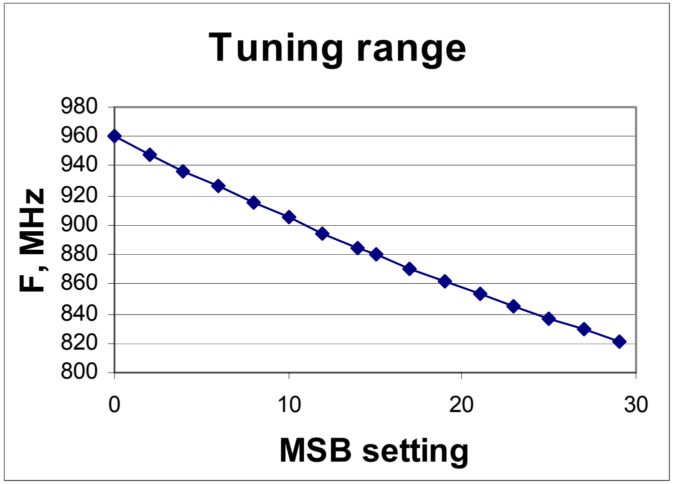


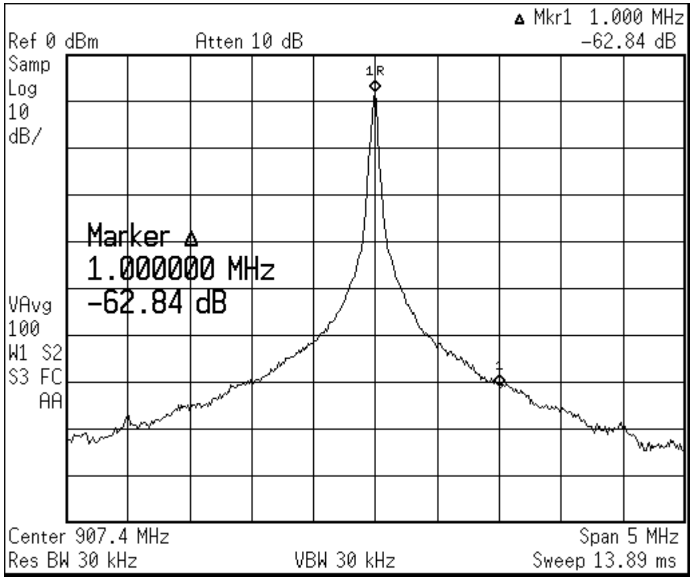
Inversion cap:
(Q*Con/Coff) is about 6x better than a normal switch plus capacitor

array	min step (MHz)	range (MHz)
varactor	0.01	0.1
min cap	0.07	0.99
mid cap	0.89	12.29
max cap	11.69	142.14



Oscillator results





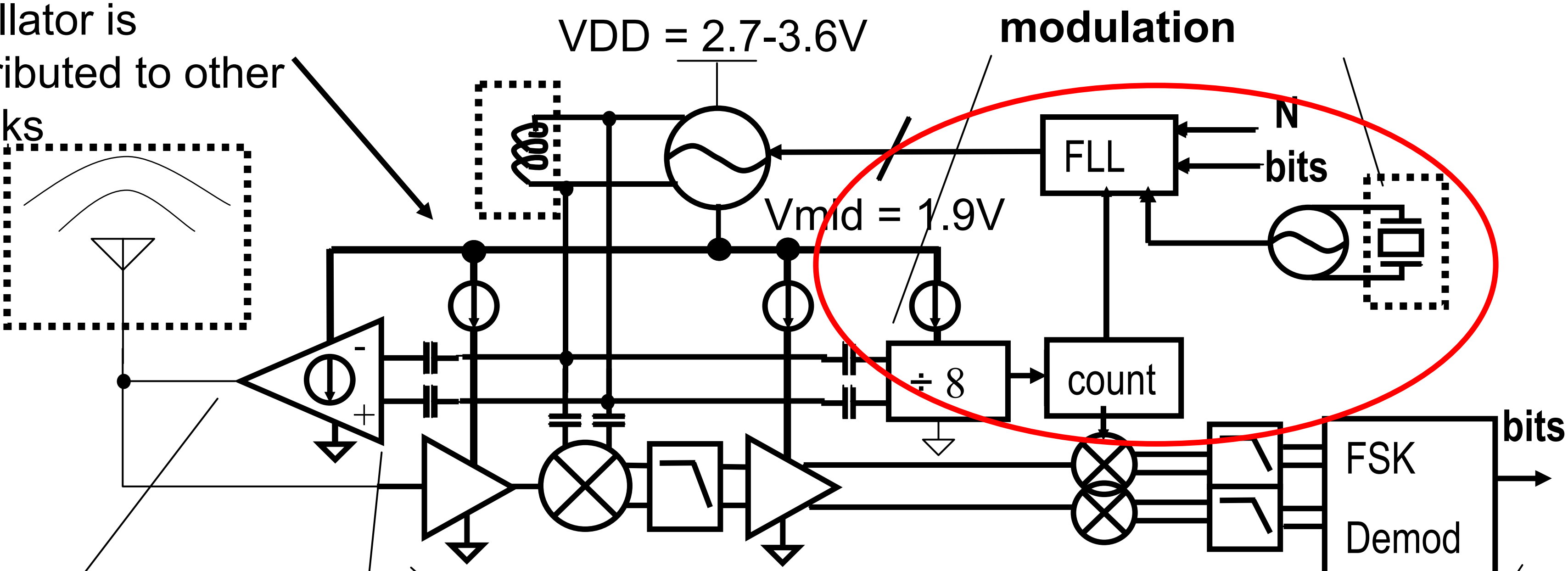
- Tuning from 820MHz to 960MHz
- LSB precision of 2.6 kHz
- Phase noise @ 1MHz = -107dBc
- PN rolls off @ 40dB/dec below 1MHz, 20dB/dec above.
- Noise is bias dominated.
- Oscillator starts to squegg for Ibias below 200µA (220µW)

Top level

900MHz RF oscillator:
Tunes out all RF gates
Sets minimum current

Bias stacking:
current from
oscillator is
distributed to other
blocks

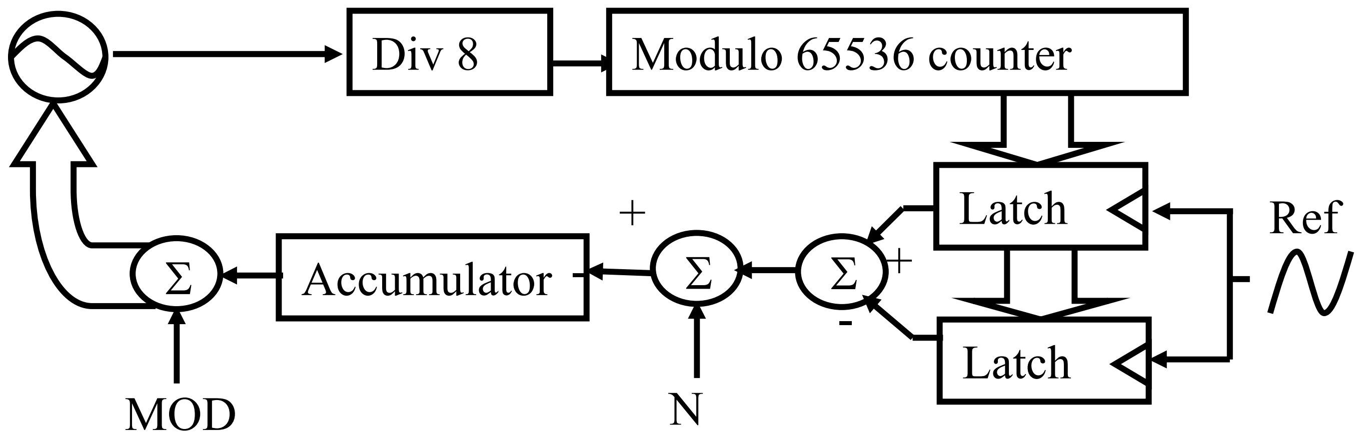
**Frequency control:
sets channel, FSK
modulation**



Transmitter:
drives ~200μW
signal to
antenna

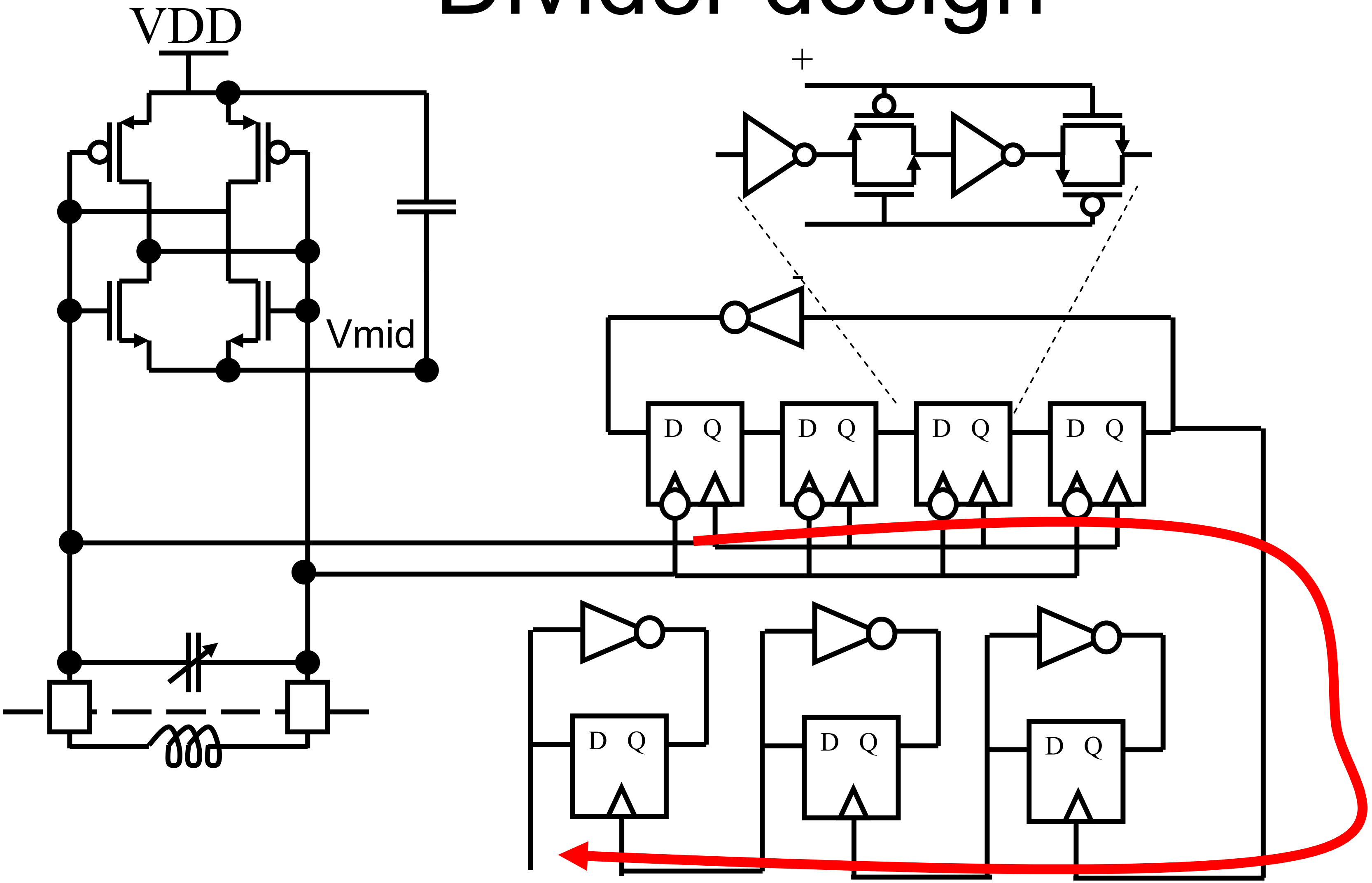
Receiver: detects, down-converts and
demodulates RF signals from antenna

Frequency control loop (FLL)

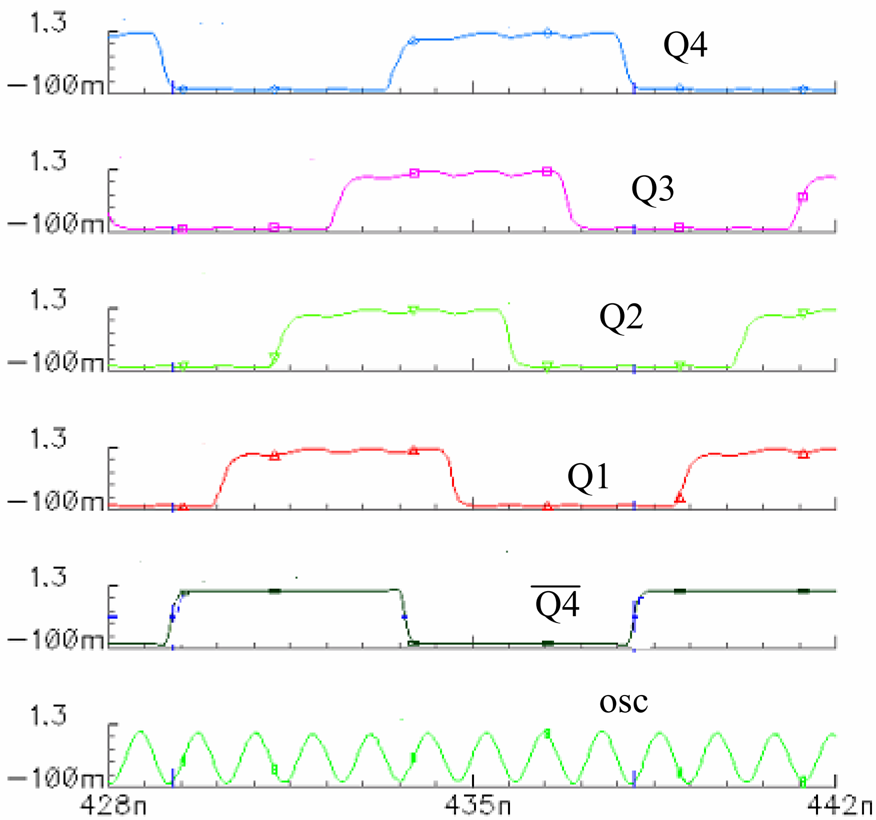


- Have Crystal oscillator for network synchrony.
- RF Oscillator control is digital.
  - Crystal samples continuously running counter.
  - Subtracting successive samples gives F_{RF}/F_{ref}.
- Early counter stages set power, so
  - Use some custom logic.
  - divide-by-8 before counter

Divider design

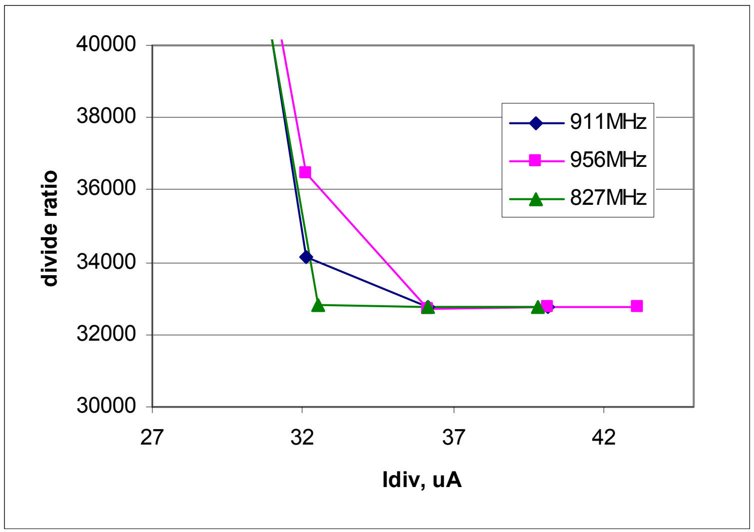


Ring Divider Simulation



- Four stages with ~1ns delay set by input.
- Extra inverter incorporating reset capability.
- Fails by dividing by 9 (extra inverter causes cyclic slip).

Divider/FLL results



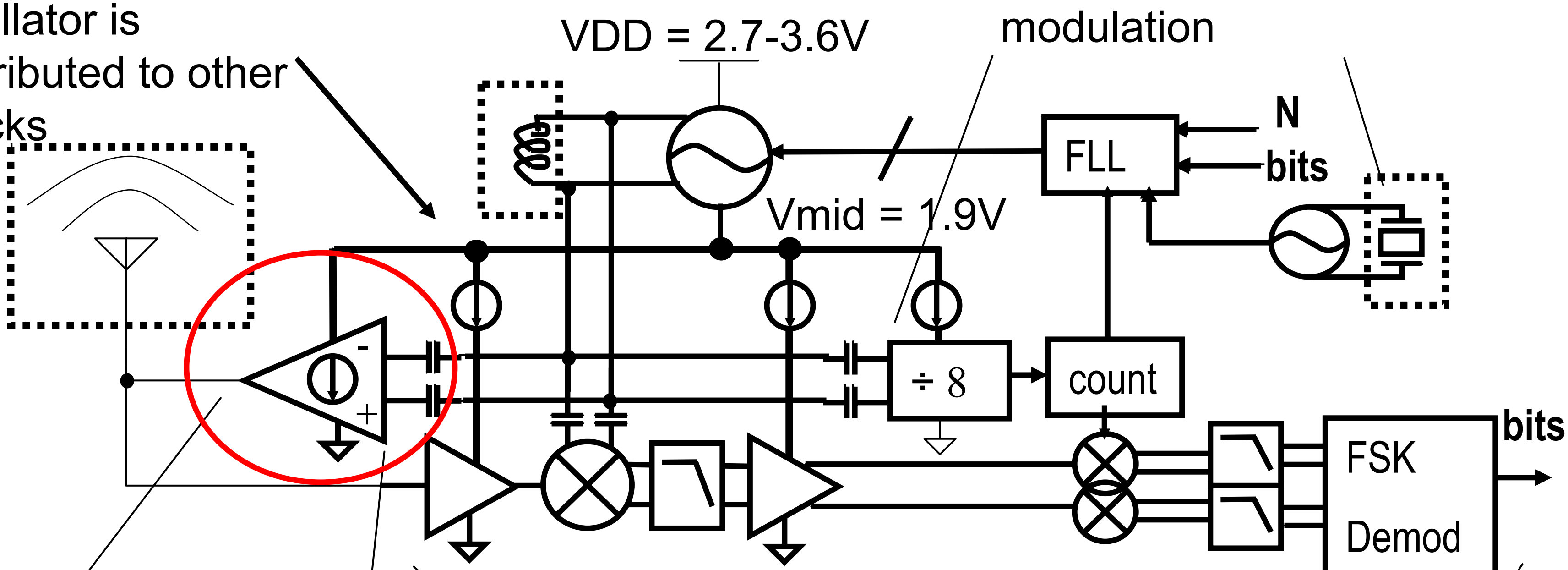
- FLL works
  - Accurately sets frequency
  - Stabilizes Frequency under bias perturbations
- Divider fails at low currents by under counting.
- Requires ~ 55μW

Top level

900MHz RF oscillator:
Tunes out all RF gates
Sets minimum current

Bias stacking:
current from
oscillator is
distributed to other
blocks

Frequency control:
sets channel, FSK
modulation



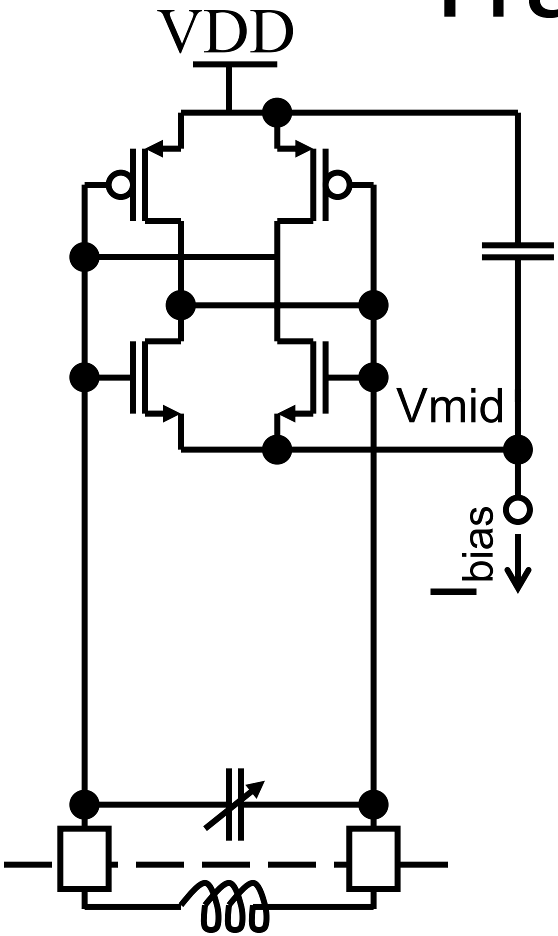
Transmitter:
drives ~200μW
signal to
antenna

Receiver: detects, down-converts and
demodulates RF signals from antenna

Transmitter

- Transmitter is just a buffering of the oscillator.
- Want to transmit 100-300uW
- Simple antennas have impedance of ~100 ohms.
- For low cost, impedance matching is limited to a series inductor (can be part of the antenna).
- This implies the driver must source a 1mA, 200mV rms signal from a 3V supply: this will be inefficient!
- So stack two amplifiers and reuse bias.

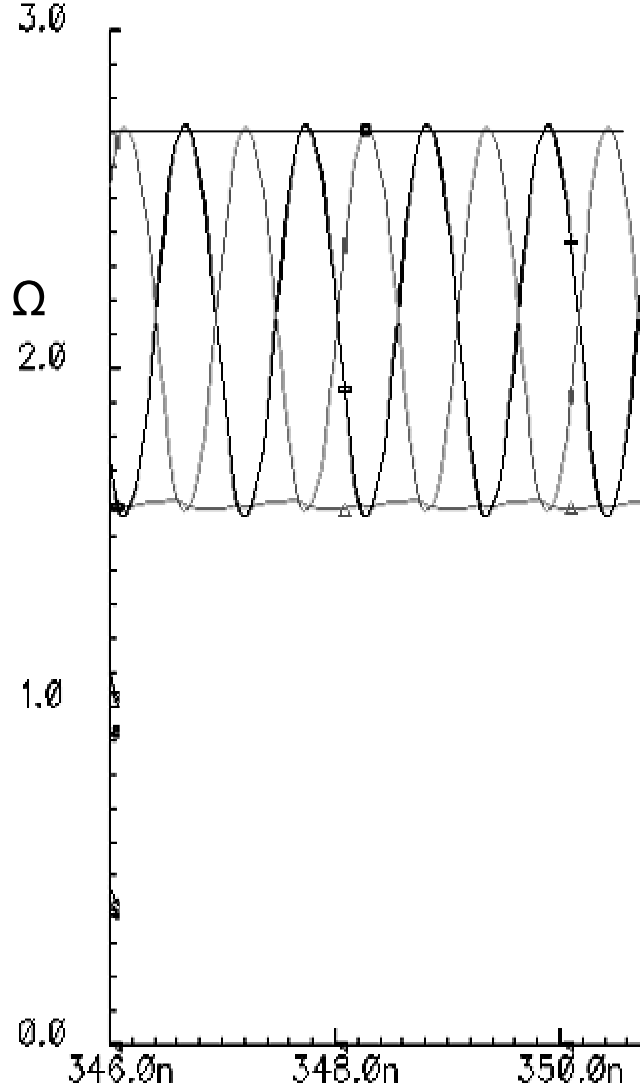
Transmitter design



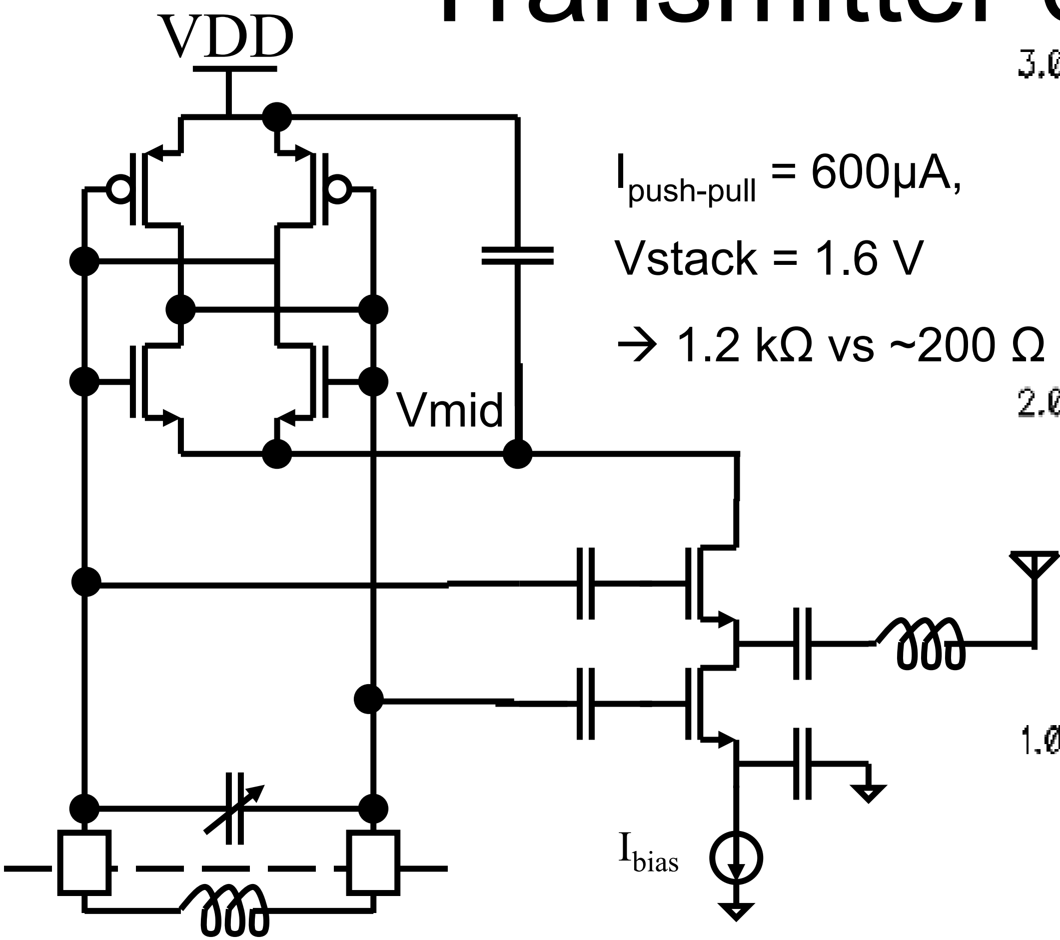
I_{bias} = 300µA,

Vmid = 1.6 V

→ 2.4 kΩ vs ~200 Ω



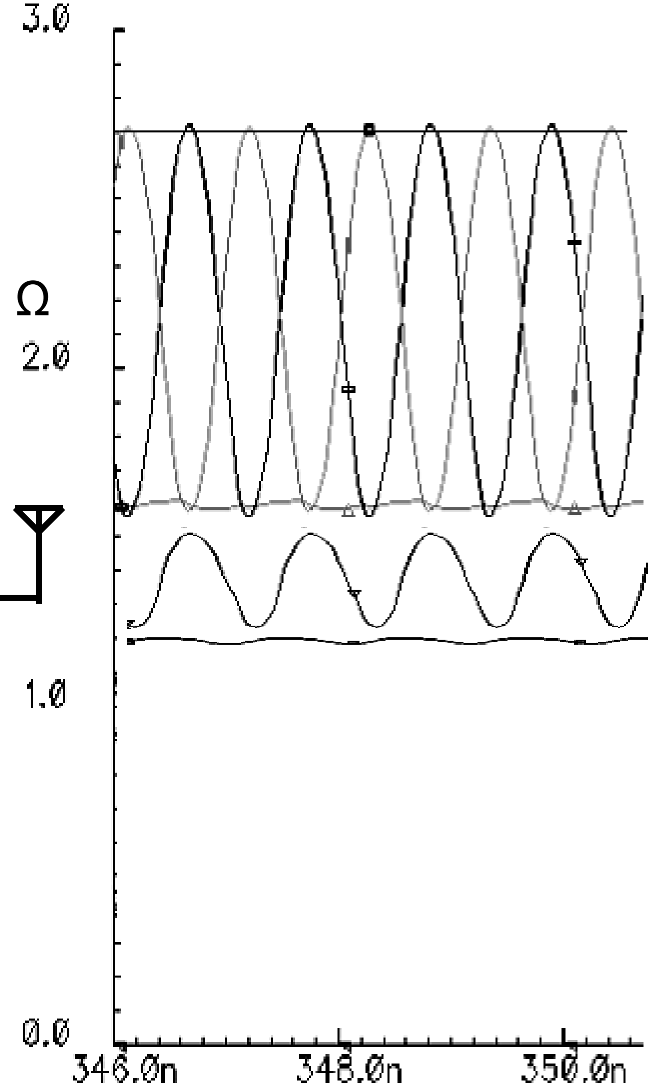
Transmitter design



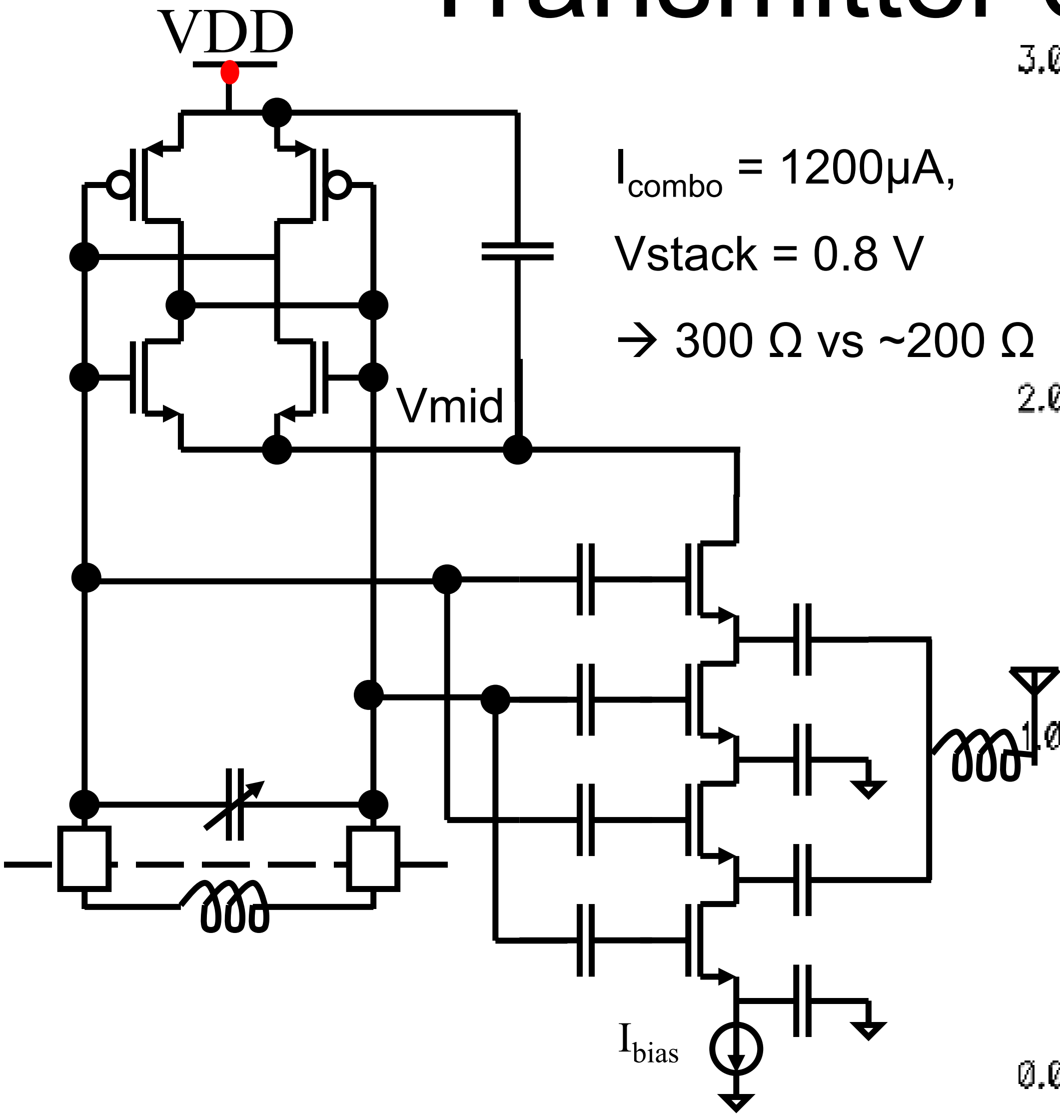
$I_{push\text{-}pull}$ = 600µA,

Vstack = 1.6 V

→ 1.2 kΩ vs ~200 Ω



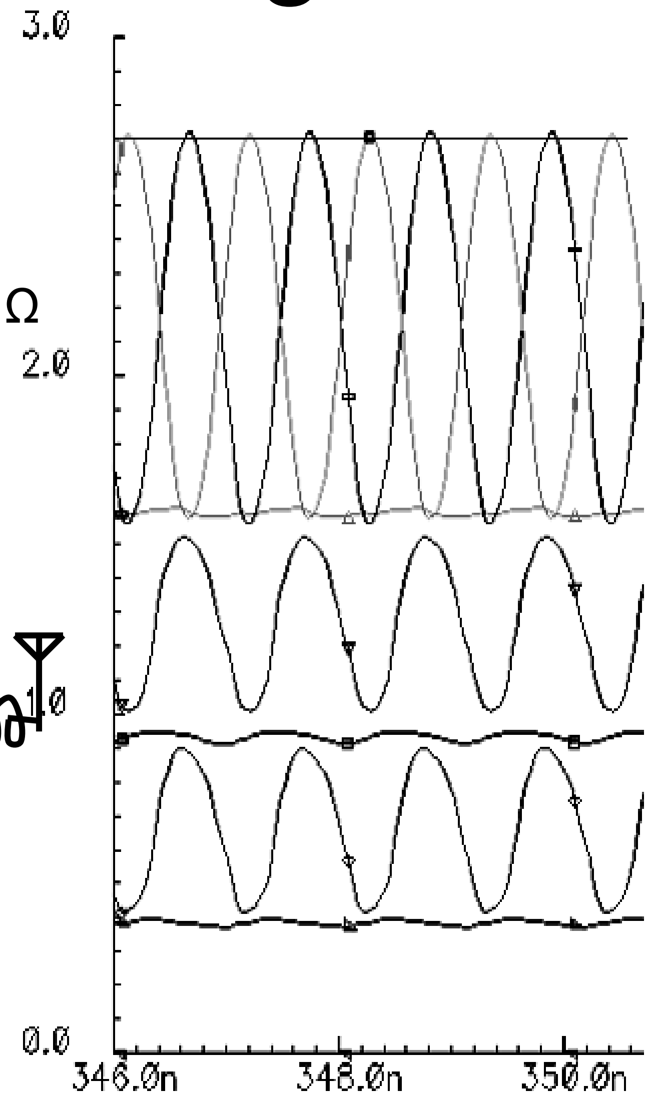
Transmitter design



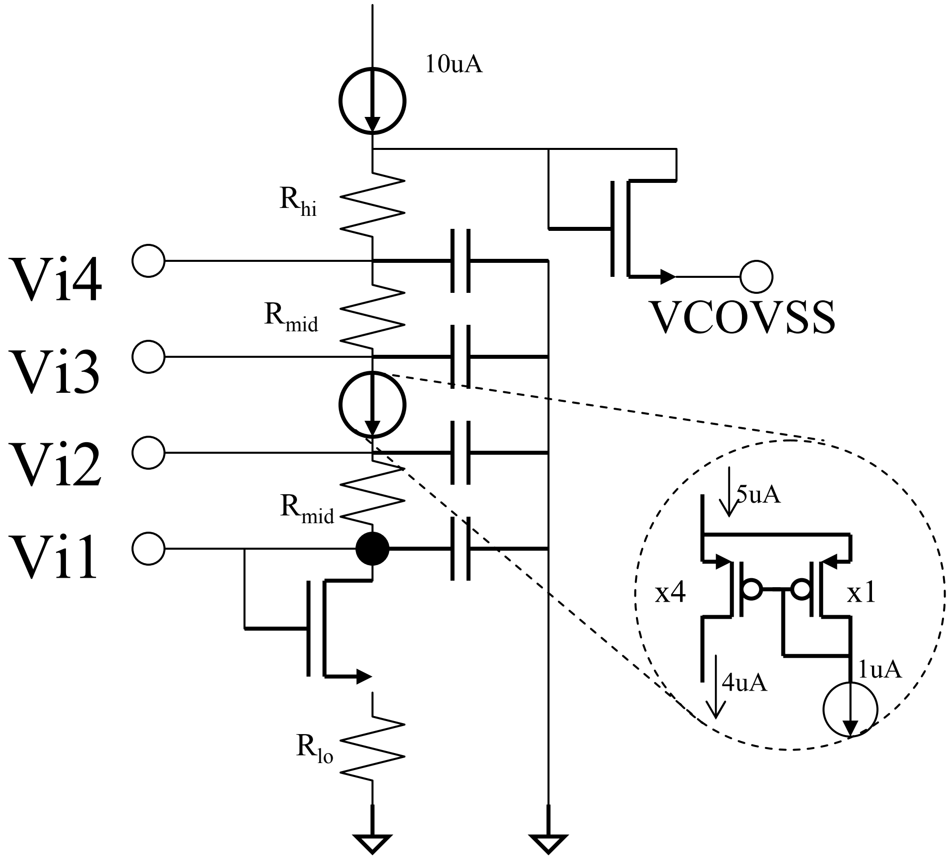
I_{combo} = 1200µA,

Vstack = 0.8 V

→ 300 Ω vs ~200 Ω



Bias Levels For Driver

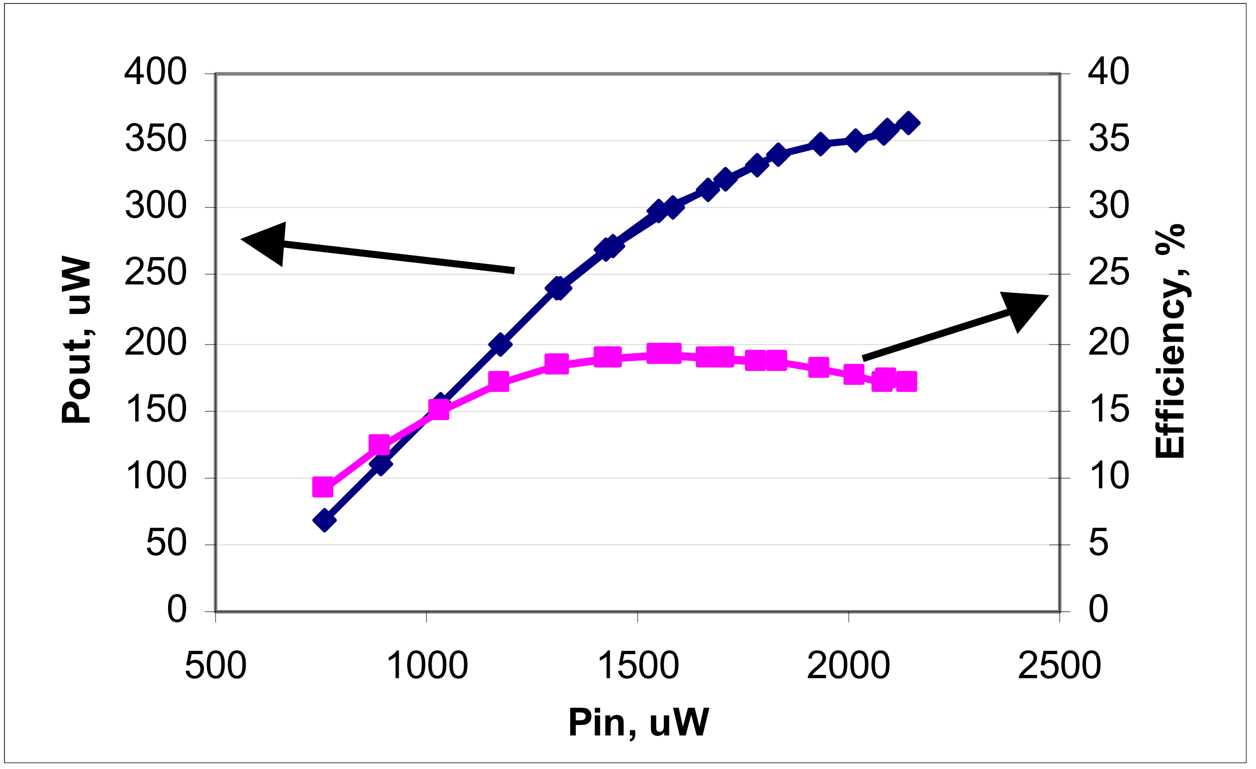


Need to set up bias levels for four transistors of antenna driver

Varying supply is taken up by current source at the middle:

Voltage delivered through 60kΩ minimum width resistors

Transmitter Results



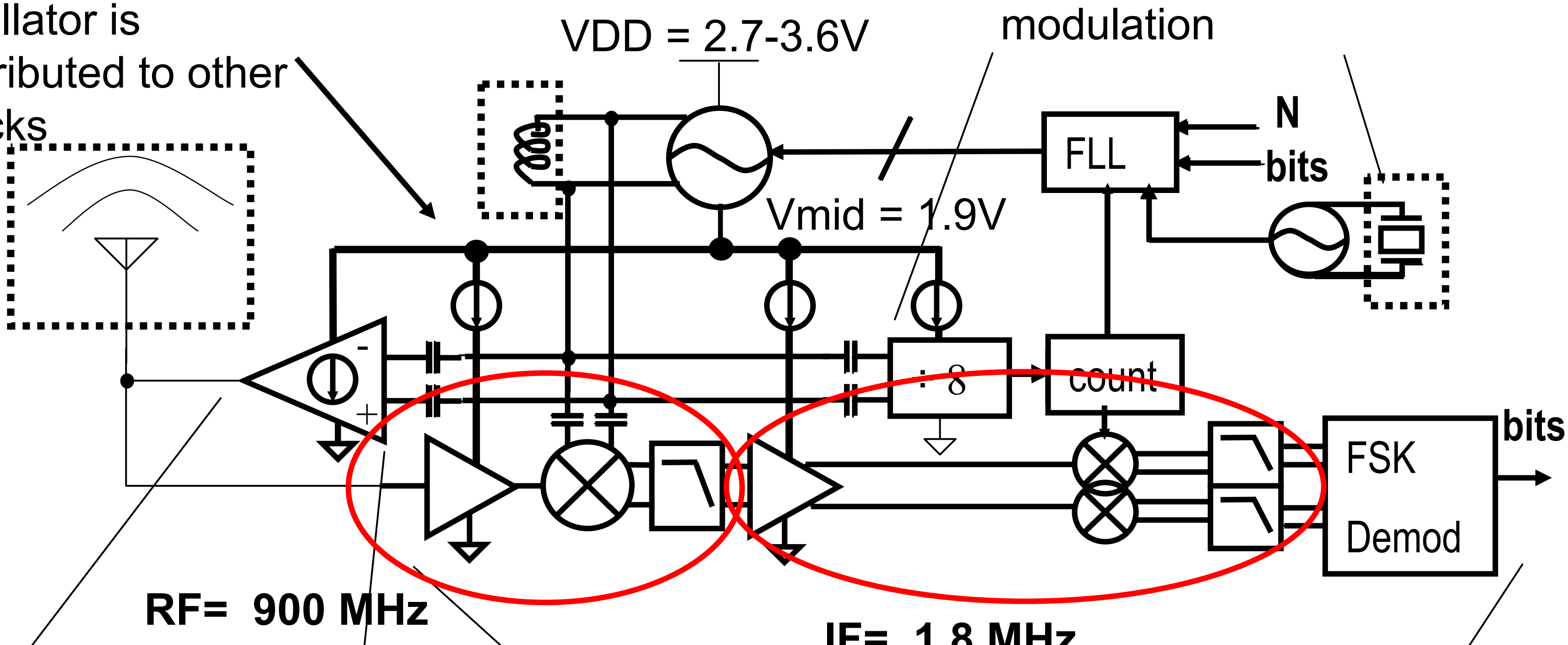
- Peak efficiency of 20% when radiating 300μW into 50Ω. (implies PA efficiency of >40%)
- Can radiate 1mW if reconfigured (efficiency~15%)

Top level

Bias stacking: current from oscillator is distributed to other blocks

900MHz RF oscillator:
Tunes out all RF gates
Sets minimum current

Frequency control: sets channel, FSK modulation

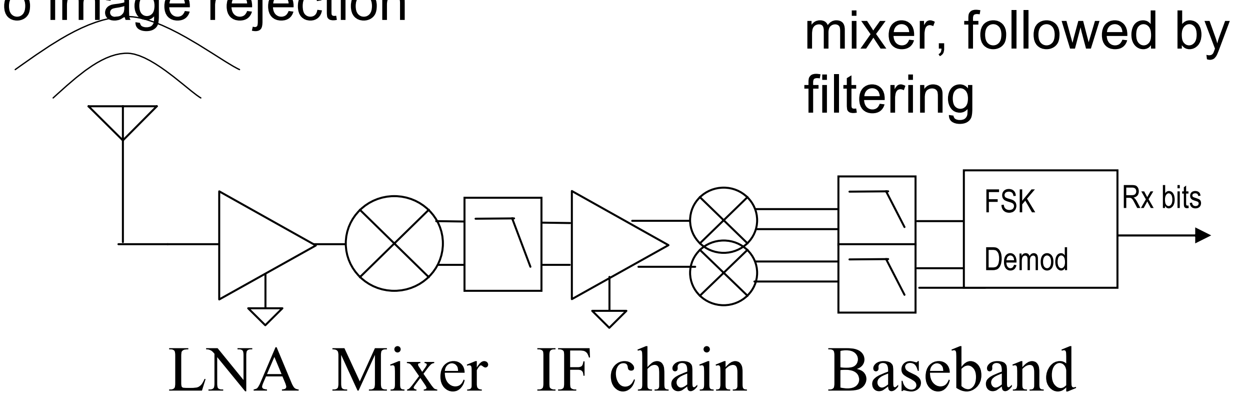


Transmitter: drives ~200μW signal to antenna

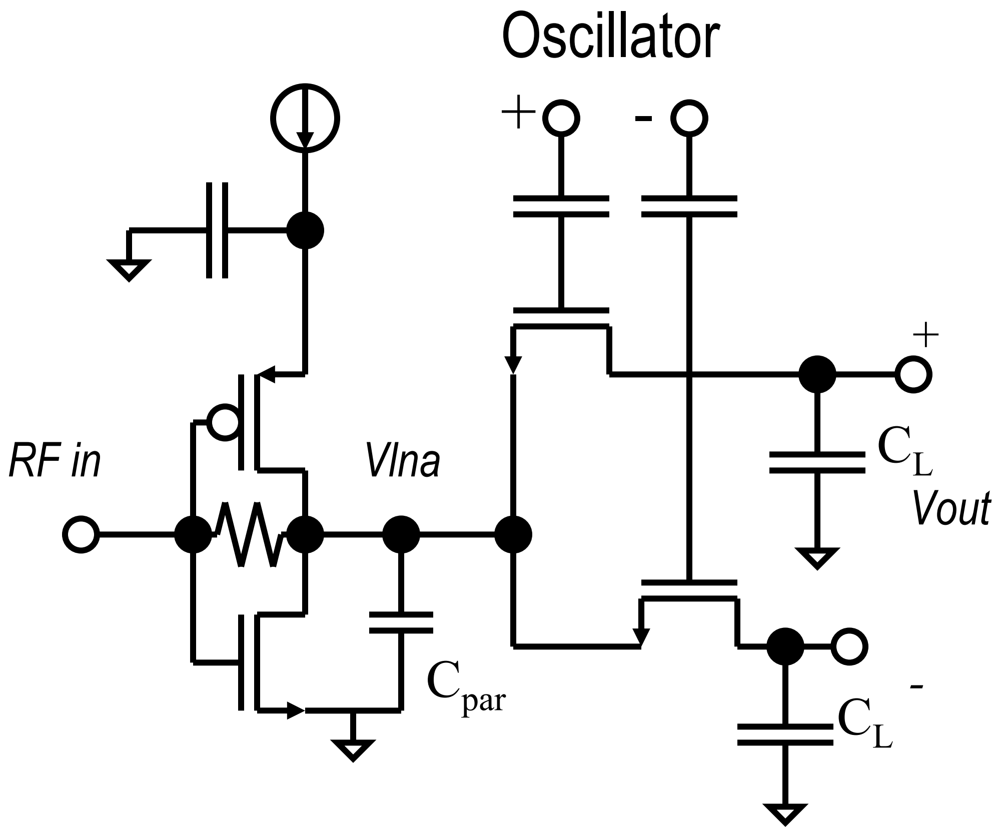
Receiver: detects, down-converts and demodulates RF signals from antenna

Receiver Overview

- Architecture:
  - Low power dictates Direct conversion or low IF.
  - Direct conversion suffers from DC offset, IP2, flicker noise
- Low IF receiver
  - Generate IF from LO.
  - No image rejection
- Sensitivity: ~-90dBm
  - Want high gain up front
  - NF set by LNA, so spend most bias current in LNA
- Interference
  - Mostly out-of-band (cell phones etc)
  - No SAW filter up front
  - So use linear, passive mixer, followed by filtering

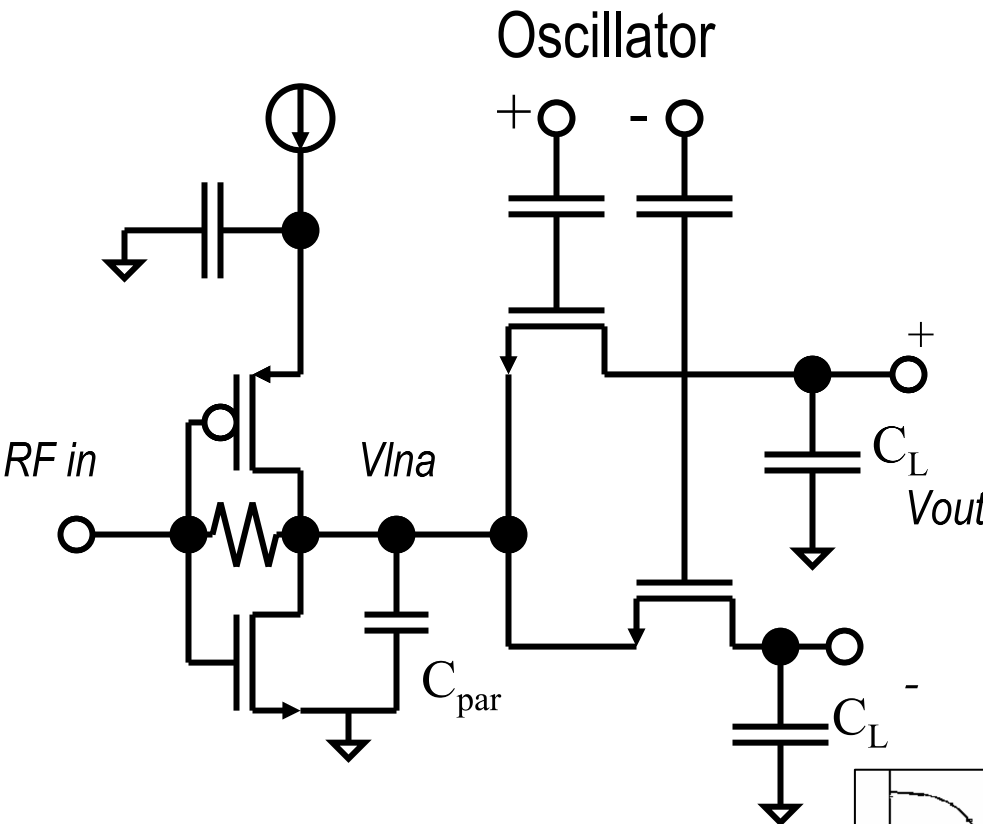


Rx Front End

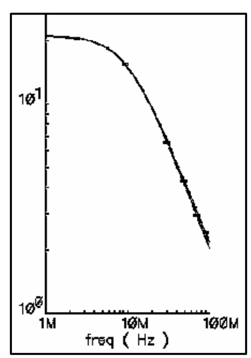


- **Resistively biased inverter as LNA.**
  - $A_v = 2Gm_{LNA} / (\omega_{LO} C_{par})$ *(20dB)*
  - NF ~*9dB*

Rx Front End

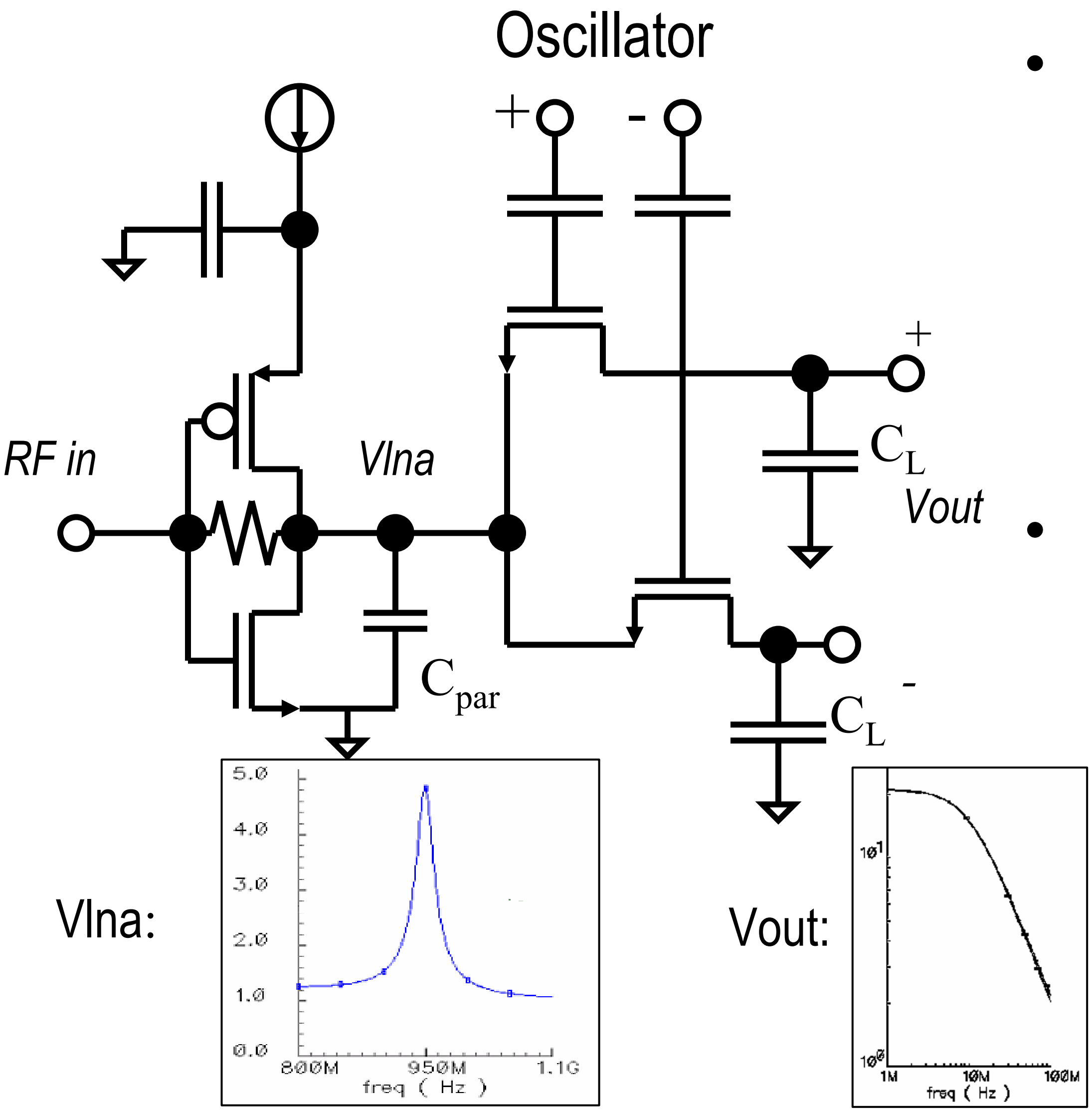


Vout:



- **Resistively biased inverter as LNA.**
  - Av = $2Gm_{LNA} /(\omega_{LO}C_{par})$ *(20dB)*
  - NF ~*9dB*
- **Passive mixer dissipates little power**
  - Vout: 1-pole LPF at $2F_{LO}C_p/C_L$

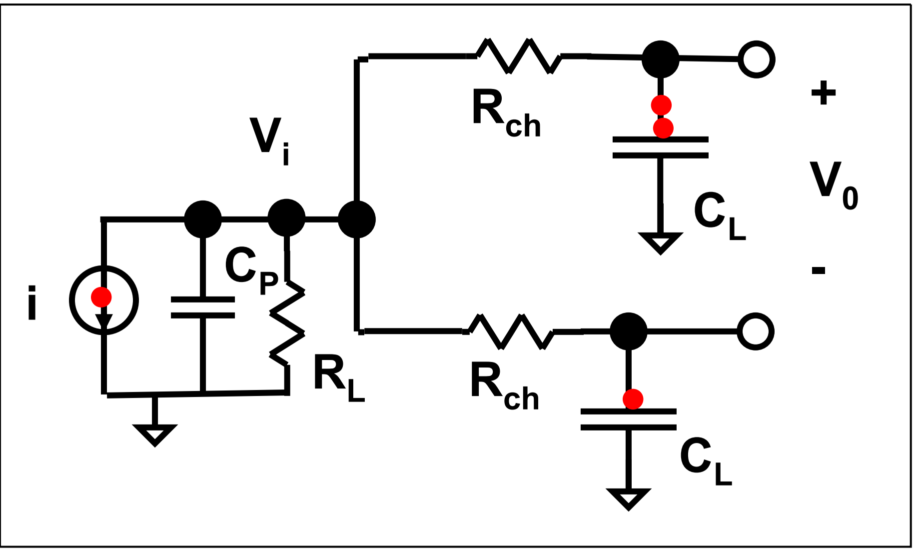
Rx Front End



- **Resistively biased inverter as LNA.**
  - Av = $2Gm_{LNA}/(\omega_{LO}C_{par})$ *(20dB)*
  - NF ~*9dB*
- **Passive mixer dissipates little power**
  - Vout: 1-pole LPF at $2F_{LO}C_p/C_L$
  - LPF shunts RF signals through switches.
  - P_{OBC} = -22dBm

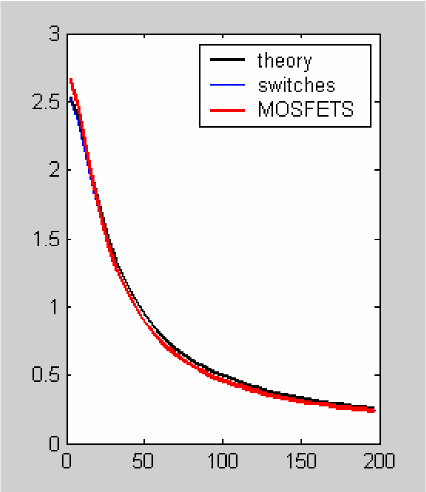
Cool mixer/filter effect

$$V_0(k+1) = V_0(k)\left(\frac{C_L - C_P}{C_L + C_P}\right)$$



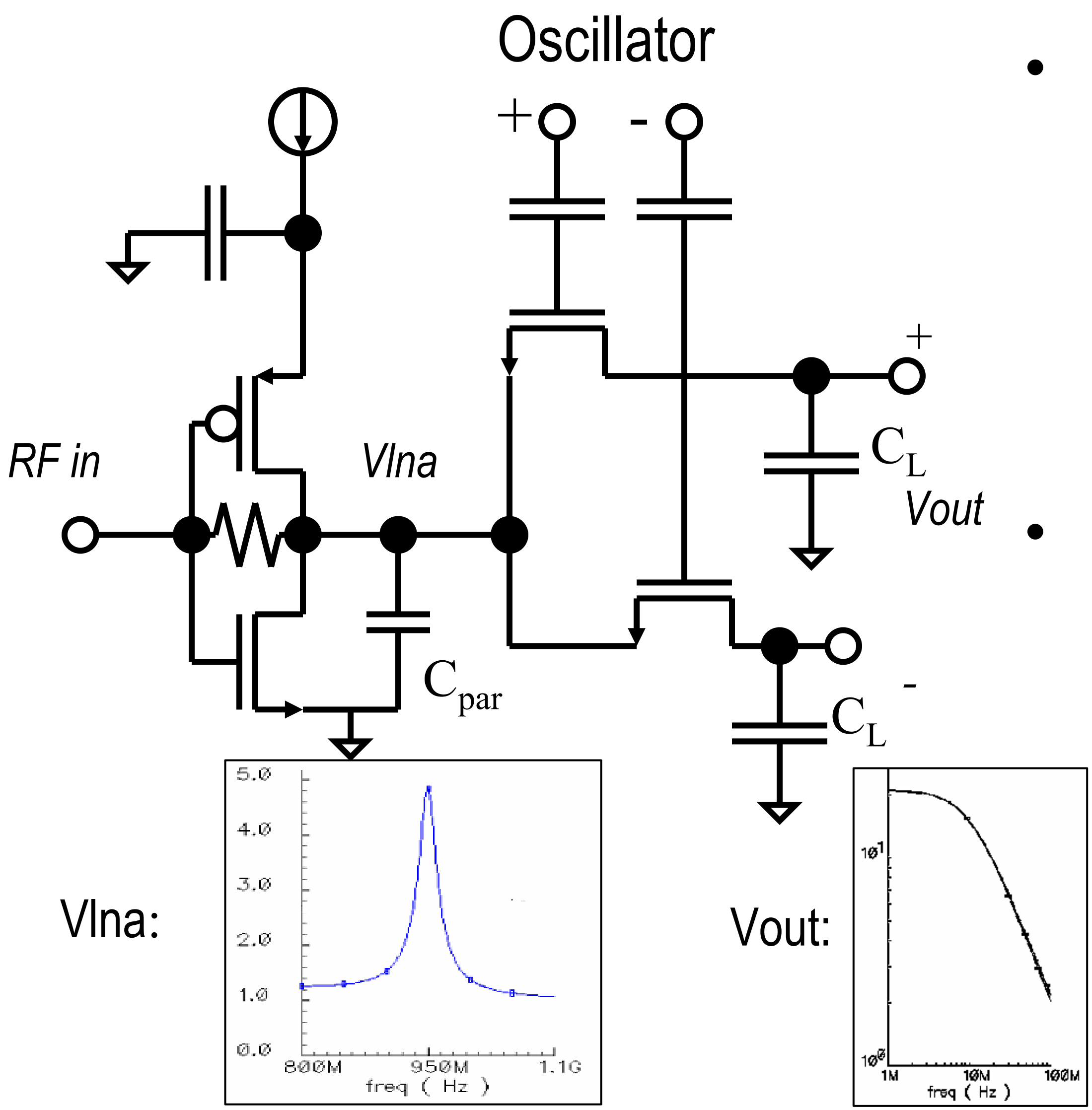
$$i = A\sin(\omega_{LO}t + \Delta\omega kT)$$

$$\frac{V_0}{A} = \frac{\dfrac{4A}{C_L\omega_{LO}}}{j\Delta\omega + \left(\dfrac{2C_P}{TC_L} - \dfrac{1}{2R_LC_L}\right)}$$



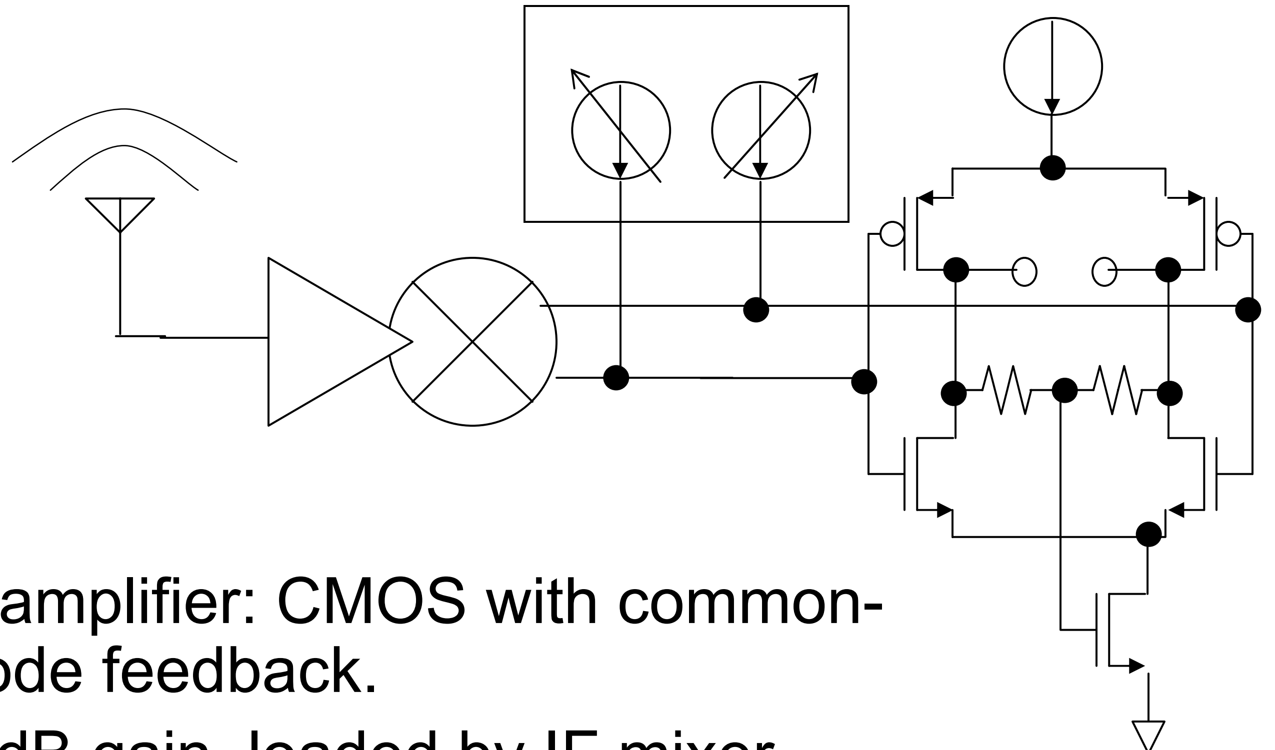
$$V_i \approx V_0\sin(\omega_{LO}t)$$

Rx Front End



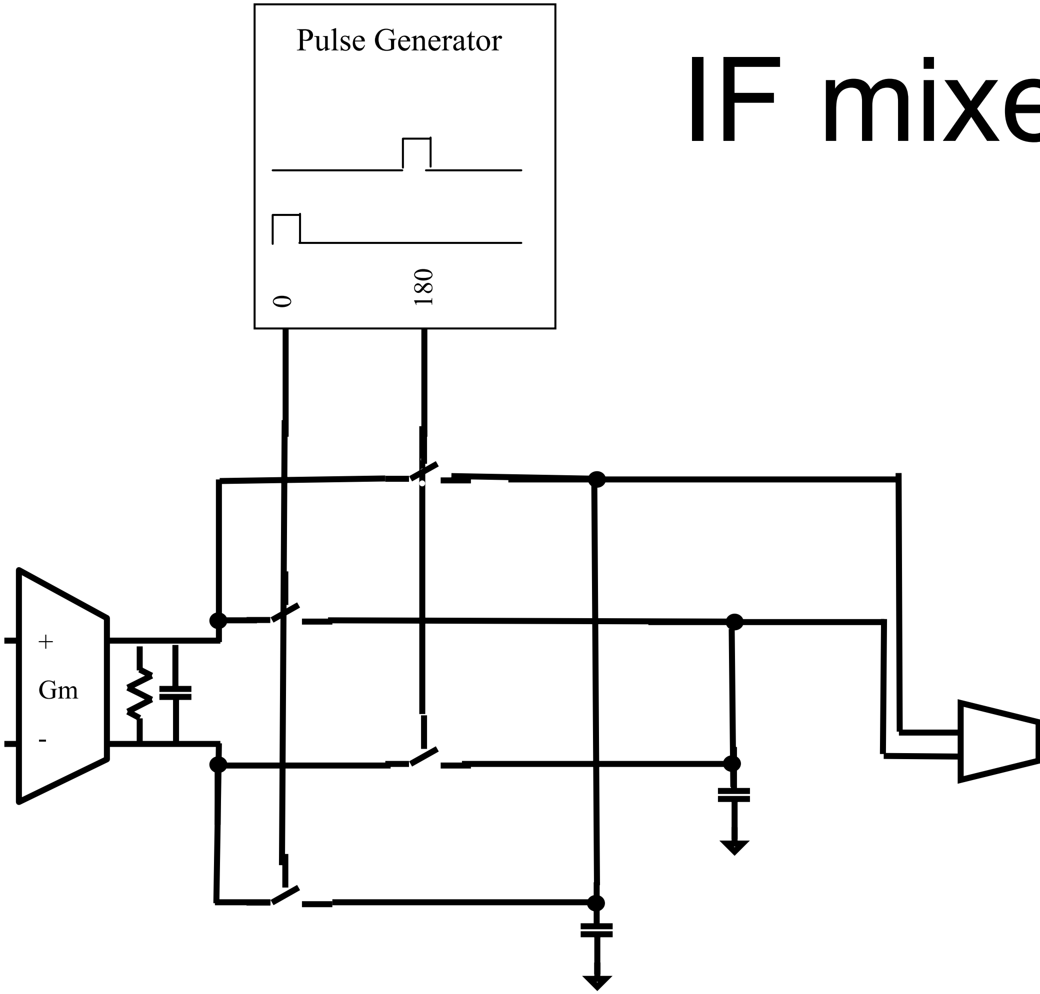
- **Resistively biased inverter as LNA.**
  - $Av = 2Gm_{LNA} /(\omega_{LO}C_{par})$ *(20dB)*
  - NF ~*9dB*
- **Passive mixer dissipates little power**
  - Vout: 1-pole LPF at $2F_{LO}C_p/C_L$
  - LPF shunts RF signals through switches.
  - P_{OBC} = -22dBm

IF Amplifier



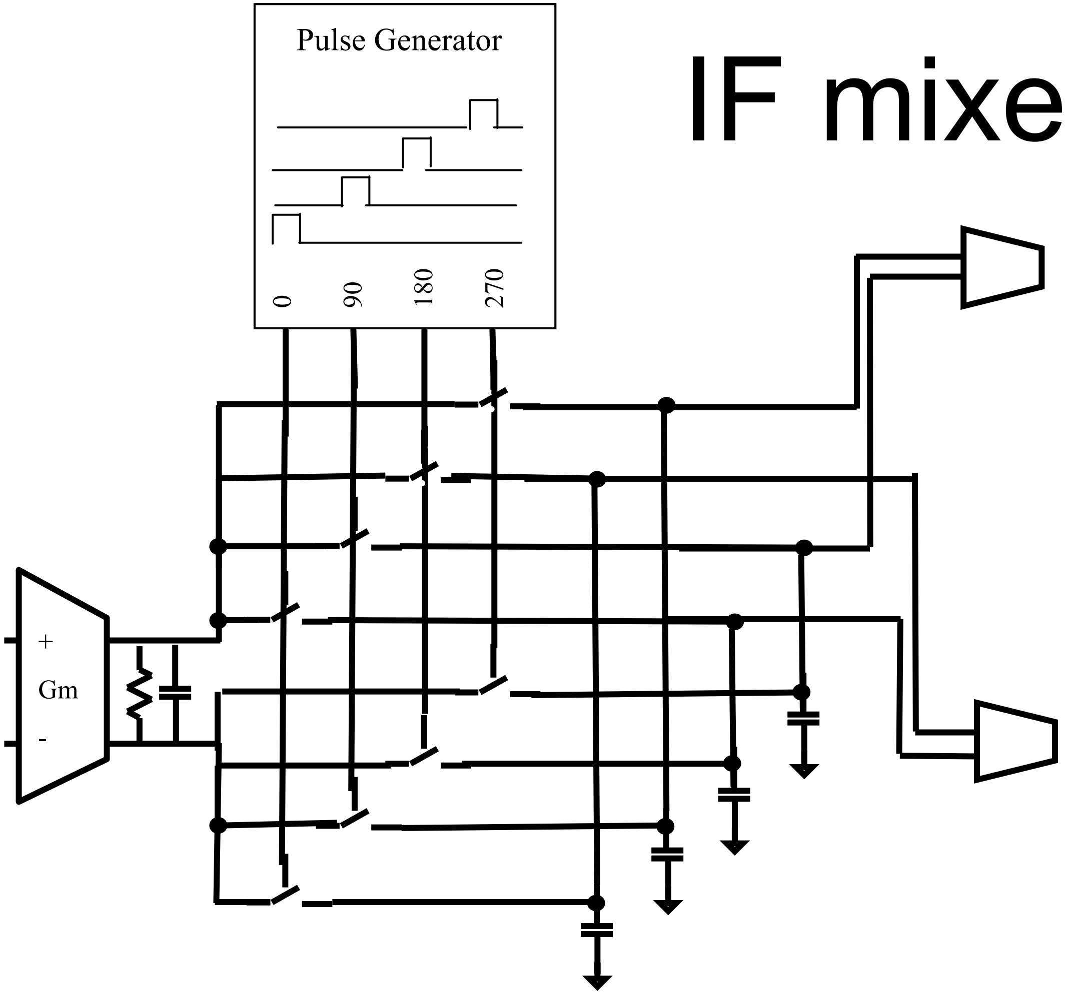
- IF amplifier: CMOS with common-mode feedback.
- 26dB gain, loaded by IF mixer.
- 5-bit, differential current DAC cancels LO self-mixing.

IF mixer



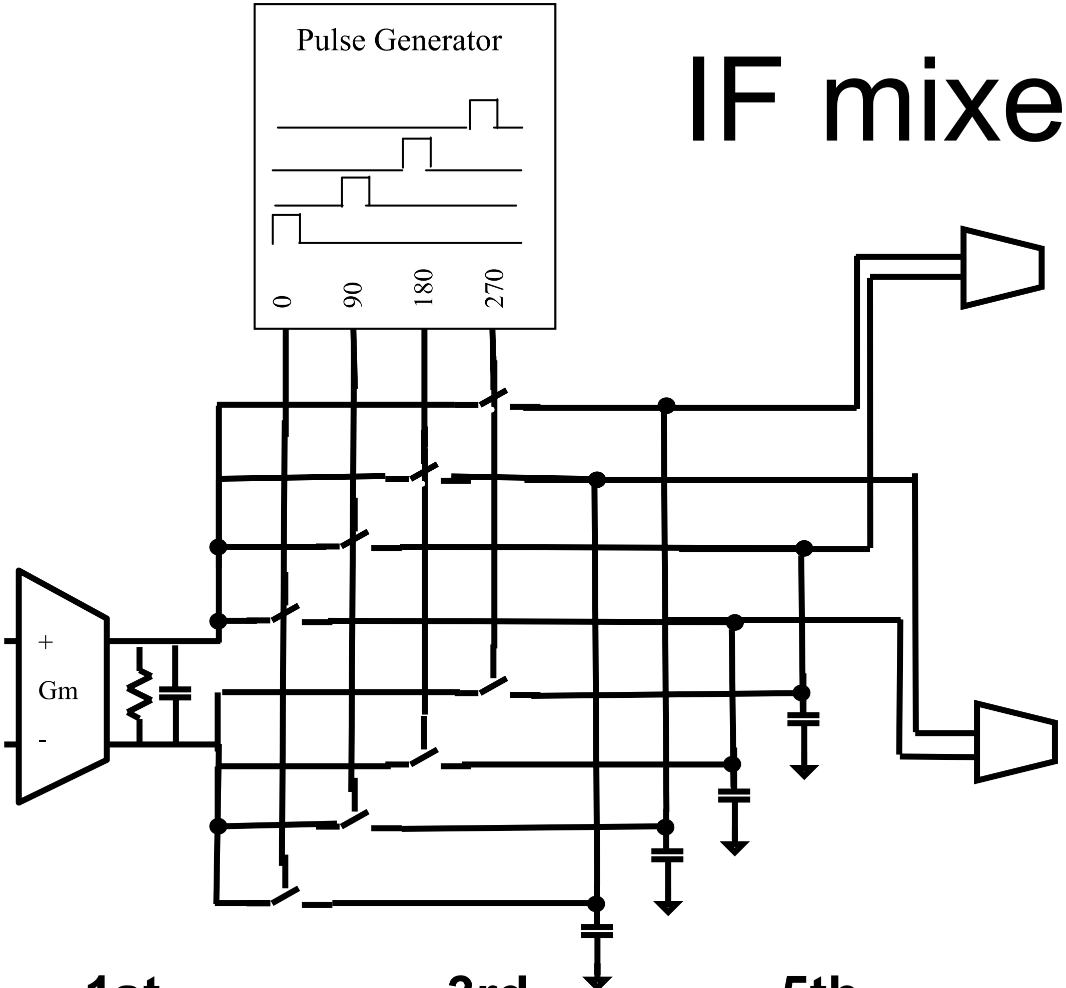
- **Switches sample to capacitors**
  - Get S-C pole
  - Shunts DC at amplifier by 20dB.

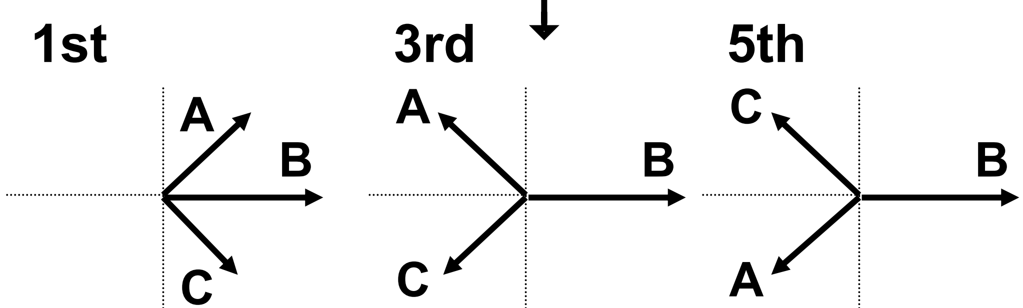
IF mixer



- **Switches sample to capacitors**
  - Get S-C pole
  - Shunts DC at amplifier by 20dB.
- **IF from divided LO:**
  - I/Q phase split

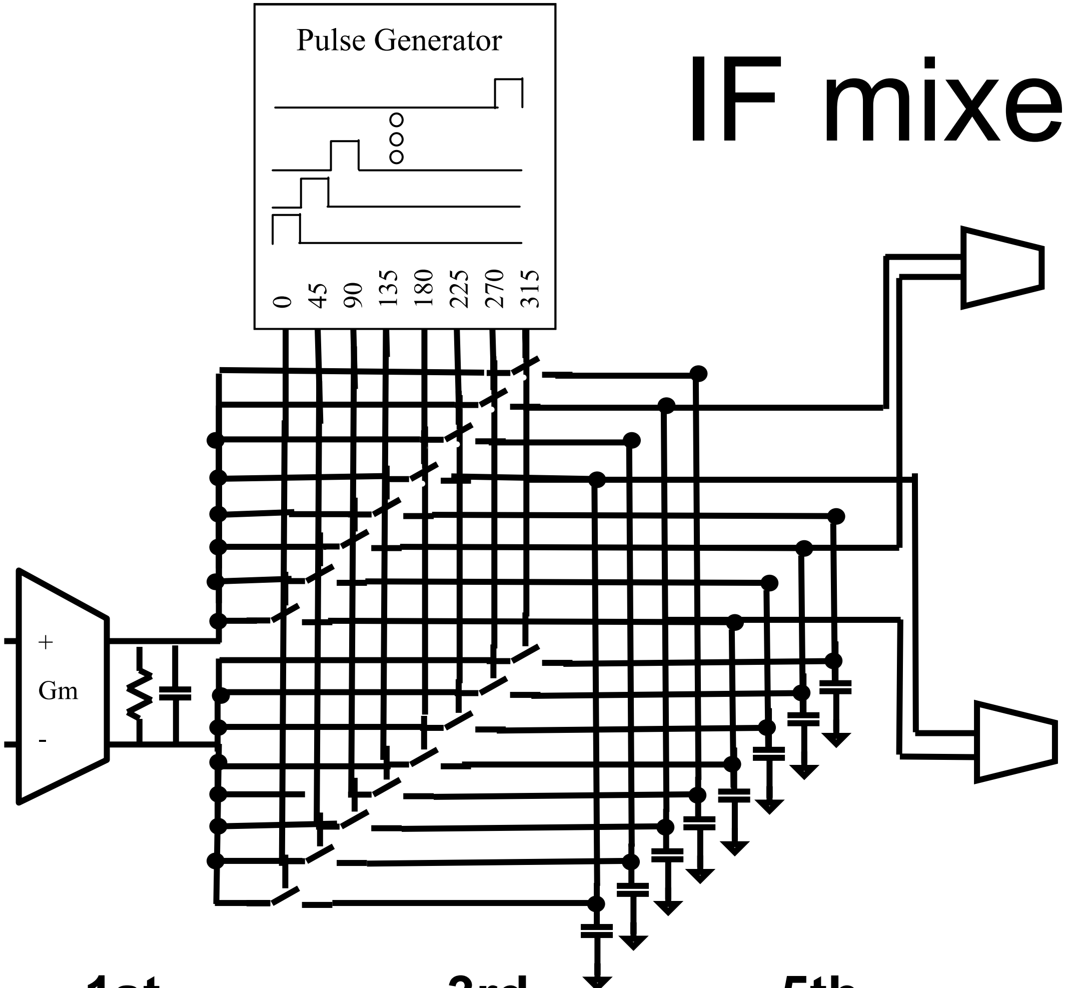
IF mixer

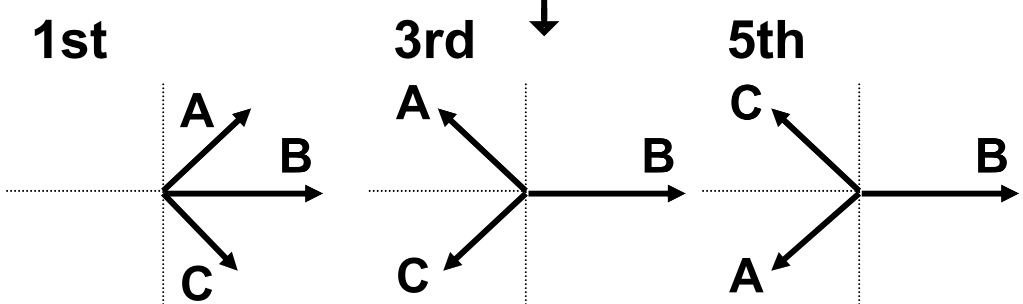




- **Switches sample to capacitors**
  - Get S-C pole
  - Shunts DC at amplifier by 20dB.
- **IF from divided LO:**
  - I/Q phase split
- **Use harmonic suppression:**
  - Cancel 3rd, 5th harmonics by recombining 45° split signals

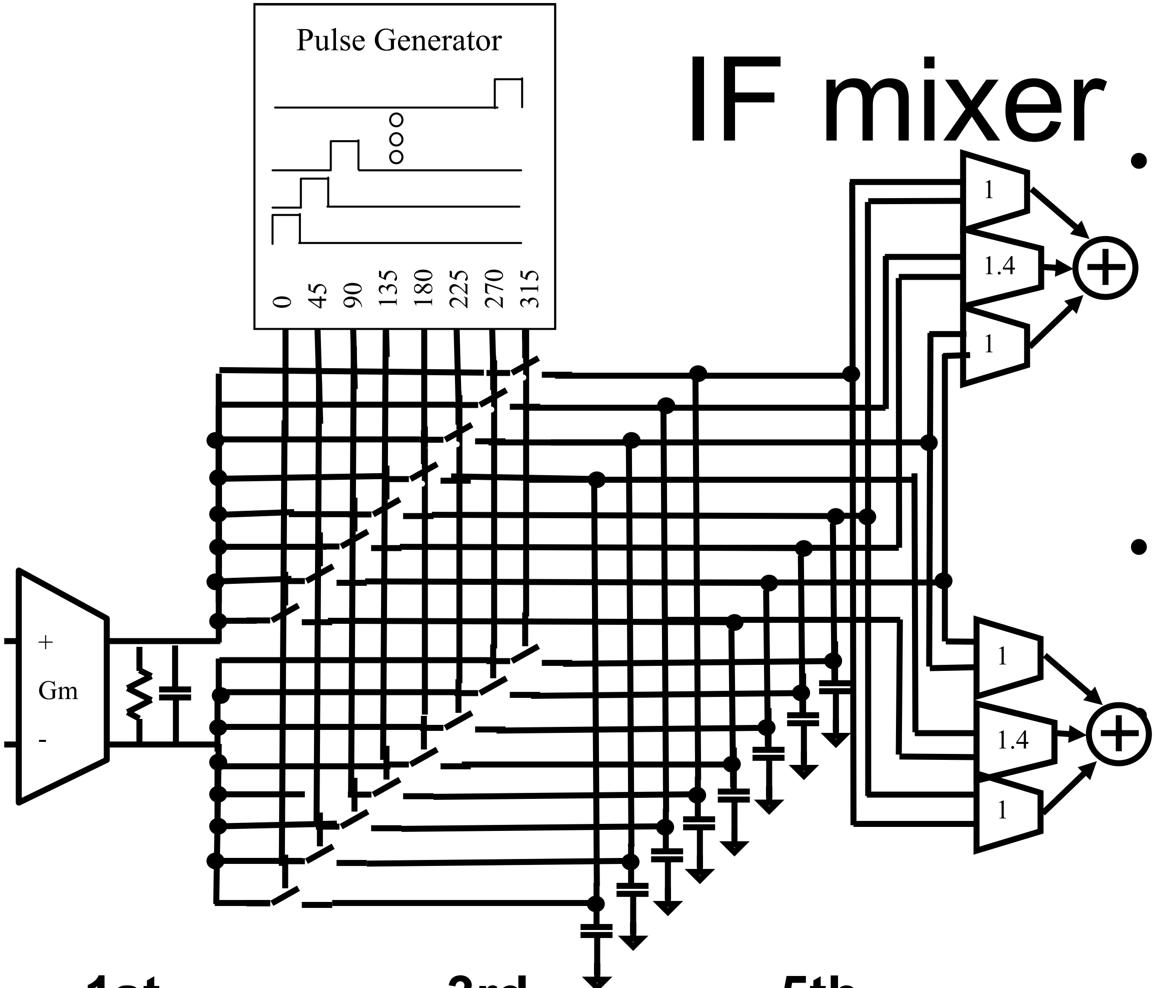
IF mixer



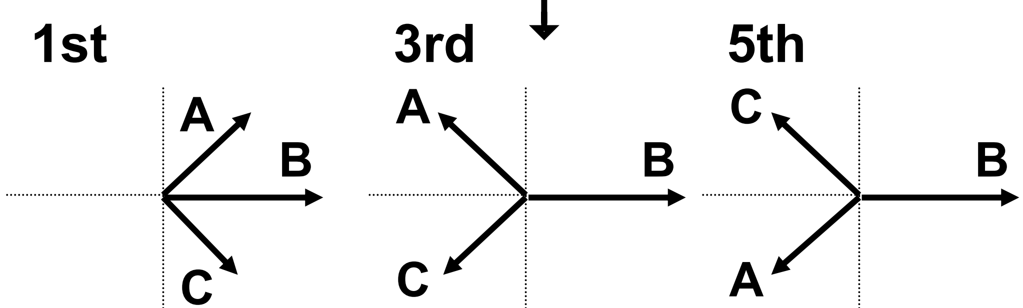


- **Switches sample to capacitors**
  - Get S-C pole
  - Shunts DC at amplifier by 20dB.
- **IF from divided LO:**
  - I/Q phase split
- **Use harmonic suppression:**
  - Cancel 3rd, 5th harmonics by recombining 45° split signals
  - 8 samples

IF mixer

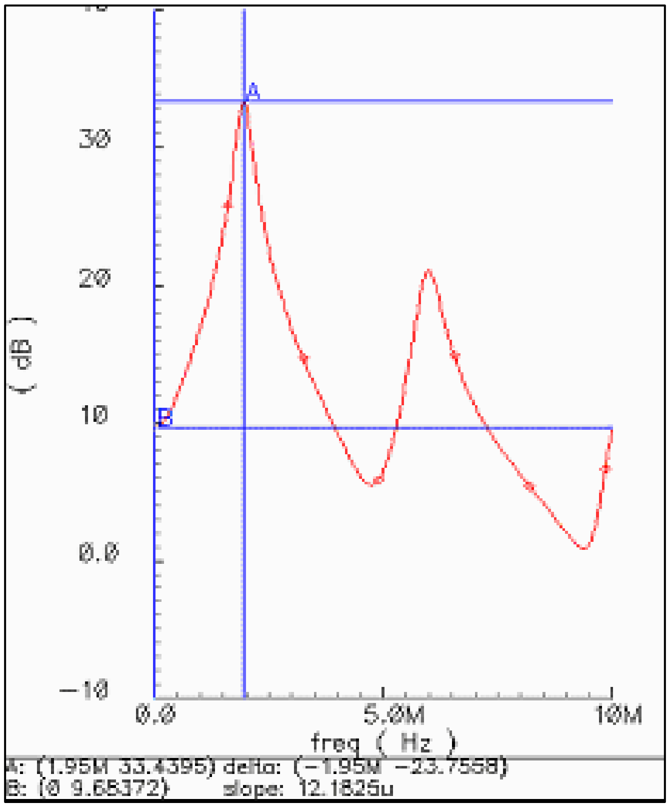


- **Switches sample to capacitors**
  - Get S-C pole
  - Shunts DC at amplifier by 20dB.
- **IF from divided LO:**
  - I/Q phase split
- **Use harmonic suppression:**
  - Cancel 3rd, 5th harmonics by recombining 45° split signals
  - 8 samples
  - Weight, sum samples



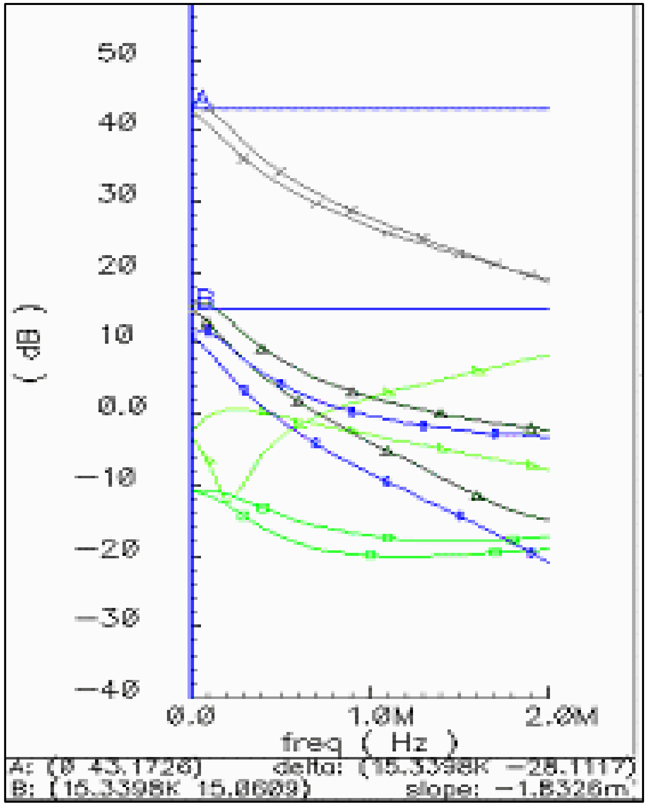
IF mixer simulations

IF (input) of mixer



DC is rejected by 23dB

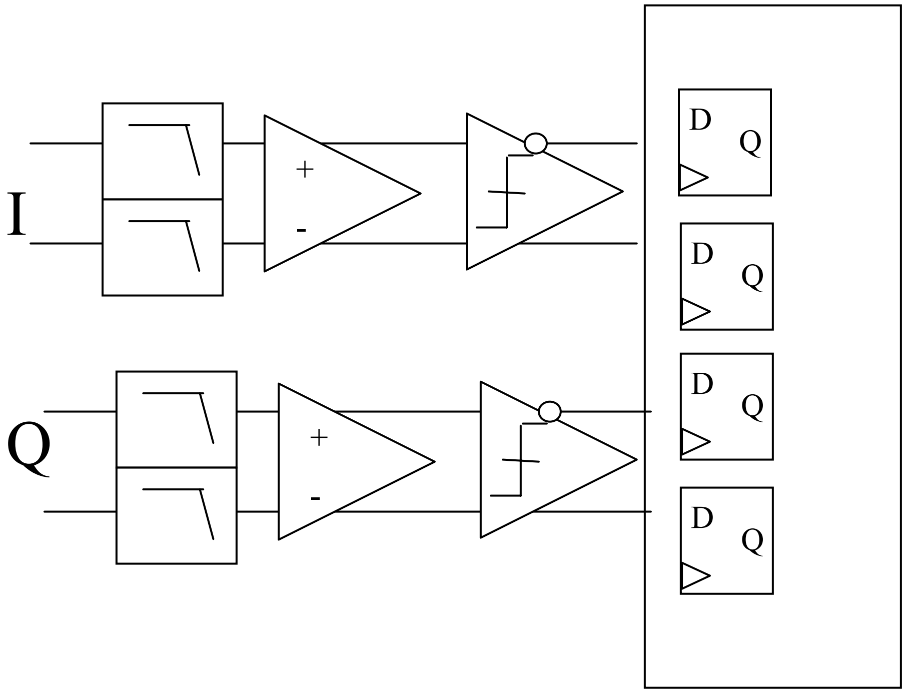
Baseband (output)



3rd harmonic mixing is suppressed by 20dB

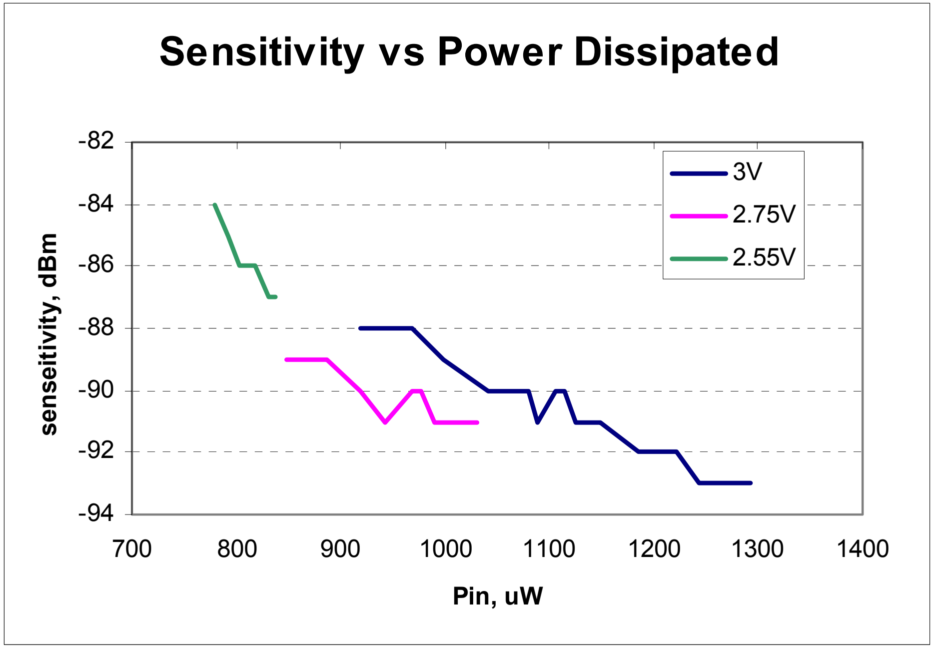
Baseband

Wanted to demonstrate full bits-to-bits communication, so need an FSK demodulator.



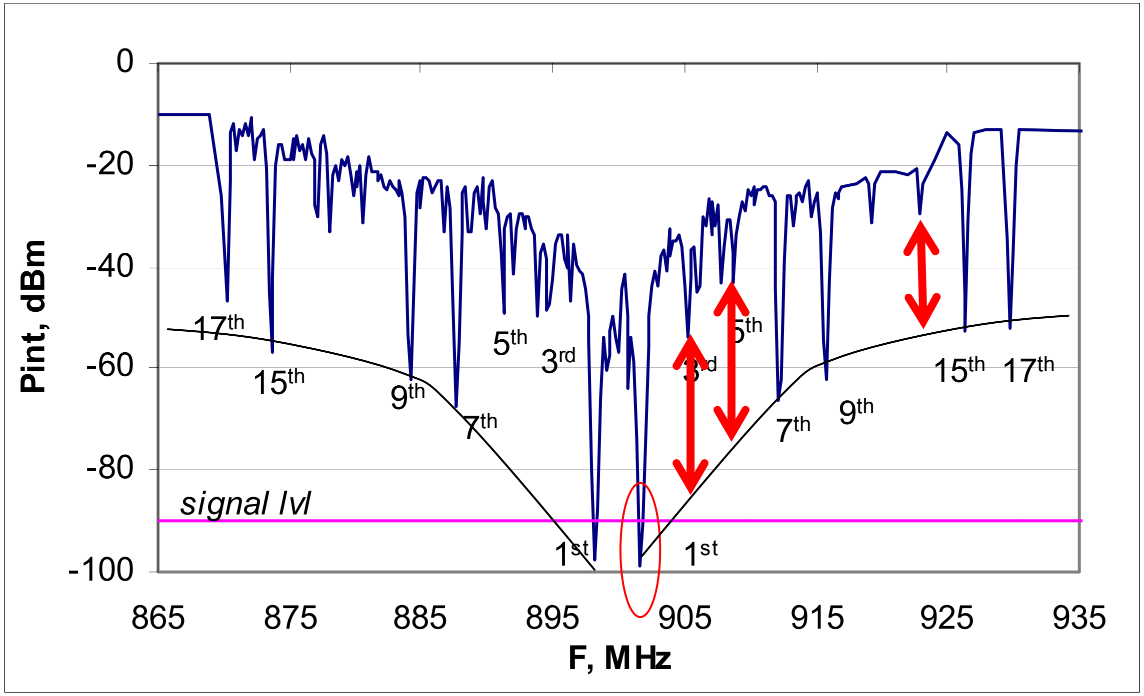
- Additional gain and filtering is needed
- Simple Sallen-key filters provide 2 poles.
- Switched-cap amplifiers reject DC, add 12dBgain
- Flip-flop based demodulator clocks in ones/zeros

Receiver Results: sensitivity



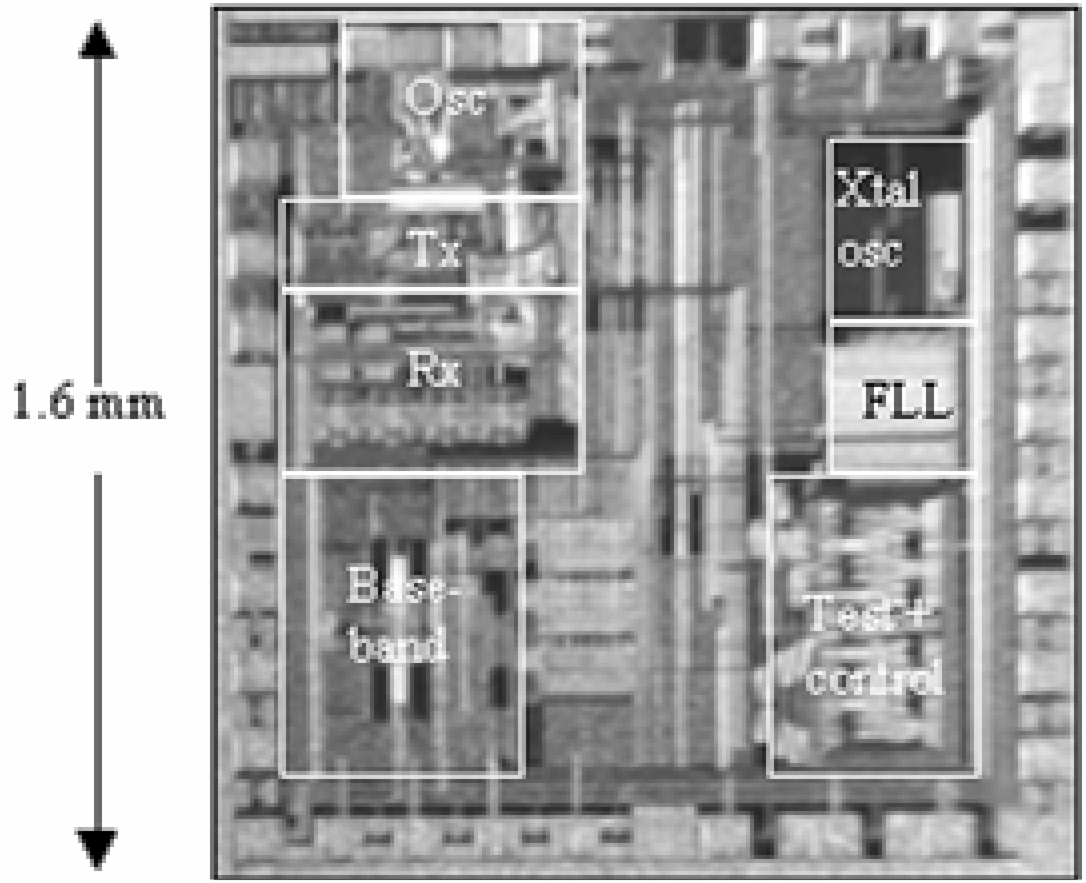
- NF ~12dB
- Sensitivity ~ -93dBm
  - From 50Ω+14nH
  - BER ~10^{-3}, no error correction
- BW = 300kHz
- IF = 1.8MHz

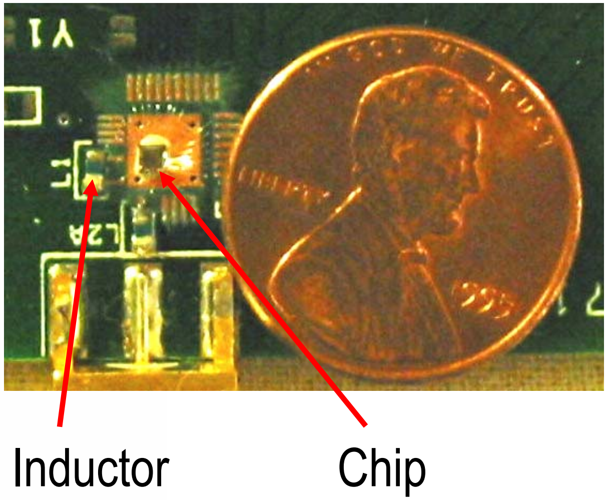
Receiver Results: Interference



- Wide band 4dB desense: -12dBm
- Close-in desense a mix of compression, phase noise
- 3rd, 5th harmonic interference reduced by 40dB.

Top Level


1.6 mm
Osc
Tx
Rx
Base-
band
Xtal
osc
FLL
Test+
control


Inductor
Chip

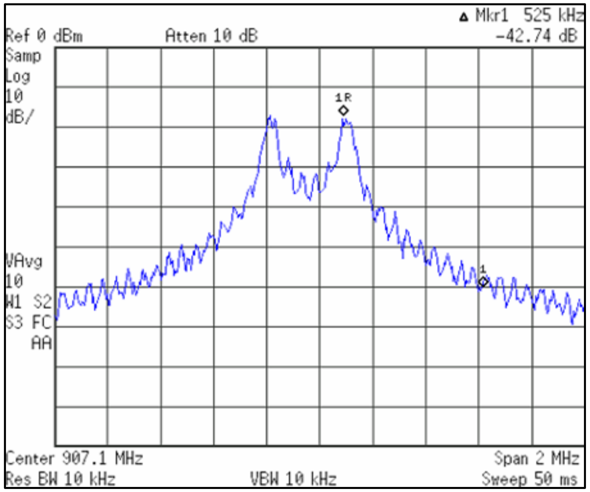
Power summary

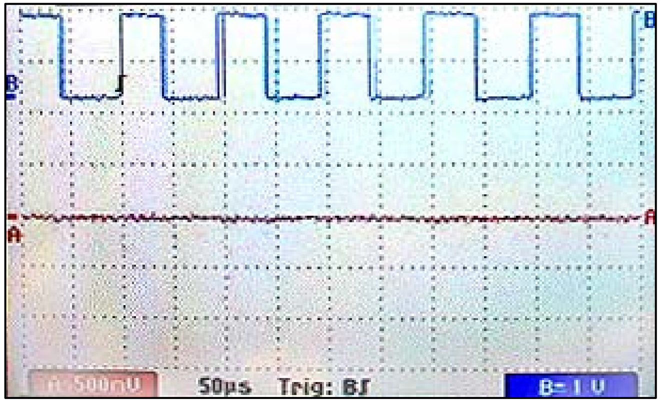
	tx, nom	tx, low	rx nom	rx low
osc	480	319	336	161
Tx	630	464	0	0
bias	60	54	90	81
divider	90	80	90	80
counter	23	23	23	23
lna	0	0	378	134
IF	0	0	90	52
bb	0	0	54	48
demod	0	0	75	75
total	**1283**	**940**	**1136**	**654**
Pout	250	100		
sense, dBm			-93	-84

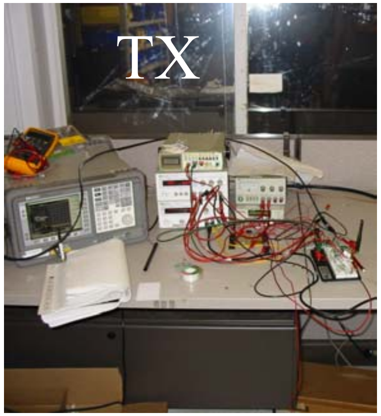
All powers in μW

Link Testing

- **Two chips communicating through the air:**
  - 20 kbps
  - 16 meters through 2 concrete walls
  - Nominal power (1.2mW RX, 1.3mW TX)
  - 100 kbps at shorter range
  - Battery, antenna, crystal oscillator inductor, tuning inductor







Conclusions

- Ultra-low power, very low cost radios demonstrated:
  - < 1.3 mW for both Receive and transmit
  - Only 4 off-chip components needed (< $1)
  - Purely digital interface.
  - Showed communication of 20kbps @ 16meters indoors.