Search <u>Login</u> Home (/S/) Q&A Communities (/S/group/CollaborationGroup/00Bb0000003cRLJEA2) Share Your Activities (/S/group/0F90X000000AXrvSAG) About This Community (/S/group/0F90X ashwinidigajerla (/s/profile/0050X0000007vjgKQAQ) (Community Member) to ST Community (/s/profile/0050X000007vh8GQAQ) (ST Employee): asked a question Edited by STM Community July 31, 2018 at 4:41 PM (/s/question/0050X00009XhGQSAZ/how-to-read-and-write-formto-sdram-memory-in-stm32f429-controller) How to read and write form/to SDRAM MEMORY in STM32f429 controller Posted on April 25, 2014 at 08:27 stm32f429-DISCO board have 8MB of on chip SDRAM module.I want to interface SDRAM chip to microcontroller.I finished the initilization part.Now I wish to write and read data 8MB SDRAM memory was organized as 4 internal banks 1MB each. How i write/read to total 8MB with Single write/read command to SDRAM instead of individual internal bank Access #whiskey-tango-foxtrot STM32 MCUs (/S/topic/0TO0X000000BSqSWAW/) 25 answers 1.52K views glory_man (/s/profile/0050X000007vqnqQAA) (Community Member) Edited by ST Community July 21, 2018 at 5:34 PM Posted on April 25, 2014 at 09:04 http://www.st.com/web/catalog/tools/FM116/SC959/SS1532/LN1848/PF259090 (http://www.st.com/web/catalog/tools/FM116/SC959/SS1532/LN1848/PF259090) you can find documents and software examples for your board. For example, http://www.st.com/web/en/catalog/tools/PF259429 (http://www.st.com/web/en/catalog/tools/PF259429) contains an example of SDRAM manipulation $stsw-stm32138.zip\ \ STM32F429I-Discovery_FW_V1.0.1\ \ Projects\ \ Peripheral_Examples\ \ FMC_SDRAM.\ This\ examples\ uses\ FMC_controller\ to\ interface\ with\ the\ SDRAM\ memory.$ After SDRAM initialization you can read/write/erase data in to any memory cell. clive1 (NFA Crew) (/s/profile/0050X000007vuogQAA) (Community Member) Edited by ST Community July 21, 2018 at 5:35 PM Posted on April 25, 2014 at 18:43 It accesses just like ANY other memory space within the microprocessors purview. For the STM32F429I-DISCO, the SDRAM is situated at 0xD0000000 unsigned char *sdram = (unsigned char *)0xD00000000; ashwinidigajerla (/s/profile/0050X000007vlgKQAQ) (Community Member) Edited by ST Community July 21, 2018 at 5:35 PM Posted on April 26, 2014 at 07:05 Thank you.I got clarity reading and wriring from base address. By reading the sdram data sheet I understood that total memory is bank oriented with 4 internal banks in rows and column format, to access any memory location we need to send internal bank address,row and colum address with GPIO pins in alternate fun mode. My doubt is to access any location every time do i need to send all above address or is there any AUTO INCREMENT OF BASE ADDRESS WHILE READ/WRITE, YOUR ANSWER WILL MORE HELP ME

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clive1 (NFA Crew) (/s/profile/0050X000007vuogQAA) (Community Member)

Edited by STM Community October 12, 2018 at 12:55 PM

Posted on April 26, 2014 at 14:40 The SDRAM Geometry is configured in the initialization code, it appears to the programmer as a linear 8MB region.

```
// STM32F429 SDRAM - sourcer32@gmail.com
      stdio.h
      stdlib.h
       #include
       string.h
11 #include ''stm32f429i_discovery.h''
12 #include ''stm32f429i_discovery_sdram.h''
13 #define BANK2 // DISCO
      // STM32F429I-DISCO Bank2
// STM32F4x9I-EVAL Bank1
// Bank1 Bank2
14
15
 16
      // 0xC0000000 0xD0000000 256MB
// 0xCFFFFFF 0xDFFFFFFF
 17
      // 0x00000000 0x04000000 64MB
// 0x03FFFFFF 0x07FFFFFF
#define IS42S16400J_SIZE 0x400000
 19
22
23
      #ifdef BANK1
       #define SDRAM_ADDR 0xC0000000
      #define SDRAM_ADDR_SWP 0x80000000
#define SDRAM_BANK FMC_Bank1_SDRAM
#endif // BANK1
 24
 27
      #ifdef BANK2
28
29
       #define SDRAM_ADDR 0xD0000000
#define SDRAM_ADDR_SWP 0x9000000
      32
33
34
      /**
* @brief Main program
35
36
       * @param None
* @retval None
37
38
39
40
41
42
       int main(void)
       int i:
       unsigned long *sdram = (unsigned long *)SDRAM_ADDR;
      /*!<
At
43
44
       this stage the microcontroller clock setting is already configured,
       this is done through SystemInit() function which is called from startup files (startup_stm32f429_439xx.s) before to branch to application main. To reconfigure the default setting of SystemInit() function, refer to
 45
48
49
50
      system_stm32f4xx.c file
*/
/* Add your application code here */
      /* Add your application code nere */

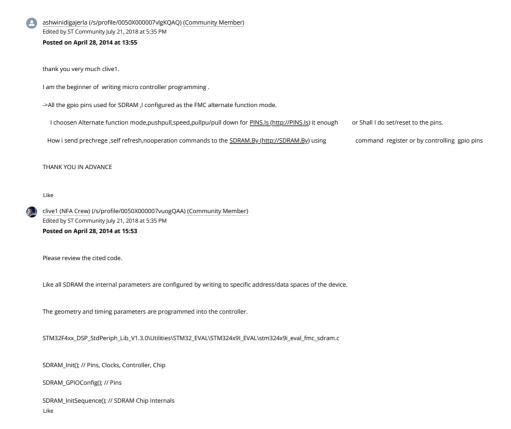
* SDRAM_Init();

// * FMC SDRAM GPIOS Configuration */

// SDRAM_GPIOConfig(); // SDRAM_Init() should do this

/* Disable write protection */
 51
52
 53
54
55
       FMC_SDRAMWriteProtectionConfig(SDRAM_BANK, DISABLE);
for(
56
57
58
59
60
61
62
       ; i<10; i++) // Front, Random
      printf(''%08X '', sdram[i]);
 63
      if ((i % 5) == 4)
putchar('
');
66
67
68
       putchar(
69
70
71
       ');
for(
72
73
 74
      ; i<0x200000; i++) // 8MB in 32-bit words
75
76
77
       sdram[i] = i;
for(
 79
80
81
       ; i<10; i++) // Front
       printf(''%08X '', sdram[i]);
 82
      if ((i % 5) == 4)
putchar('
');
 84
85
86
87
88
89
      putchar('
');
for(
92
93
94
        ; i<10; i++) // Back
      printf(''%08X '', sdram[i+0x1FFFF6]);
if ((i % 5) == 4)
95
96
97
98
99
      putchar('
');
100 putchar('
```

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```
ashwinidigajerla (/s/profile/0050X000007vlgKQAQ) (Community Member)
Edited by STM Community July 21, 2018 at 5:42 PM
                             Posted on May 05, 2014 at 14:24
                           hai clave here i am attached my sdram code.will u please check it and give any information if possible
                           reading and writing from base address 0xd0000000. Then what is the use of address and data pins.
                           do i need to send row address,column address,bank address using pins?
                           please clarify me.
                             void FMC_SDRAM_Init(UINT8 U8_Bank)
                           UINT32 temp1=0,temp2=0,temp3=0;
                           UINT8 u8_i = 0;
                           ST_pFMC_REGS_Ptr_t->FMC_SDCR1 = FMCSDRAM_CR1_CR2_REG_RESET;
                           ST pFMC REGS Ptr t->FMC SDCR2 = FMCSDRAM CR1 CR2 REG RESET;
                           ST_pFMC_REGS_Ptr_t->FMC_SDTR1 = FMCSDRAM_TR1_TR2_REG_RESET;
                                     ST_pFMC_REGS_Ptr_t->FMC_SDTR2 = FMCSDRAM_TR1_TR2_REG_RESET;
                                                                            Gpioclk Init(GPIO PORTA):
                                   Gpioclk_Init(GPIO_PORTB);
                                   Gpioclk_Init(GPIO_PORTC);
                                   Gpioclk_Init(GPIO_PORTD);
                                   Gpioclk Init(GPIO PORTE):
                                   Gpioclk_Init(GPIO_PORTF);
                                   Gpioclk_Init(GPIO_PORTG);
                                   Gpioclk_Init(GPIO_PORTH);
                                   Gpioclk Init(GPIO PORTI);
                                   RCC_AHBPeripheralEnable(AHB_FSMC);
                           while(En_SDRAM_ConfigPort_List_t[u8_i] != 0)
                         Sdram_Gpio_Pin_Config(En_SDRAM_ConfigPort_List_t(u8_i],SDRAM_ConfigPin_List(u8_i),GPIO_MODER_ALTFUN_MASK,GPIO_OTYPE_PP,GPIO_OSPEEDR_MEDIUM_MASK,GPIO_PUPD_NOPULL,ALTFUN_FMC);
                           u8_i++;
                                                        temp1 = (UINT32)(FMC\_SDCR1\_ROW\_ADDRWIDTH\_12|FMC\_SDCR1\_COLUM\_ADDRWIDTH\_8|FMC\_SDCR1\_MWIDTH\_16|FMC\_SDCR1\_INTRNLBANKS\_4|EMP1 = (UINT32)(FMC\_SDCR1\_ROW\_ADDRWIDTH\_12|FMC\_SDCR1\_COLUM\_ADDRWIDTH\_8|FMC\_SDCR1\_MWIDTH\_16|FMC\_SDCR1\_INTRNLBANKS\_4|EMP1 = (UINT32)(FMC\_SDCR1\_ROW\_ADDRWIDTH\_12|FMC\_SDCR1\_MWIDTH\_16|FMC\_SDCR1\_INTRNLBANKS\_4|EMP1 = (UINT32)(FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_INTRNLBANKS\_4|EMP1 = (UINT32)(FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_INTRNLBANKS\_4|EMP1 = (UINT32)(FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_INTRNLBANKS\_4|EMP1 = (UINT32)(FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_16|FMC\_SDCR1\_ROW\_ADDRWIDTH\_
                                                FMC\_SDCR1\_3CAS\_LATENCY\\ | FMC\_SDCR1\_WP\_EN\\ | FMC\_SDCR1\_RPIPE\_1HCLK\\ | FMC\_SDCR1\_RBURST\_ENABLE\\ | FMC\_SDCR1\_2HCLKPERIOD\\ | FMC\_SDCR1\_RBURST\_ENABLE\\ | FMC\_SDCR1\_2HCLKPERIOD\\ | FMC\_SDCR1\_RBURST\_ENABLE\\ | FMC\_SDC
                                             temp2 = (UINT32)(FMC\_SDTR1\_TRCD\_2|FMC\_SDTR1\_TRP\_2|FMC\_SDTR1\_TWR\_2|FMC\_SDTR1\_TRC\_6|FMC\_SDTR1\_TRAS\_4|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TRAS\_4|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR\_7|FMC\_SDTR1\_TXSR_7|FMC\_SDTR1\_TXSR_7|FMC\_SDTR1\_TXSR_7|FMC\_SDTR1\_TXSR_7|FMC\_SDTR1\_TXSR_7|FMC\_SDTR1\_TXSR_7|FMC\_SDTR1\_TXSR_7|FMC\_SDTR1\_TXSR_7|FMC\_SDTR1\_TXSR_7|FMC\_SDT
                                                [FMC_SDTR1_TMRD_2);
                                                     if(U8_Bank ==SDRAM_BANK1)
                                             ST_pFMC_REGS_Ptr_t->FMC_SDCR1 = temp1;
                                                                  ST_pFMC_REGS_Ptr_t->FMC_SDTR1 = temp2;
```

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