PA

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0		TIMER1_C H0/TIMER 1_ETI	TIMER4_C H0	TIMER7_E TI				USART1_ CTS	UART3_T X			ENET_MII _CRS				EVENTOU T
PA1		TIMER1_C H1	TIMER4_C H1					USART1_ RTS	UART3_R X			ENET_MII _RX_CLK/ ENET_RMI I_REF_CL K				EVENTOU T
PA2		TIMER1_C H2	TIMER4_C H2	TIMER8_C H0		I2S_CKIN		USART1_ TX				ENET_MDI O				EVENTOU T
PA3		TIMER1_C H3	TIMER4_C H3	TIMER8_C H1		I2S1_MCK		USART1_ RX			USBHS_U LPI D0	ENET_MII COL				EVENTOU T
PA4						SPI0_NSS	SPI2_NSS/ I2S2 WS	USART1_ CK			_	_	USBHS_S OF	DCI_HSYN C		EVENTOU T
PA5		TIMER1_C H0/TIMER 1_ETI		TIMER7_C H0_ON		SPI0_SCK					USBHS_U LPI_CK					EVENTOU T
PA6		TIMER0_B RKIN	TIMER2_C H0	TIMER7_B RKIN		SPI0_MIS O	I2S1_MCK			TIMER12_ CH0			SDIO_CM D	DCI_PIXC LK		EVENTOU T
PA7		TIMER0_C H0_ON	TIMER2_C H1	TIMER7_C H0_ON		SPI0_MOS				TIMER13_ CH0		ENET_MII _RX_DV/E NET_RMII CRS_DV	EXMC_SD NWE			EVENTOU T
PA8	ск_оито	TIMER0_C H0			I2C2_SCL			USART0_ CK		CTC_SYN	USBFS_S OF		SDIO_D1			EVENTOU T
PA9		TIMER0_C H1			I2C2_SMB A	SPI1_SCK/ I2S1_CK		USART0_ TX					SDIO_D2	DCI_D0		EVENTOU T
PA10		TIMER0_C H2			I2C2_TXF RAME			USART0_ RX			USBFS_ID			DCI_D1		EVENTOU T
PA11		TIMER0_C H3						USART0_ CTS	USART5_ TX	CAN0_RX	USBFS_D M					EVENTOU T
PA12		TIMER0_E TI						USART0_ RTS	USART5_ RX	CAN0_TX	USBFS_D P					EVENTOU T
						•					•					
PA13	JTMS/SW DIO															EVENTOU T
PA14	JTCK/SW CLK															EVENTOU T
PA15	JTDI	TIMER1_C H0/TIMER 1_ETI				SPI0_NSS	SPI2_NSS/ I2S2_WS	USART0_ TX								EVENTOU T

\mathbf{PB}

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0		TIMER0_C H1_ON	TIMER2_C H2	TIMER7_C H1_ON				SPI2_MOS I/I2S2_SD			USBHS_U LPI_D1	ENET_MII _RXD2	SDIO_D1			EVENTOU T
PB1		TIMER0_C H2_ON	TIMER2_C H3	TIMER7_C H2_ON							USBHS_U LPI_D2	ENET_MII _RXD3	SDIO_D2			EVENTOU T
PB2		TIMER1_C H3						SPI2_MOS I/I2S2_SD			USBHS_U LPI_D4		SDIO_CK			EVENTOU T
PB3	JTDO/TRA CESWO	TIMER1_C H1				SPI0_SCK	SPI2_SCK/ I2S2_CK	USART0_ RX		I2C1_SDA						EVENTOU T
PB4	NJTRST		TIMER2_C H0		I2C0_TXF RAME	SPI0_MIS O	SPI2_MIS O	I2S2_ADD _SD		I2C2_SDA			SDIO_D0			EVENTOU T
PB5			TIMER2_C H1		I2C0_SMB A	SPI0_MOS	SPI2_MOS I/I2S2_SD			CAN1_RX	USBHS_U LPI_D7	ENET_PP S_OUT	EXMC_SD CKE1	DCI_D10		EVENTOU T
PB6			TIMER3_C H0		I2C0_SCL			USARTO_ TX		CAN1_TX			EXMC_SD NE1	DCI_D5		EVENTOU T
PB7			TIMER3_C H1		I2C0_SDA			USARTO_ RX					EXMC_NL/ EXMC_NA DV			EVENTOU T
PB8		TIMER1_C H0/TIMER 1_ETI	TIMER3_C H2	TIMER9_C H0	I2C0_SCL					CAN0_RX		ENET_MII _TXD3	SDIO_D4	DCI_D6		EVENTOU T
PB9		TIMER1_C H1	TIMER3_C H3	TIMER10_ CH0	I2C0_SDA	SPI1_NSS/ I2S1 WS				CAN0_TX			SDIO_D5	DCI_D7		EVENTOU T
PB10		TIMER1_C H2			I2C1_SCL	SPI1_SCK/ I2S1_CK	I2S2_MCK	USART2_ TX			USBHS_U LPI_D3	_RX_ER	SDIO_D7			EVENTOU T
PB11		TIMER1_C H3			I2C1_SDA	I2S_CKIN		USART2_ RX				ENET_MII _TX_EN/E NET_RMII _TX_EN				EVENTOU T

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB12		TIMER0_B RKIN			I2C1_SMB A	SPI1_NSS/ I2S1_WS		USART2_ CK		CAN1_RX	USBHS_U LPI_D5	ENET_MII _TXD0/EN ET_RMII_ TXD0	USBHS_ID			EVENTOU T
PB13		TIMER0_C H0_ON			I2C1_TXF RAME	SPI1_SCK/ I2S1_CK		USART2_ CTS		CAN1_TX	USBHS_U LPI_D6	ENET_MII _TXD1/EN ET_RMII_ TXD1				EVENTOU T
PB14		TIMER0_C H1_ON		TIMER7_C H1_ON		SPI1_MIS O	I2S1_ADD _SD	USART2_ RTS		TIMER11_ CH0			USBHS_D M			EVENTOU T
PB15	RTC_REFI N	TIMER0_C H2_ON		TIMER7_C H2_ON		SPI1_MOS I/I2S1_SD				TIMER11_ CH1			USBHS_D P			EVENTOU T

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0											USBHS_U LPI_STP		EXMC_SD NWE			EVENTOU T
PC1						SPI2_MOS I/I2S2_SD		SPI1_MOS I/I2S1_SD				ENET_MD C				EVENTOU T
PC2							I2S1_ADD _SD				USBHS_U LPI_DIR	ENET_MII _TXD2	EXMC_SD NE0			EVENTOU T
PC3						SPI1_MOS I/I2S1_SD					USBHS_U LPI_NXT	ENET_MII _TX_CLK	EXMC_SD CKE0			EVENTOU T
PC4												ENET_MII _RXD0/EN ET_RMII_ RXD0	EXMC_SD NE0			EVENTOU T
PC5								USART2_ RX				ENET_MII _RXD1/EN ET_RMII_ RXD1	EXMC_SD CKE0			EVENTOU T
PC6			TIMER2_C H0	TIMER7_C H0		12S1_MCK			USART5_ TX				SDIO_D6	DCI_D0		EVENTOU T
PC7			TIMER2_C H1	TIMER7_C H1		SPI1_SCK/ I2S1_CK	I2S2_MCK		USART5_ RX				SDIO_D7	DCI_D1		EVENTOU T
PC8	TRACED0		TIMER2_C H2	TIMER7_C H2					USART5_ CK				SDIO_D0	DCI_D2		EVENTOU T

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC9	CK_OUT1		TIMER2_C H3	TIMER7_C H3	I2C2_SDA	I2S_CKIN							SDIO_D1	DCI_D3		EVENTOU T
PC10							SPI2_SCK/ I2S2_CK	USART2_ TX	UART3_T X				SDIO_D2	DCI_D8		EVENTOU T
PC11						I2S2_ADD _SD	SPI2_MIS O	USART2_ RX	UART3_R X				SDIO_D3	DCI_D4		EVENTOU T
PC12					I2C1_SDA		SPI2_MOS I/I2S2_SD		UART4_T X				SDIO_CK	DCI_D9		EVENTOU T
PC13																EVENTOU T
PC14																EVENTOU T
PC15																EVENTOU T

\mathbf{PD}

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0							SPI2_MOS I/I2S2_SD			CAN0_RX			EXMC_D2			EVENTOU T
PD1								SPI1_NSS/ I2S1_WS		CAN0_TX			EXMC_D3			EVENTOU T
PD2			TIMER2_E TI						UART4_R X				SDIO_CM D	DCI_D11		EVENTOU T
PD3	TRACED1					SPI1_SCK/ I2S1_CK		USART1_ CTS					EXMC_CL K	DCI_D5		EVENTOU T
PD4								USART1_ RTS					EXMC_NO E			EVENTOU T
PD5								USART1_ TX					EXMC_N WE			EVENTOU T
PD6						SPI2_MOS I/I2S2_SD		USART1_ RX					EXMC_N WAIT	DCI_D10		EVENTOU T
PD7								USART1_ CK					EXMC_NE 0/EXMC_N CE1			EVENTOU T

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD8								USART2_ TX					EXMC_D1 3			EVENTOU T
PD9								USART2_ RX					EXMC_D1 4			EVENTOU T
PD10								USART2_ CK					EXMC_D1 5			EVENTOU T
PD11								USART2_ CTS					EXMC_A1 6/EXMC_C LE			EVENTOU T
PD12			TIMER3_C H0					USART2_ RTS					EXMC_A1 7/EXMC_A LE			EVENTOU T
PD13			TIMER3_C H1										EXMC_A1 8			EVENTOU T
PD14			TIMER3_C H2										EXMC_D0			EVENTOU T
PD15	CTC_SYN C		TIMER3_C H3										EXMC_D1			EVENTOU T

PE

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0			TIMER3_E TI										EXMC_NB L0	DCI_D2		EVENTOU T
PE1		TIMER0_C H1_ON											EXMC_NB L1	DCI_D3		EVENTOU T
PE2	TRACECK											ENET_MII _TXD3	EXMC_A2 3			EVENTOU T
PE3	TRACED0												EXMC_A1 9			EVENTOU T
PE4	TRACED1												EXMC_A2 0	DCI_D4		EVENTOU T
PE5	TRACED2			TIMER8_C H0									EXMC_A2 1	DCI_D6		EVENTOU T

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE6	TRACED3			TIMER8_C H1									EXMC_A2 2	DCI_D7		EVENTOU T
PE7		TIMER0_E TI											EXMC_D4			EVENTOU T
PE8		TIMER0_C H0_ON											EXMC_D5			EVENTOU T
PE9		TIMER0_C H0											EXMC_D6			EVENTOU T
PE10		TIMER0_C H1_ON											EXMC_D7			EVENTOU T
PE11		TIMER0_C H1											EXMC_D8			EVENTOU T
PE12		TIMER0_C H2_ON											EXMC_D9			EVENTOU T
PE13		TIMER0_C H2											EXMC_D1 0			EVENTOU T
PE14		TIMER0_C H3											EXMC_D1 1			EVENTOU T
PE15		TIMER0_B RKIN											EXMC_D1 2			EVENTOU T

\mathbf{PF}

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0	CTC_SYN C				I2C1_SDA								EXMC_A0			EVENTOU T
PF1					I2C1_SCL								EXMC_A1			EVENTOU T
PF2					I2C1_SMB A								EXMC_A2			EVENTOU T
PF3					I2C1_TXF RAME								EXMC_A3			EVENTOU T
PF4													EXMC_A4			EVENTOU T
PF5													EXMC_A5			EVENTOU T

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF6				TIMER9_C H0									EXMC_NI ORD			EVENTOU T
PF7				TIMER10_ CH0									EXMC_NR EG			EVENTOU T
PF8										TIMER12_ CH0			EXMC_NI OWR			EVENTOU T
PF9										TIMER13_ CH0			EXMC_CD			EVENTOU T
PF10													EXMC_INT R	DCI_D11		EVENTOU T
PF11													EXMC_SD NRAS	DCI_D12		EVENTOU T
PF12													EXMC_A6			EVENTOU T
PF13													EXMC_A7			EVENTOU T
PF14													EXMC_A8			EVENTOU T
PF15													EXMC_A9			EVENTOU T

\mathbf{PG}

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG0													EXMC_A1 0			EVENTOU T
PG1													EXMC_A1 1			EVENTOU T
PG2													EXMC_A1 2			EVENTOU T
PG3													EXMC_A1 3			EVENTOU T
PG4													EXMC_A1 4			EVENTOU T
PG5													EXMC_A1 5			EVENTOU T
PG6													EXMC_INT 1	DCI_D12		EVENTOU T

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG7									USART5_ CK				EXMC_INT 2	DCI_D13		EVENTOU T
PG8									USART5_ RTS			ENET_PP S_OUT	EXMC_SD CLK			EVENTOU T
PG9									USART5_ RX				EXMC_NE 1/EXMC_N CE2	DCI_VSYN C		EVENTOU T
PG10													EXMC_NC E3_0/EXM C_NE2	DCI_D2		EVENTOU T
PG11												ENET_MII _TX_EN/E NET_RMII _TX_EN	EXMC_NC	DCI_D3		EVENTOU T
PG12									USART5_ RTS				EXMC_NE 3			EVENTOU T
PG13	TRACED2								USART5_ CTS			ENET_MII _TXD0/EN ET_RMII_ TXD0	EXMC_A2			EVENTOU T
PG14	TRACED3								USART5_ TX			ENET_MII _TXD1/EN ET_RMII_ TXD1	EXMC_A2 5			EVENTOU T
PG15									USART5_ CTS				EXMC_SD NCAS	DCI_D13		EVENTOU T

PH

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH0																EVENTOU T
PH1																EVENTOU T
PH2												ENET_MII _CRS	EXMC_SD CKE0			EVENTOU T
PH3					I2C1_TXF RAME							ENET_MII _COL	EXMC_SD NE0			EVENTOU T

PH4				I2C1_SCL				USBHS_U LPI_NXT				EVENTOU T
PH5				I2C1_SDA						EXMC_SD NWE		EVENTOU T
PH6				I2C1_SMB A			TIMER11_ CH0		ENET_MII _RXD2	EXMC_SD NE1	DCI_D8	EVENTOU T
PH7				I2C2_SCL					ENET_MII _RXD3	EXMC_SD CKE1	DCI_D9	EVENTOU T
PH8				I2C2_SDA						EXMC_D1 6	DCI_HSYN C	EVENTOU T
PH9				I2C2_SMB A			TIMER11_ CH1			EXMC_D1 7	DCI_D0	EVENTOU T
PH10		TIMER4_C H0		I2C2_TXF RAME						EXMC_D1 8	DCI_D1	EVENTOU T
PH11		TIMER4_C H1								EXMC_D1 9	DCI_D2	EVENTOU T
PH12		TIMER4_C H2								EXMC_D2 0	DCI_D3	EVENTOU T
PH13			TIMER7_C H0_ON				CAN0_TX			EXMC_D2 1		EVENTOU T
PH14			TIMER7_C H1_ON							EXMC_D2 2	DCI_D4	EVENTOU T
PH15			TIMER7_C H2_ON							EXMC_D2 3	DCI_D11	EVENTOU T

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PI0			TIMER4_C H3			SPI1_NSS/ I2S1_WS							EXMC_D2 4	DCI_D13		EVENTOU T
PI1						SPI1_SCK/ I2S1_CK							EXMC_D2 5	DCI_D8		EVENTOU T
PI2				TIMER7_C H3		SPI1_MIS O	I2S1_ADD _SD						EXMC_D2 6	DCI_D9		EVENTOU T
PI3				TIMER7_E TI		SPI1_MOS I/I2S1_SD							EXMC_D2 7	DCI_D10		EVENTOU T

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PI4				TIMER7_B RKIN									EXMC_NB L2	DCI_D5		EVENTOU T
PI5				TIMER7_C H0									EXMC_NB L3	DCI_VSYN C		EVENTOU T
PI6				TIMER7_C H1									EXMC_D2 8	DCI_D6		EVENTOU T
PI7				TIMER7_C H2									EXMC_D2 9	DCI_D7		EVENTOU T
PI8																EVENTOU T
PI9										CAN0_RX			EXMC_D3 0			EVENTOU T
PI10												ENET_MII _RX_ER	EXMC_D3 1			EVENTOU T
PI11											USBHS_U LPI_DIR					EVENTOU T