Q2 (d), (e), (f)

CS2100 - Tutorial 7 - Direct Mapped Cache

Week 9

1. Direct Mapped

Cache block size = 4 = 2^2 bytes

Number of cache blocks = 16 = 2^4

"Cross out previous workings"

No.	Memory Address [Dec: Binary]		Cache Hit / Miss
1	4:	00…00 0000 0100	Miss
2	16:	00…00 0001 0000	Miss
3	32:	00…00 0010 0000	Miss
4	20:	00…00 0001 0100	Miss
5	80:	00…00 0101 0000	Miss
6	68:	00…00 0100 0100	Miss
7	76:	00…00 0100 1100	Miss
8	224:	00…00 1110 0000	Miss
9	36:	00…00 0010 0100	Miss
10	44:	00…00 0010 1100	Miss
11	16:	00…00 0001 0000	Miss
12	172:	00…00 1010 1100	Miss
13	20:	00…00 0001 0100	Hit
14	24:	00…00 0001 1000	Miss
15	36:	00…00 0010 0100	Hit
16	68:	00…00 0100 0100	Hit

Cache block	Valid bit	Tag	Word
0			
1	1	1	Mem[68]
2			
3	1	1	Mem[76]
4	1	0	Mem[16]
5	1	0	Mem[20]
6	1	0	Mem[24]
7			
8	1	3	Mem[224]
9	1	0	Mem[36]
10			
11	1	2	Mem[172]
12			
13			
14			
15			

2. AY11/12 Assignment #4

Cache block size = 2^4 bytes

Number of cache blocks = 2^1

(a).

Instruction Cache Block 0	~~[i0, i1, i2, i3]~~ ~~[i8, i9, i10, i11]~~ [i16, i17, i18, i19]
Instruction Cache Block 1	~~[empty]~~ ~~[i4, i5, i6, i7]~~ [i12, i13, i14, i15]

i0:

i1: Miss

i2: Hit

i3: Hit

0x10 ← i4: Miss

i5: Hit

i6: Hit

i7: Hit

0x20 ← i8: Miss

i9: Hit

i10: Hit

i11: Hit

0x38 ← i14: Miss

i15: Hit

i16: Miss

(b). No. of hits: 2 (i1, i2, i3) + 10 (i4 to i16) (7) = 72

(d). Cache block size = 2^3 bytes

Number of cache blocks = 2^1

Data cache block 0: s[32..39]

Data cache block 1: s[24..31]

(e).

(f).