CS2100 - Tutorial 6 - Pipelining

Week 8

1. Pipelining Basics

1000 1101 1111 1000 0...0 (16 zeros)

(i).

```
i.   0x8df80000   # lw $24, 0($15)      #Inst.Addr = 0x100
```

IF / ID	
No Control Signal	----- ----
PC+4	0x104
OpCode	0x23
Rs	$15
Rt	$24
Rd	X
Funct	X
Imm(16)	0

ID / EX	
MToR	1
RegWr	1
MemRd	1
MemWr	ϕ
Branch	ϕ
RegDst	ϕ
ALUsrc	1
ALUop	00
PC+4	0x104
RData1	116_{10}
RData2	X
Rt	$24
Rd	X
Imm(32)	0

EX / MEM	
MToR	1
RegWr	1
MemRd	1
MemWr	ϕ
Branch	ϕ
BrcTgt	0x104
isZero?	ϕ
AluRes	$116_{10}+0$
RData2	$24
DstRNum	$24

MEM / WB	
MToR	1
RegWr	1
MemRes	Mem($116_{10}+0$)
AluRes	$116_{10}+0$
DstRNum	$24

ii. `0x1023000C  # beq $1, $3, 12     #Inst.Addr = 0x100`

IF / ID	
No Control Signal	----- ----
PC+4	0x104
OpCode	0x4
Rs	$1
Rt	$3
Rd	X
Funct	X
Imm(16)	12_{10}

ID / EX	
MToR	X
RegWr	ϕ
MemRd	ϕ
MemWr	ϕ
Branch	1
RegDst	X
ALUsrc	ϕ
ALUop	01
PC+4	0x104
RData1	102_{10}
RData2	104_{10}
Rt	$3
Rd	X
Imm(32)	12_{10}

EX / MEM	
MToR	X
RegWr	ϕ
MemRd	ϕ
MemWr	ϕ
Branch	1
BrcTgt	0x110
isZero?	ϕ
AluRes	-2_{10}
RData2	104_{10}
DstRNum	$3

MEM / WB	
MToR	X
RegWr	ϕ
MemRes	X
AluRes	-2_{10}
DstRNum	$3

... 0010 0010

iii. `0x0285c822  # sub $25, $20, $5  #Inst.Addr = 0x100`

IF / ID	
No Control Signal	----------
PC+4	0x104
OpCode	0x0
Rs	$20
Rt	$5
Rd	$25
Funct	0x22
Imm(16)	X

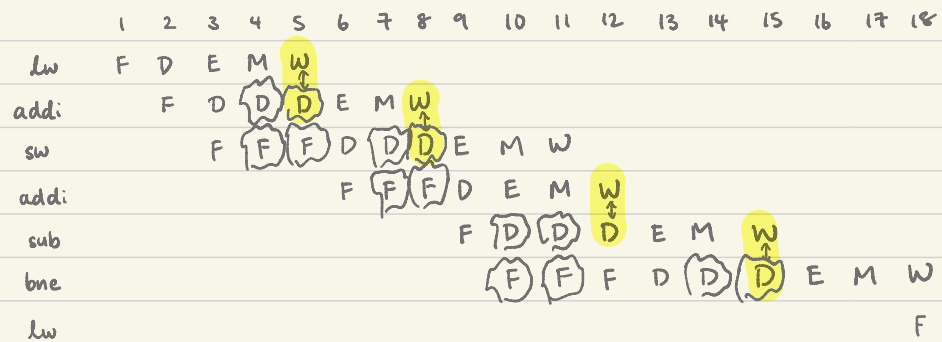
ID / EX	
MToR	ϕ
RegWr	1
MemRd	ϕ
MemWr	ϕ
Branch	ϕ
RegDst	1
ALUsrc	ϕ
ALUop	10
PC+4	0x104
RData1	121_{10}
RData2	106_{10}
Rt	$5
Rd	$25
Imm(32)	X

EX / MEM	
MToR	ϕ
RegWr	1
MemRd	ϕ
MemWr	ϕ
Branch	ϕ
BrcTgt	X
isZero?	ϕ
AluRes	15_{10}
RData2	106_{10}
DstRNum	$25

MEM / WB	
MToR	ϕ
RegWr	1
MemRes	X
AluRes	15_{10}
DstRNum	$25

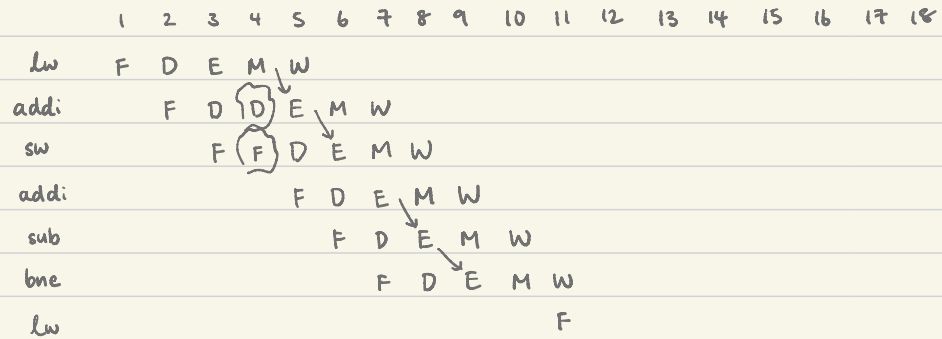
2. Pipeline Hazards

(a).



Total cycles : 18

(b).



Total cycles : 11

(c).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
lw																		
addi																		
sw																		
addi																		
sub																		
bne																		
lw																		

Total cycles :

(d).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
lw																		
addi																		
sw																		
addi																		
sub																		
bne																		
lw																		

Total cycles :

(e).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
lw																		
addi																		
sw																		
addi																		
sub																		
bne																		
lw																		

Total cycles :

3. Data Forwarding Mechanism

(a). Latch information

(b). Datapath

(c). Signal

```
sub $2, $1, $3     #i
and $12, $2, $5    #i+1
```