ECE411 – Checkpoint 4 – Group2

bslevin2
erjohns3
pickar2

Progress

In this checkpoint, three new features were added to our pipelined LC3b processor. First, branch prediction was implemented in a static taken fashion. The IF block will calculate the new offset address and that will be sent to the PC. If there is a miss prediction, the current IF_ID, ID_EX, and EX_MEM will be reset to 0 (NOP) on the upcoming clock rise.

In addition, performance counters were implemented. They will increment based on a certain event and are resettable. Examples of where they are used includes cache hits, cache misses, branch taken, branch miss prediction, pipeline stalls, and so on. They can be accessed by reading from memory at locations 0xFFE0 or higher by the LDR command. They can be reset by writing any value to those addresses with STR.

The eviction buffer was implemented into memory between the L2 Cache and main memory. It stores the values for write when physical memory is busy and cannot be used.

- Branch prediction, counters, writing testcode, and debugging were done by `pickar2` (John).
- The eviction buffer was implemented by `erjohns3` (Eric).

Roadmap

The current roadmap for Checkpoint 5 is to fix a few performance issues and then implement advanced features. One such performance issue would be the data forwarding and hazard module. It forwards on the same clock cycle, thus some commands will have to travel through the entirety of the execute stage once again. The plan is to add a register to hold the value to make it take an additional cycle, thus speeding up the

clock. The estimated performance gain would be 103 ns --> 130 ns (this is estimated from the loss due to forwarding).

For advanced design, we are looking to implement a multi-cycle L2 Cache. Due to our large cache size (32 byte cache lines, 4 ways), it would improve performance. In addition, we are also looking towards the branch prediction options and memory stage leapfrogging.