ECE411 – Checkpoint 2 – Group2

bslevin2
erjohns3
pickar2

Progress

A LC3*b* CPU with pipelining was implemented. Furthermore, it utilizes an instruction and data cache that get their data from simulated memory (200 ns delay) through an arbiter. As a result, the LC3*b* architecture checks for stalls from cache misses. Currently, branch prediction and data hazards are ignored, but it will perform correctly if NOPs are inserted as a buffer in the necessary places.

- Everything for this checkpoint was done by `pickar2` (John).
- The arbiter was initially done by `erjohns3` (Eric), but due to errors and debugging time it was rewritten.

Roadmap

Currently, there is no roadmap planned due to minimal or lack of team contribution. I (`pickar2`) plan to continue working on it whenever I have time.

Late Turn-in

Due to lack of group contribution, not everything was completed in time. This section hopes to clarify what was done on time and what was not.

The following were completed before the deadline:

- Basic LC3*b* pipelined data path (some instructions did not work properly, see section below for more info)
- Split L1 Caches (Magic memory was used; no arbiter present)
- Arbiter with compilation issues and bugs (thus not used)

After the deadline, I was the only one contributing to fixing any additional issues. It was done in around a week's time due to time constraints with other classes. The following are implemented features or corrected issues done after the deadline:

- Fixed LC3b TRAP command and basic control signal bug
- Fixed LC3b xxb commands
- Fixed LC3b xxi commands to work with two memory operations when memory delay was present. This allowed the full LC3b instruction set to be implemented with simulated memory (200ns delay).
- Remade Arbiter to perform correctly.
- Updated the data path diagram with and without pipelining.
- Write the progress report.