# ECE411 MP3

#### April 29<sup>th</sup> Spring 2017 Group2

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### Design Features

Four-way Set Associative L2 Cache

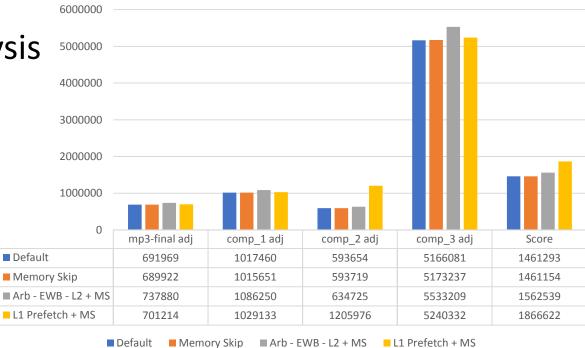
Hardware Prefetching (Basic – icache)

Memory Stage Leapfrogging

#### Quantitative Analysis

Advanced Feature Performance





122.91 MHz (8.137 ns) 122.74 MHz (8.148 ns) 114.76 MHz (8.714 ns)

121.17 MHz (8.253 ns)

- Performance Considerations
  - Critical Paths

## Looking Back

Greater focus on clock speed

 Early design choices taking into consideration future advanced features into account