ECE411 – Checkpoint 3 – Group2

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Progress

Hazard detection and forwarding along with an L2 Cache was implemented for this checkpoint. For forwarding, data is moved from the output of MEM to the start of EX (so it will recalculate values) or to the registers right before EX. Likewise, the output of EX is also forwarded right before EX, and takes priority for forwarding over MEM.

Unfortunately, due to the current implementation of the forwarding from MEM to EX (where it passes through EX on the same clock cycle), it has greatly lowered our clock speed from ~130ns to ~100ns. Time will be spent resolving the issue with this critical path.

As for data hazards, if a memory operation that is not a single cycle is taking place, data behind it in the pipeline will jump over it and on to write back provided it does not modify the PC, needs the value that the memory operation is obtaining, or requires a memory operation itself.

- All forwarding and data hazard work and debugging was done by `pickar2` (John).
- Each group member worked on the L2 Cache, `pickar2`'s implementation was used.

Roadmap

Currently, there is no roadmap planned due not knowing how much group members know of the current project's code and preference to advanced design.