ECE411 – Checkpoint 1 – Group2

bslevin2
erjohns3
pickar2

Progress

A LC3α CPU with pipelining was implemented (Instructions ADD(i), AND(i), NOT, LDR, STR, and BR). It utilizes magic memory that reads and writes instantly; thus it does not need to check for cache misses or memory stalls. Furthermore, branch prediction and data hazards are ignored, but it will perform correctly if NOPs are inserted as a buffer in the necessary places.

- All three group members worked on the CPU's paper diagram.
- The implementation (SystemVerilog), testing, and debugging were done by `pickar2` (John).
- The Memory paper design (4-way L2 Cache and Arbiter) was done by `erjohns3` (Eric).

Roadmap

The current workload distribution for checkpoint 2 has not been determined at the present time due to `bslevin2` (Ben) being out of town due to a family emergency. It is currently predicted that `pickar2` (John) will continue on the LC3-b ISA and memory access, `erjohns3` (Eric) on the arbiter and 4-way L2 Cache, and all of us on the data-forwarding paper design. This is subject to change when `bslevin2` (Ben) is available.