**INHA UNIVERSITY TASHKENT**

**DEPARTMENT OF CSE & ICE**

**SPRING SEMESTER 2017**

**SOC 2060 - COMPUTER ARCHITECTURE**

**HOME ASSIGNMENT 2**

**Submitted by**

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**Student ID U1510060**

**Group: 15.1 Sophomore**



**INSTRUCTIONS :**

**- Answer All the QUESTIONS**

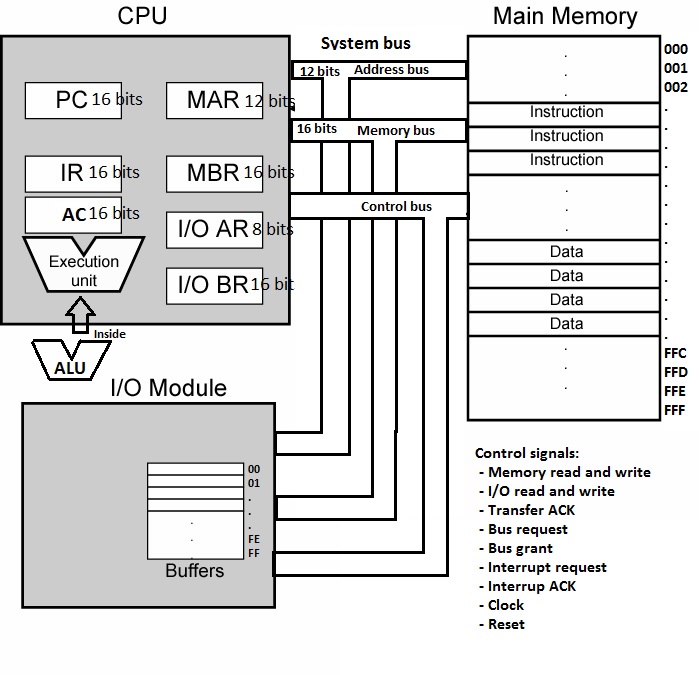
**- Home Assignments are to be carried out individually and not in Groups**

**- Home Assignment Report should be prepared using this Template provided**

**- Last date for submission of the Home Assignment is 16th March 2017**

**- Late submissions not entertained, Adhere to the deadline strictly**

1. A.



B.

|  |  |  |  |
| --- | --- | --- | --- |
| **Address** | **Instruction** | **Machine code (Hex)** | **RTL Notation** |
| 200 | LD 300 | 0300 | AC 🡨[300] |
| 202 | ADD 302 | 2302 | AC🡨AC+[302] |
| 204 | ST 350 | 1350 | [350]🡨AC |
| 206 | LD 302 | 0302 | AC🡨[302] |
| 208 | SUB 300 | 3300 | AC🡨AC-[300] |
| 20A | ST 352 | 1352 | [352]🡨AC |
| 20C | LD 350 | 0350 | AC🡨[350] |
| 20E | NOT AC | B060 | AC🡨~AC |
| 210 | AND 352 | 9352 | AC🡨 AC &[352] |
| 212 | ST 354 | 1354 | [354]🡨AC |
| 214 | LD 352 | 0352 | AC🡨[352] |
| 216 | NOT AC | B020 | AC🡨~AC |
| 218 | AND 350 | 2350 | AC🡨AC+[350] |
| 21A | OR 354 | A354 | AC🡨AC||[354] |
| 21C | ST 354 | 1354 | [354]🡨AC |
| 21E | IN 10 | E010 | AC🡨[I/O 10] |
| 220 | ADD 304 | 2304 | AC🡨AC+[304] |
| 222 | OUT 20 | F020 | [I/O 20]🡨AC |

iii. Data are in hexadecimal form

This table shows all steps for the first instruction

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Address | Data | | Address | Data |
|  | Step 1 | Step 2 | Step 3 | Step 4 | 200 | 0300 | 300 | | 20 |
| PC | 200 | 202 | 202 | 202 | 202 | 2302 | 301 | | 00 |
| MAR | 200 | 200 | 200 | 200 | 204 | 1350 | 302 | | 40 |
| MBR |  | 0300 | 0300 | 0300 | 206 | 0302 | 303 | | 00 |
| IR |  |  | 0300 | 0300 | 208 | 3300 | 304 | | 20 |
| AC |  |  |  | 0020 | … | 1352 | … | | 00 |

The following table includes all 18 instructions’ step 4 only

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Address** | **Data** | **Address** | **Data** |  | № | PC | MAR | MBR | IR | AC |  |
| 200 | 0300 | 300 | 20 |  | 1 | 202 | 200 | 0300 | 0300 | 0020 |  |
| 202 | 2302 | 301 | 00 |  | 2 | 204 | 202 | 2302 | 2302 | 0060 |  |
| 204 | 1350 | 302 | 40 |  | 3 | 206 | 204 | 1350 | 1350 | 0060 |  |
| 206 | 0302 | 303 | 00 |  | 4 | 208 | 206 | 0302 | 0302 | 0040 |  |
| 208 | 3300 | 304 | 20 |  | 5 | 20A | 208 | 3300 | 3300 | 0020 |  |
| 20A | 1352 | 305 | 00 |  | 6 | 20C | 20A | 1352 | 1352 | 0020 |  |
| 20C | 0350 | … |  |  | 7 | 20E | 20C | 0350 | 0350 | 0060 |  |
| 20E | B060 | 350 | **0060** |  | 8 | 210 | 20E | B060 | B060 | 009F |  |
| 210 | 9352 | 351 |  |  | 9 | 212 | 210 | 9352 | 9352 | 0000 |  |
| 212 | 1354 | 352 | **0020** |  | 10 | 214 | 212 | 1354 | 1354 | 0000 |  |
| 214 | 0352 | 353 |  |  | 11 | 216 | 214 | 0352 | 0352 | 0020 |  |
| 216 | B020 | ~~354~~ | **~~0000~~** |  | 12 | 218 | 216 | B020 | B020 | 00DF |  |
| 218 | 2350 | 354 | **0040** |  | 13 | 21A | 218 | 2350 | 2350 | 0040 |  |
| 21A | A354 | 355 |  |  | 14 | 21C | 21A | A354 | A354 | 0040 |  |
| 21C | 1354 | … |  |  | 15 | 21E | 21C | 1354 | 1354 | 0040 |  |
| 21E | E010 | 10 | 41 |  | 16 | 220 | 21E | E010 | E010 | 0041 |  |
| 220 | 2304 | … |  |  | 17 | 222 | 220 | 2304 | 2304 | 0061 |  |
| 222 | F020 | 20 | **0061** |  | 18 | 224 | 222 | F020 | F020 | 0061 |  |
|  |  | … |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  | IOAR | IOBR |  |  |  |

IV.

|  |  |
| --- | --- |
| Modified locations | Data in hex |
| 350 | 0060 |
| 352 | 0020 |
| 354 | 0040 |
| 20 | 0061 |
| **Accumulator** | **0061** |

1. a. 232-8 = 224 =16 MB

b. Program Counter – 24 bits

Instruction register – 32 bits

c. i. Perfect size. Because the memory are is from 000000 to FFFFFF that contains 24 bits of data and can be reached at one bus cycle. Data are also maximum 32 bits that can be transferred at one bus cycle too.

ii. Address bus reach at one bus cycle but data bus need 2 bus cycles

iii. Both address bus and data bus need 2 bus cycles to do task.

1. a. Through a single bus cycle, the 16-bit microprocessor transfers two byte while 32-bit microprocessor transfers four bytes. 32-bit microprocessor’s data transfer rate is **2 times** bigger than 16-bit’s, as both processors are identical.

b. 16-bit microprocessor 1000\*0.5 + (1000\*0.5)\*2=1500 bus cycles

32-bit microprocessor 1000\*0.5+1000\*0.5=1000 bus cycles

16-bit microprocessor needs **1.5 times** more bus cycles.

c. 16-bit microprocessor 1000\*0.3 + 1000\*0.3 + (1000\*0.4)\*2=1400 bus cycles

32-bit microprocessor 1000\*0.3+1000\*0.3 + 1000\*0.4=1000 bus cycles

16-bit microprocessor needs **1.4 times** more bus cycles.

4. a. Maximum bus cycle rate = 16 MHz / 4 = 4MHz/s  
Data transfer rate = 2 bytes/cycle  
Data transfer rate = bus cycle rate \* data per bus cycle = 4MHz/s \* 2bytes/cycle Data transfer rate = 8Mbytes/s = 223 bytes/s.

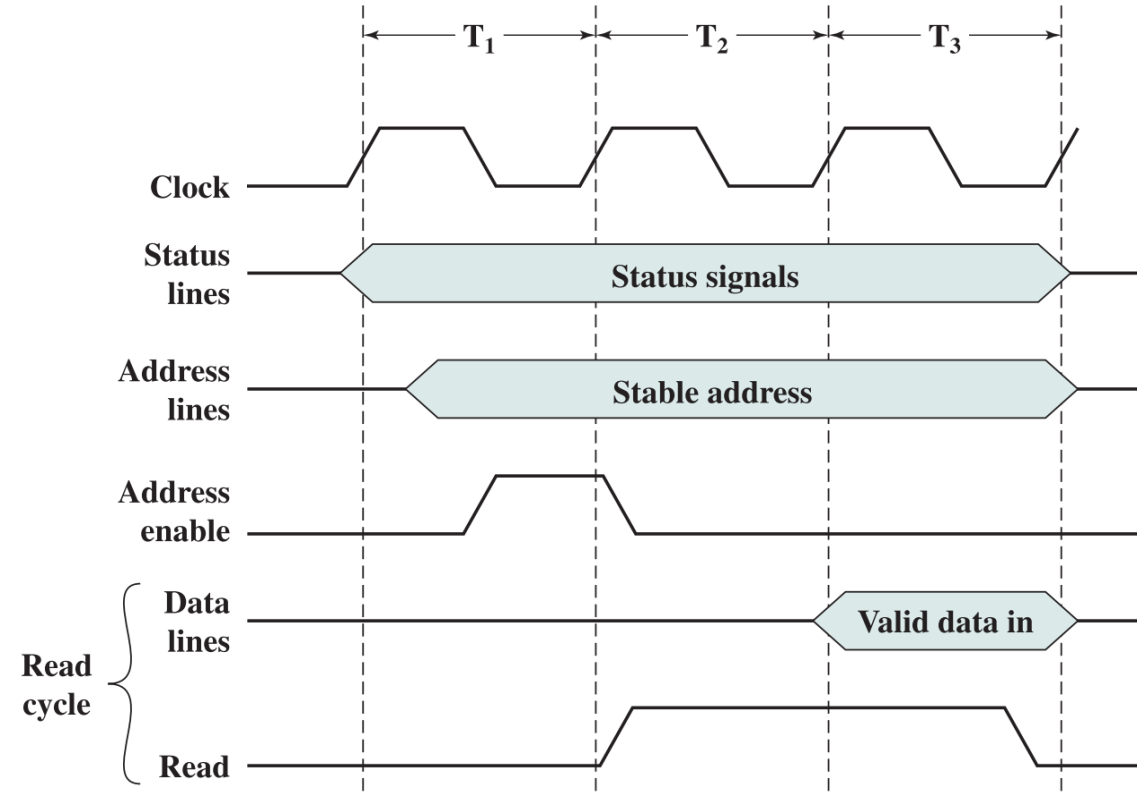
b. i. Data transfer rate = 4MHz/s \* 4bytes/cycle = 16 Mbytes/s = 24 bytes/s

ii. Data transfer rate = 8 MHz/s\*2bytes/cycle = 16 Mbytes/s = 24 bytes/s. Both of them increase performance equally.

5. a. As the clocking frequency is 10 MHz, the clock period is 10-7 s = 100 ns. Then we have three dime slots, thus it is 3\*100 ns = 300 ns.

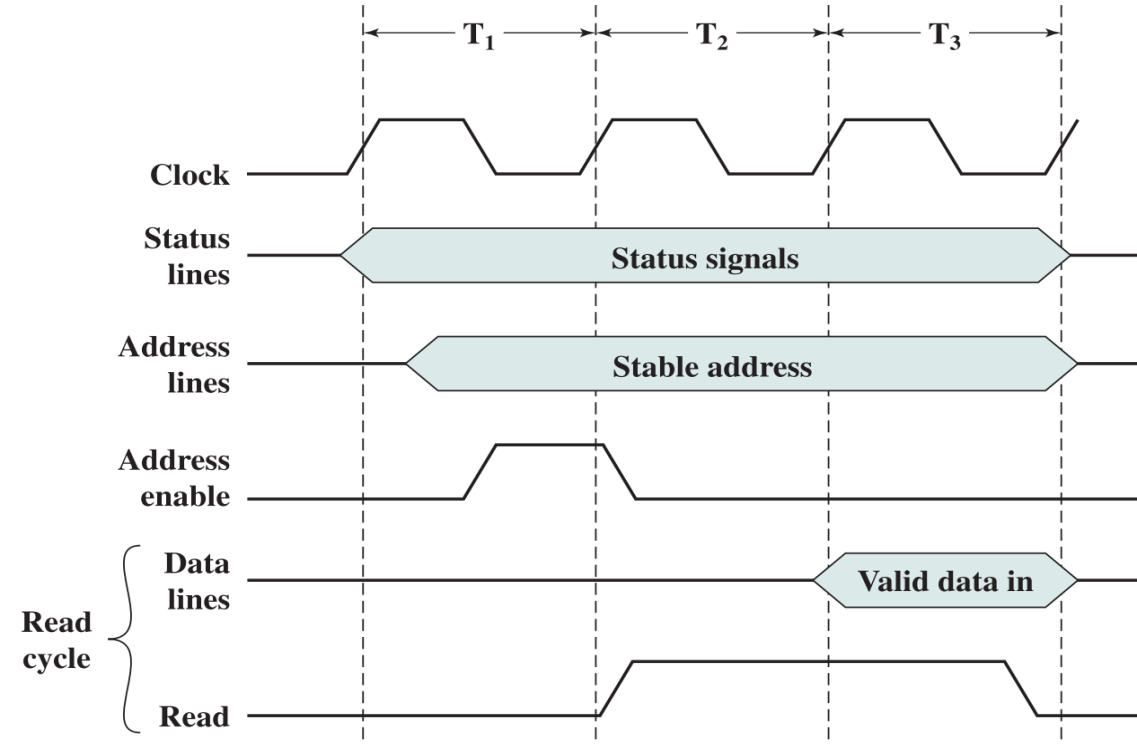
b. The middle of the second half of 100ns is 75 ns. Therefore, the memory must put the data on the bus before 75-20=55 ns from the beginning of T3.

c.



d. i. 2 clock cycles.

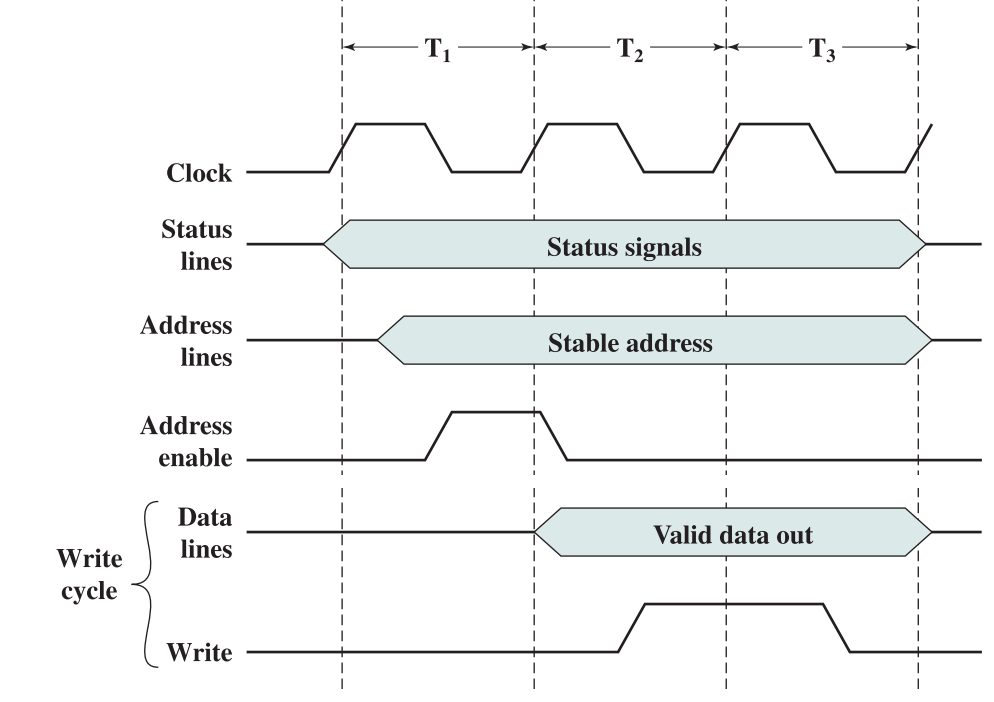
ii. at 200ns.

iii. 

**WAIT STATE**

6. a. The clock period is 200 ns which is inverse of clock rate. The write signal is 200 – 50 = 150 ns.

b. Total duration of valid data presentation to memory 150 + 20 = 170 ns

c. 

d. The number of wait states needed is 2 because we have 200ns

7. a. Fetch opcode + fetch operand address + fetch operand+1 to operand + store operand = 16 cycles. Time = 16 cycles \* 1/20 MHz = 800 ns.

b. As we have 4 operands we will have 4\*2=8 bus cycles. 8/16\*100% = **50% rise.**

c. Now instead of 16 cycles we have **24** cycles. 8/24 \* 100% = **33.3%** **rise**

d. Interrupt will be processed before fetching opcode and fetching operand address. Thus after 16 - 4 - 3 = **9** cycles interrupt enters. It is 9 \* 1/20MHz = 450 ns.

8. One bus cycle will be 1/40 = 25 ns. We have each 4\*25 = 100 ns

i. 100\*2 = 200 ns

ii. 100\*3 = 300 ns

iii. 100\*4 = 400 ns