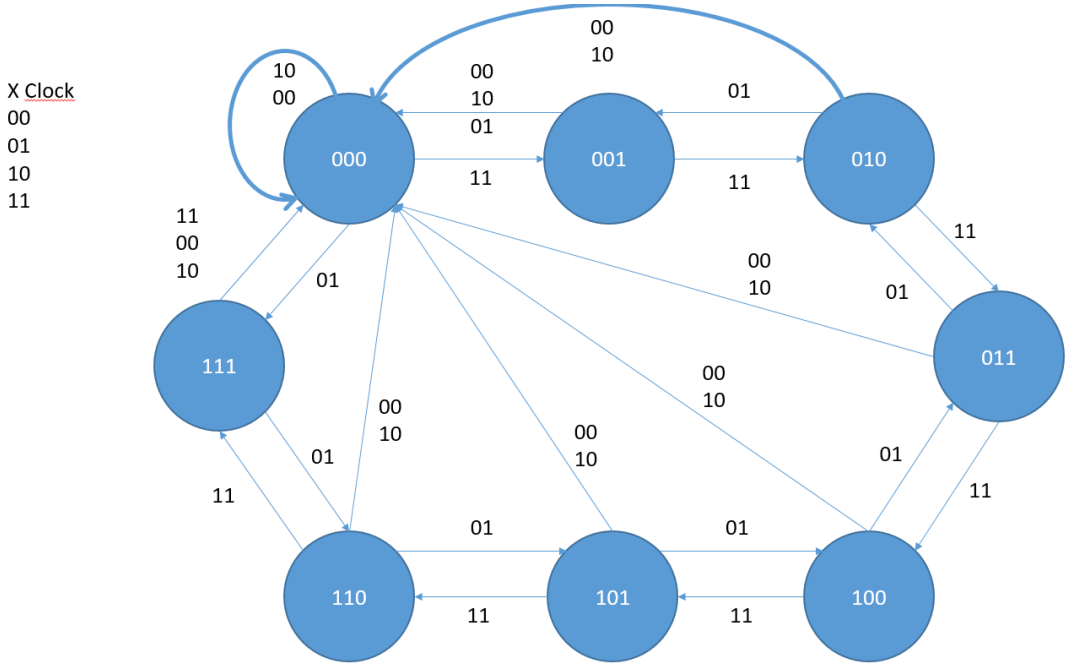
Muhammed Erkmen

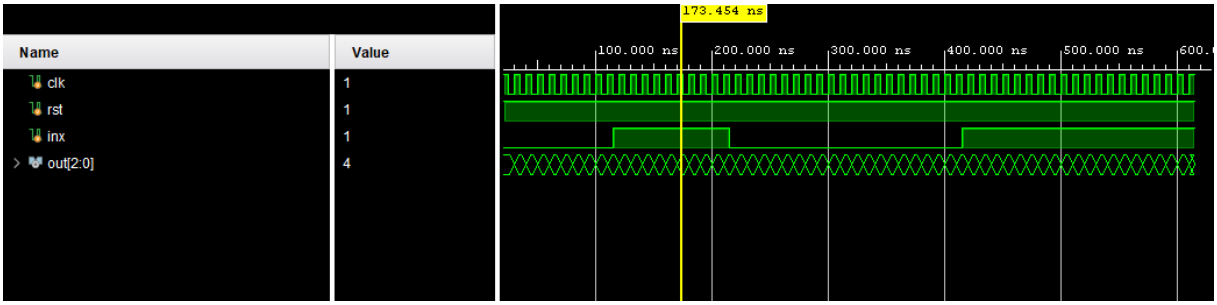
Assignment1 – Report

Question1

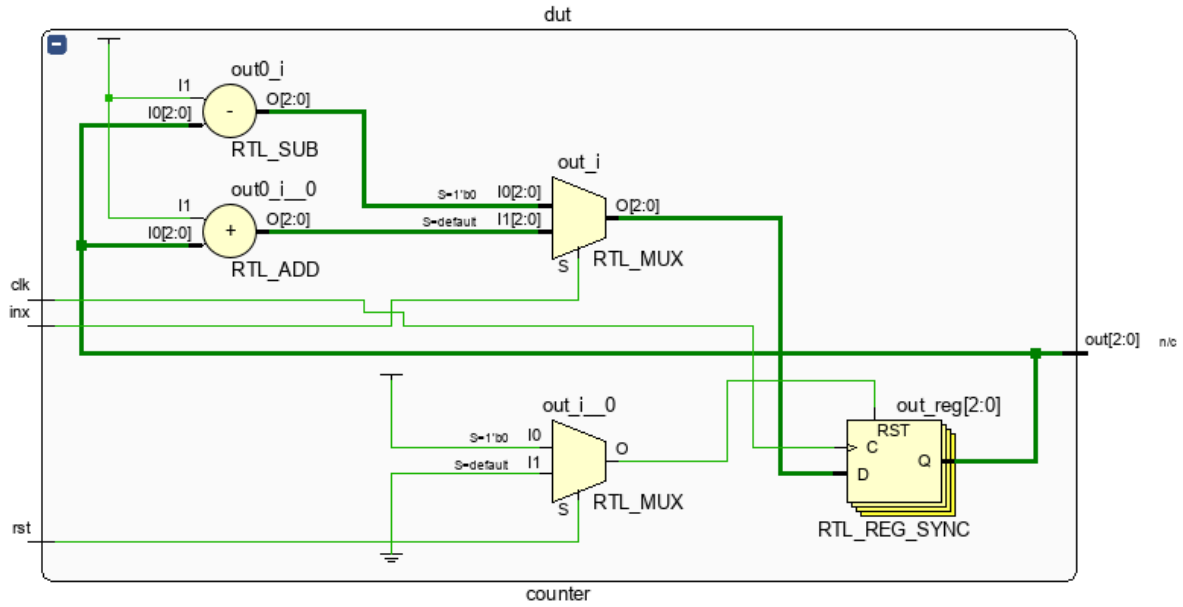
This circuit counts 0 to 7. If input X is 1, counts upwards. If input X is 0, stops and counts backwards.

State Diagram



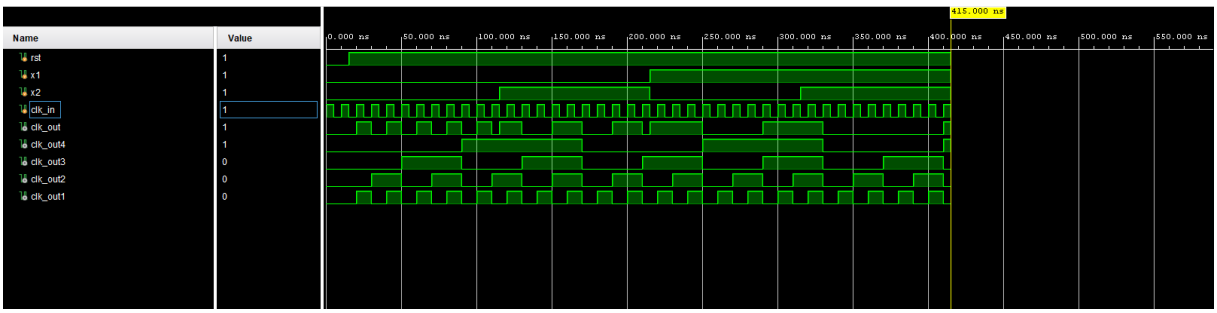


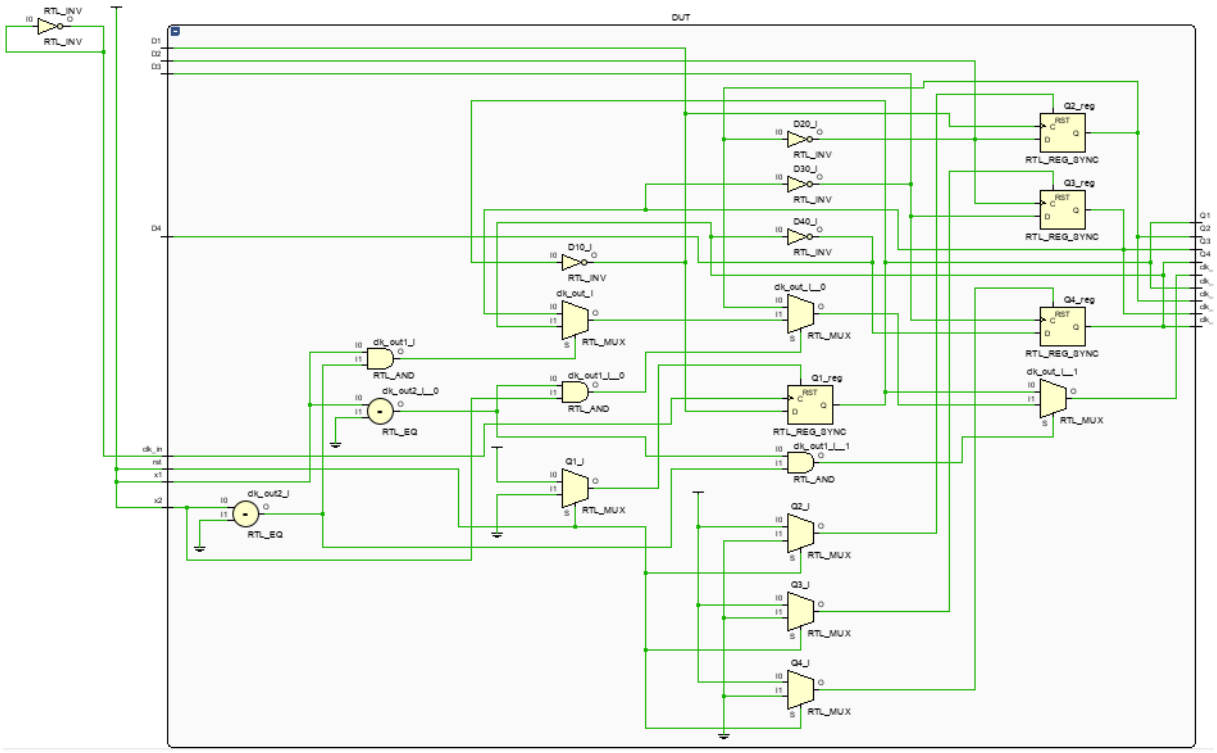
Inside of the circuit



Question2

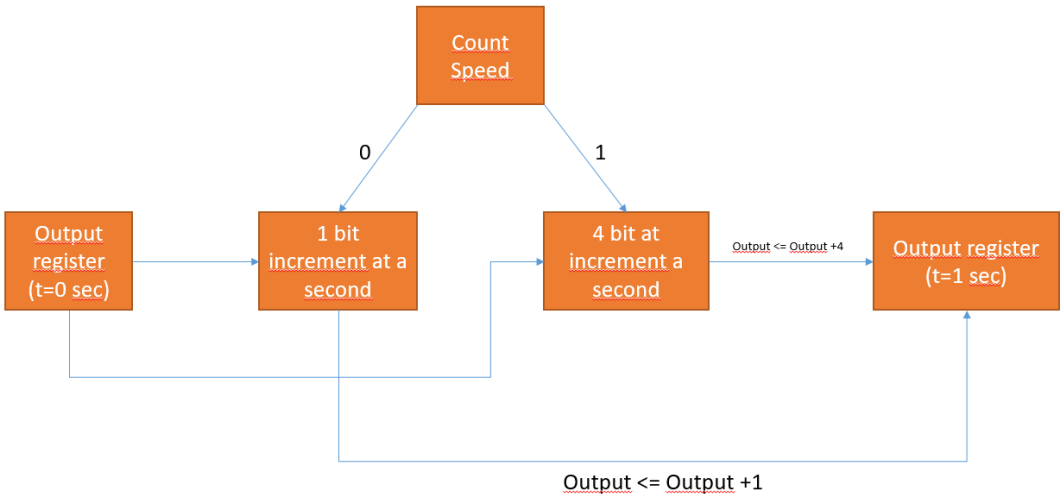
This circuit is a clock divider. There is 4 state input. 00 is divided by2, 01 is divided by4, 10 is divided by 8 and 11 is divided by 16. I coded it as a 4 D-latch, so graphs and circuits are given below.

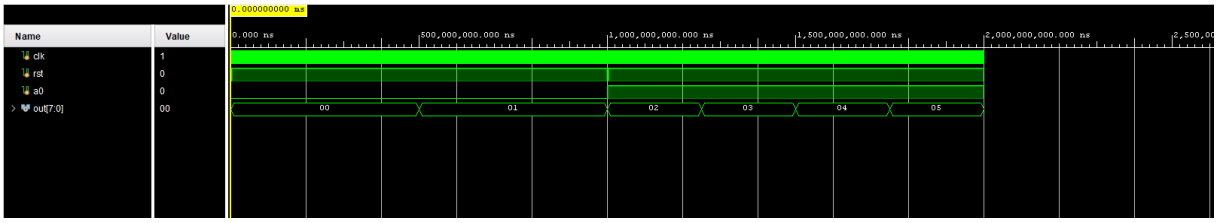




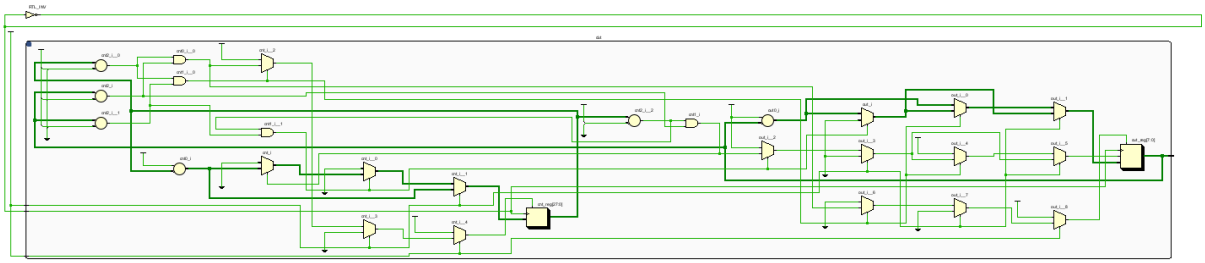
Question 3

This circuit is an 8bit counter with 2 different count speed. When A0 is 0, it counts 1 bit per second. When A0 is 1, it counts 4 bits per second.





Circuit



Question 4

Experiments tested on FPGA.