Assignment 2 Report

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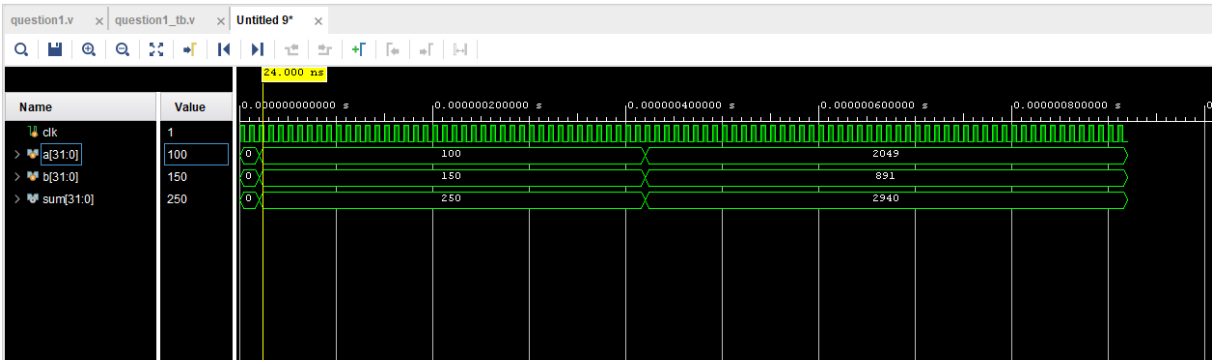
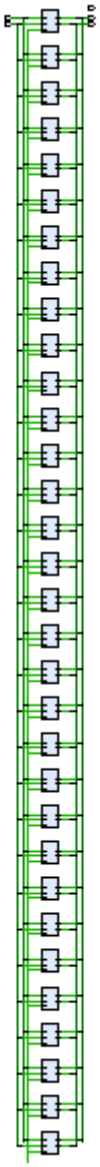
A)

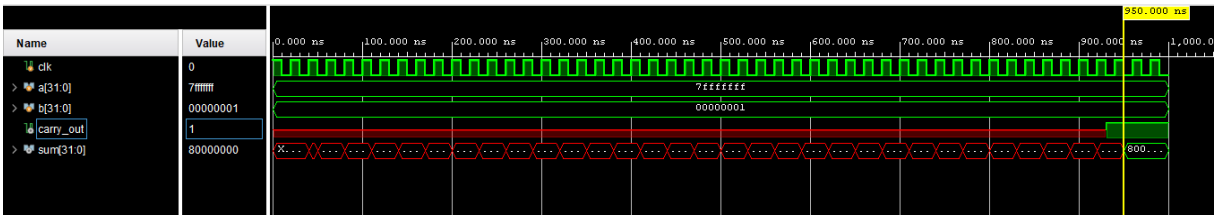
This circuit is an 32bit adder which is created by full adders. To create the full adders, i used generate block. There is no delay in this simulation.



B)

This simulation shows the delayed state. I added 15 ns delay to and&or gates, 20ns delay to XOR gates. Result is 950 ns. My calculation was 50 + 31*30 = 980 ns.




The implementation of the circuit is in the next page.