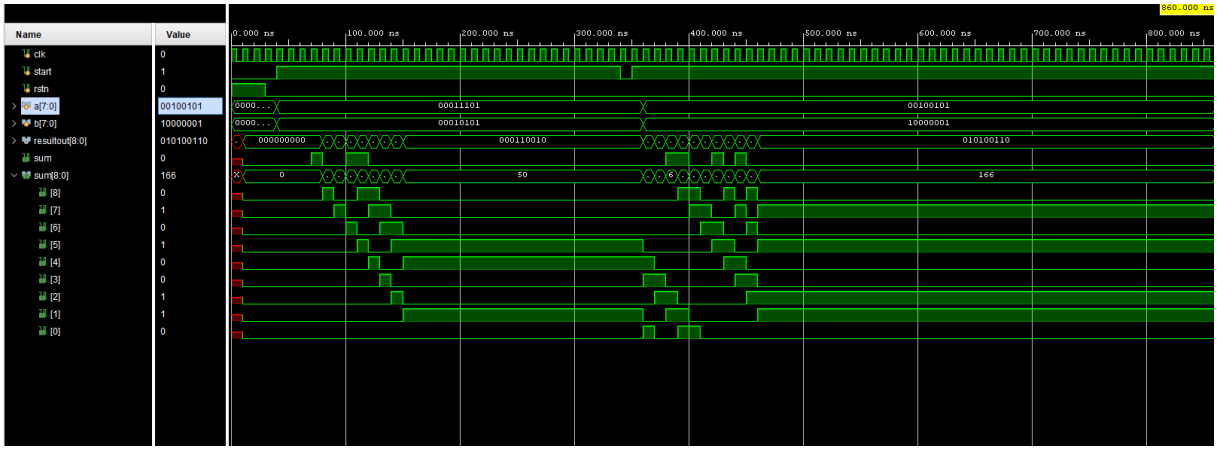
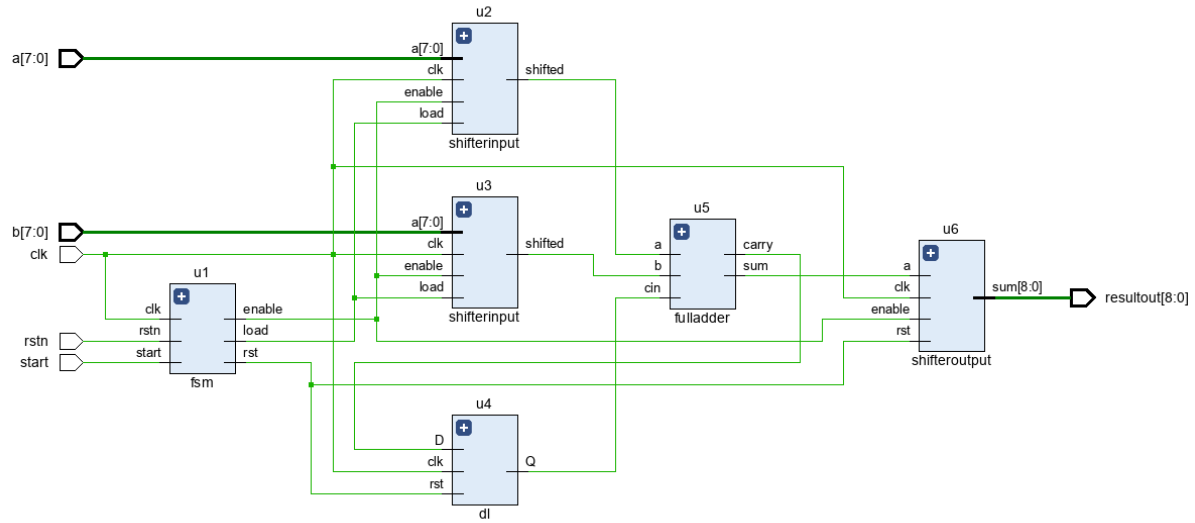
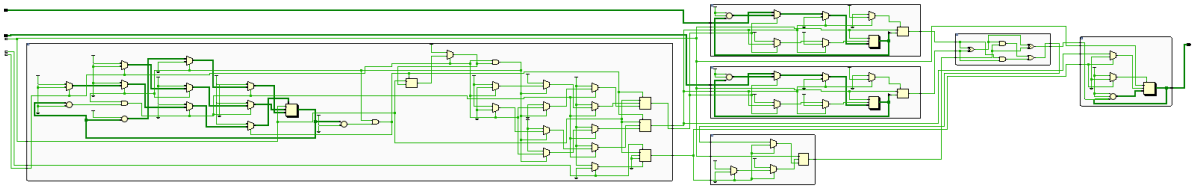
Muhammed Erkmen

Assignment – 3 Report

This system adds 2-8bit number with bit shifting method. It shifts last bits of the inputs and adds them with full adder + d latch topology. When start signal goes to 1-0-1 the circuit loads the new inputs and calculates the new sum. Testbench result is:



Circuit schematic is given below:


u2
a[7:0]
clk
enable
load
shifted
shifterinput
u3
a[7:0]
clk
enable
load
shifted
shifterinput
u5
a
b
cin
carry
sum
fulladder
u6
a
clk
enable
rst
sum[8:0]
shifteroutput
resultout[8:0]
a[7:0]
b[7:0]
clk
rstn
start
u1
clk
rstn
start
enable
load
rst
fsm
u4
D
clk
rst
Q
dl