Assignment 8

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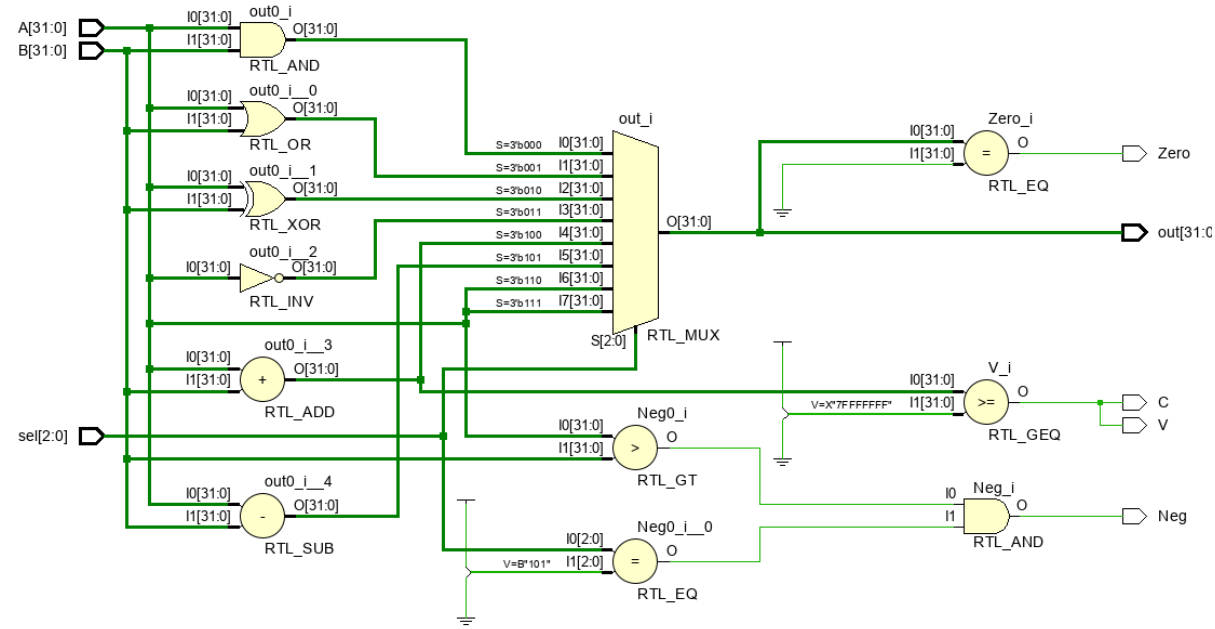
In this part of the assignment, i created an ALU block with using RISCV. In logical unit i have AND, OR , XOR and NOT operations. In arithmetic part i have ADD, SUB,LOADUI and ADDUI as wanted in the assignment paper.

ALU RTL SCHEMATIC



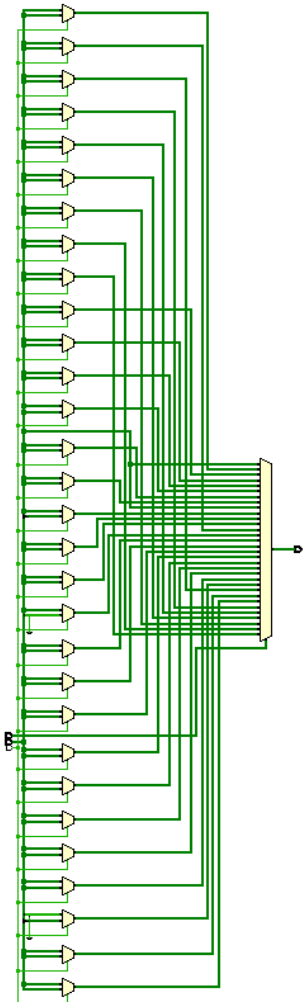
ALU TESTBENCH

100: ADD, 101: SUB, 110: LOADUI, 111: ADDUI, 000:AND, 001:OR, 010:XOR, 011:NOT

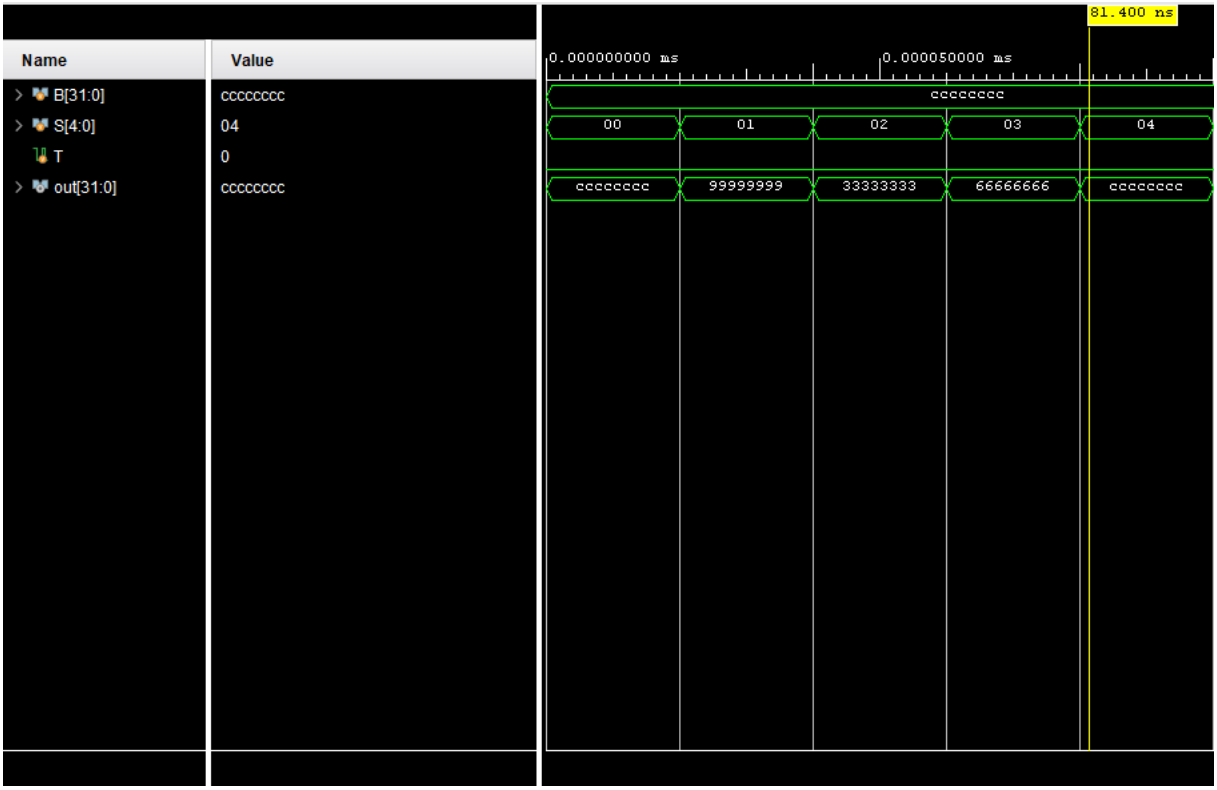
SHIFTER

I designed a shifter module without using shift(<< || >>) operator. This module shifts the input B. It shifts decimal(S[4:0]) bit right or left. It decides right or left using T input. If T = 0, it shifts left. If T=0, it shifts right.

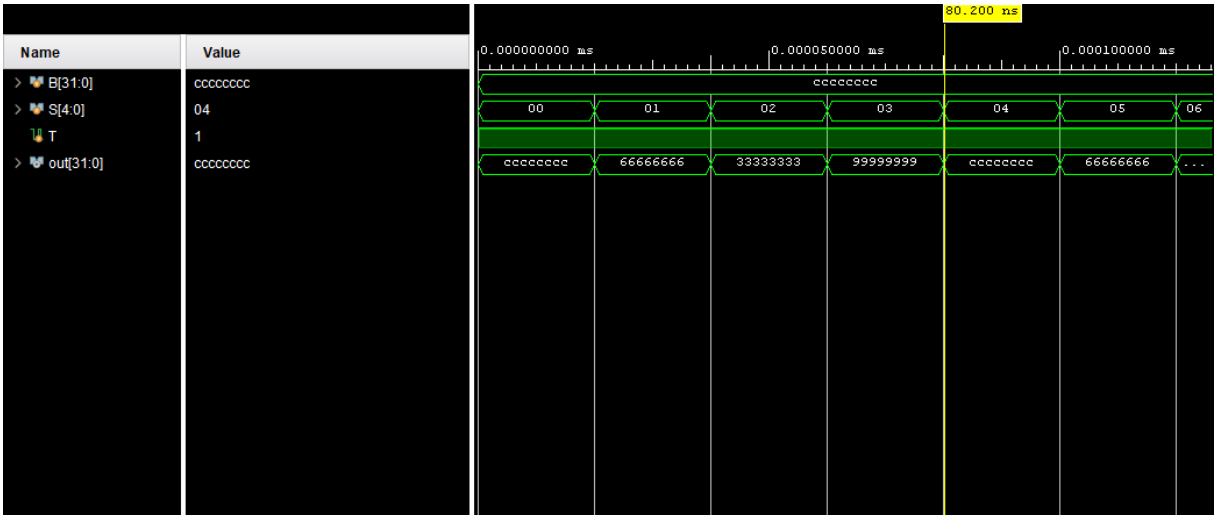
RTL Schematic of shifter:



Simulation results of shifting LEFT(T=0):



Simulation results of shifting RIGHT:



As expected, input 32'hCCCCCCCC comes output when selection is 4. When selection is 0, nothing changes in input and it goes directly to output. For left shifting, calculations has been showed in the next page.

For left shifting:

S=1:

1100_1100_1100_1100_1100_1100_1100_1100 >> 1001_1001_1001_1001_1001_1001_1001_1001

(CCCCCCC >>>> 9999999)

S=2:

1100_1100_1100_1100_1100_1100_1100_1100 >> 0011_0011_0011_0011_0011_0011_0011

(CCCCCCC >>>> 3333333)

S=3:

1100_1100_1100_1100_1100_1100_1100_1100 >> 0110_0110_0110_0110_0110_0110_0110_0110

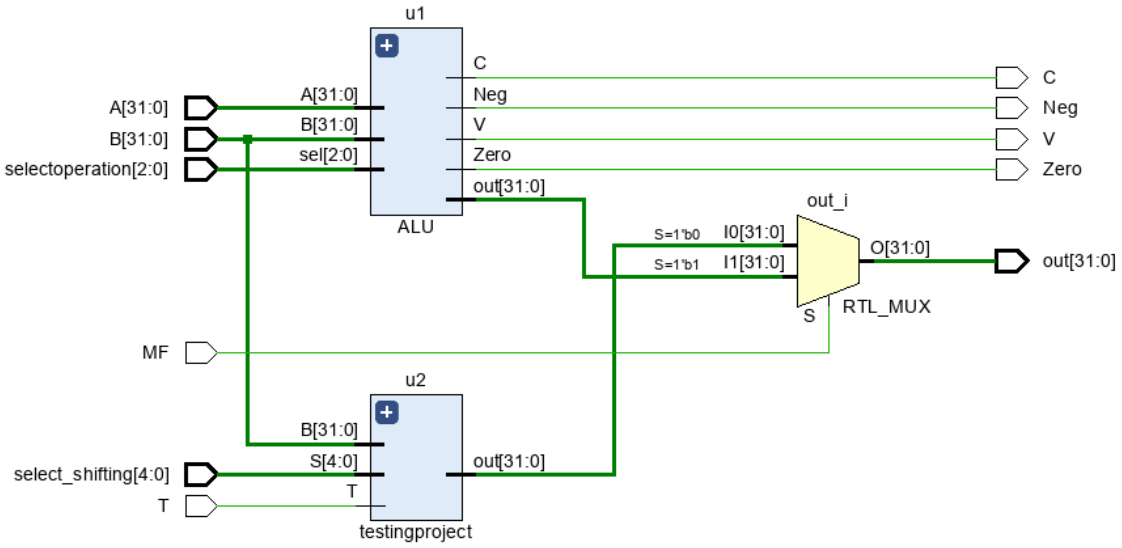
(CCCCCCC >>>> 6666666)

S=4:

1100_1100_1100_1100_1100_1100_1100_1100 >> 1100_1100_1100_1100_1100_1100_1100_1100

COMBINE AS FU:

MF is choosing output will go to SHIFTER's output or ALUs output. When MF=0 output goes to SHIFTERs output. When MF=1 output goes to ALUs output.



Simulation results show that system works correct.

MF=0 & T=0 :

Shifting S= 00: no change, 01: shifting 1 left, 02: shifting 2 left, 03:shifting 3 left

MF = 1:

Operation Select: 100: ADD, 101: SUBS