Assignment 5

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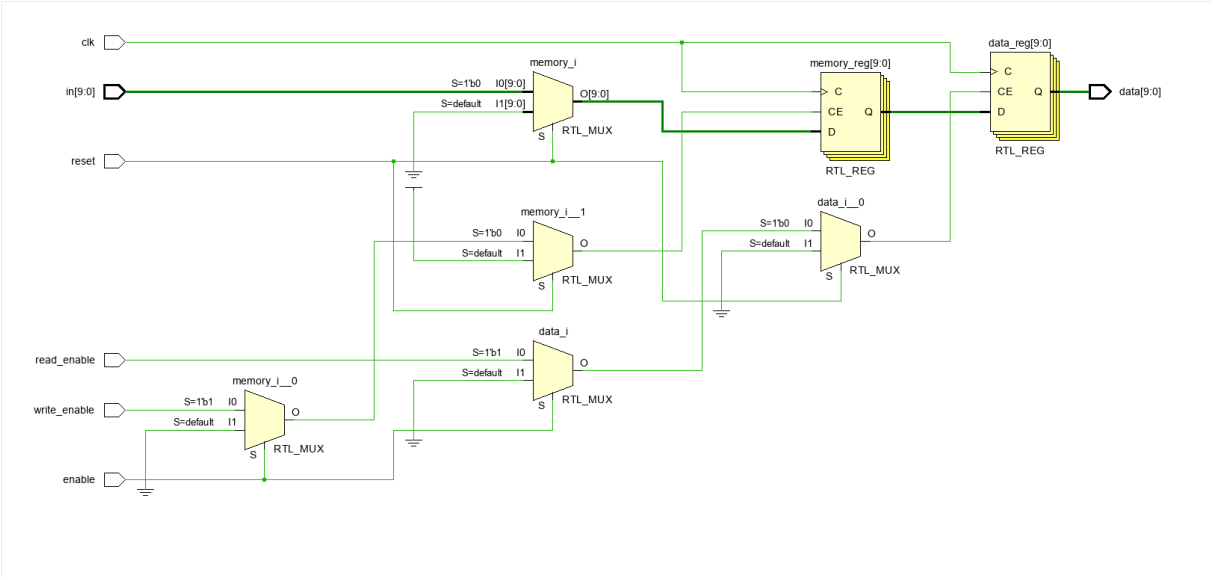
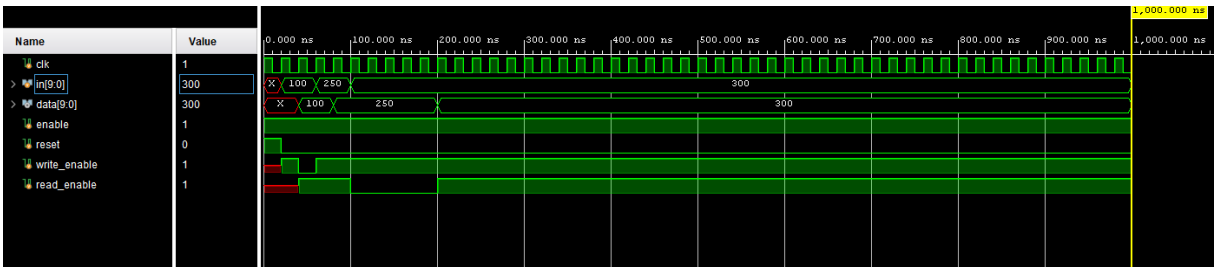
Question 1

This design is a parametrized register module that can hold the input data and give the stored data in rising edge of clock.

RTL Schematic , behavioral simulation, timing and utilization reports are given below



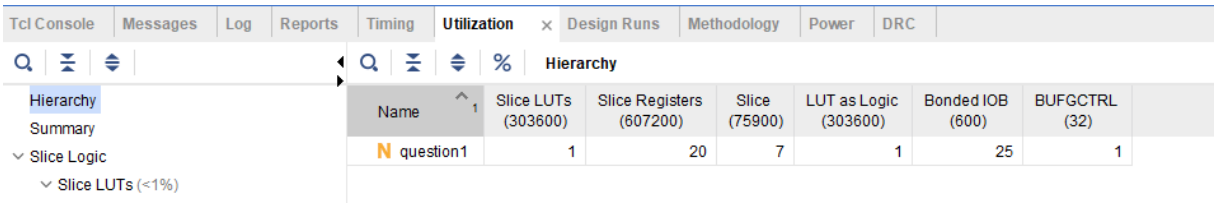


Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-2,716 ns	Worst Hold Slack (WHS):	0,081 ns	Worst Pulse Width Slack (WPWS):	3,100 ns
Total Negative Slack (TNS):	-25,485 ns	Total Hold Slack (THS):	0,000 ns	Total Pulse Width Negative Slack (TPWS):	0,000 ns
Number of Failing Endpoints:	10	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	60	Total Number of Endpoints:	60	Total Number of Endpoints:	21

Timing constraints are not met.

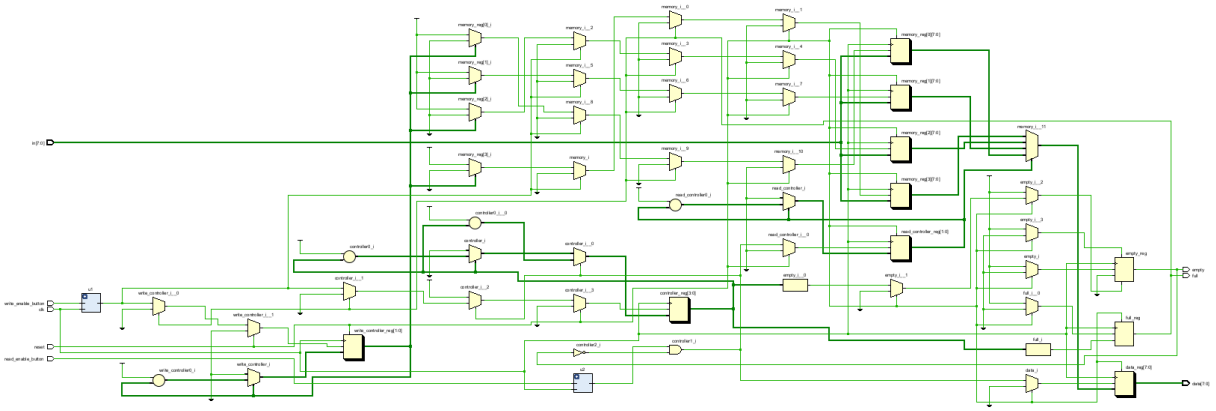
Fmax = 1/(7+2.716) = 102.92 MHz

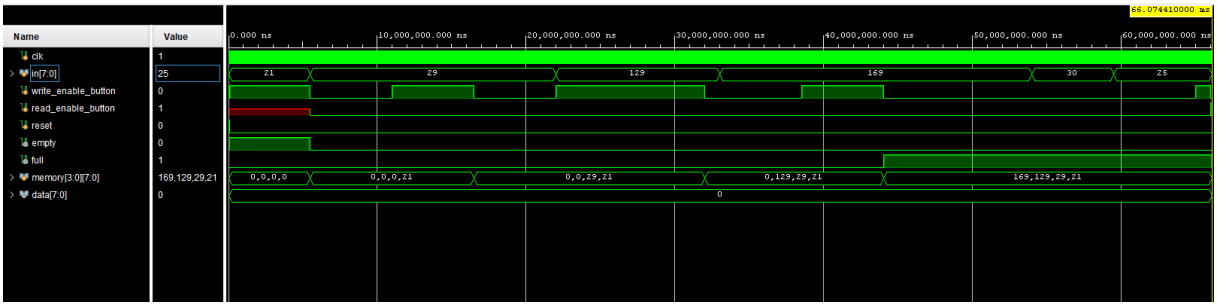


Question 2

This is a parametrized FIFO block. Parameter depth = 4, Parameter length =8. It gives the first input data of the all not readen datas when read is enable.

It has empty and full flags.





My clock's period is 6.250 ns. Here is the timing report.

Timing — **Setup** | Hold | Pulse Width

Worst Negative Slack (WNS):	-3.004 ns
Total Negative Slack (TNS):	-29.708 ns
Number of Failing Endpoints:	11
Total Number of Endpoints:	188

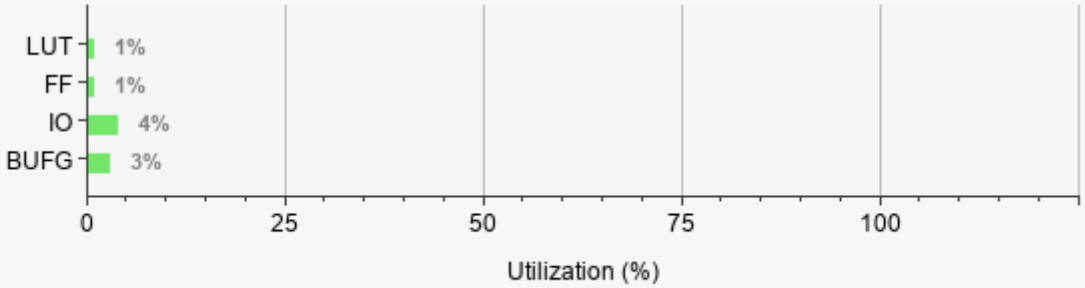
Implemented Timing Report

Fmax = (10^9)/(6.250-(-3.004) = 108 MHz

Utilization Report

Utilization Post-Synthesis | **Post-Implementation**

Graph | Table



Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	28	303600	0.01
FF	84	607200	0.01
IO	22	600	3.67
BUFG	1	32	3.13

PIN PLAN:

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	er Analo
clk	Input	PIN_AA16	4A	B4A_N0	PIN_AA16	2.5 V		12mA (default)			
data[7]	Output	PIN_W20	5A	B5A_N0	PIN_W20	2.5 V		12mA (default)	1 (default)		
data[6]	Output	PIN_Y19	4A	B4A_N0	PIN_Y19	2.5 V		12mA (default)	1 (default)		
data[5]	Output	PIN_W19	4A	B4A_N0	PIN_W19	2.5 V		12mA (default)	1 (default)		
data[4]	Output	PIN_W17	4A	B4A_N0	PIN_W17	2.5 V		12mA (default)	1 (default)		
data[3]	Output	PIN_V18	4A	B4A_N0	PIN_V18	2.5 V		12mA (default)	1 (default)		
data[2]	Output	PIN_V17	4A	B4A_N0	PIN_V17	2.5 V		12mA (default)	1 (default)		
data[1]	Output	PIN_W16	4A	B4A_N0	PIN_W16	2.5 V		12mA (default)	1 (default)		
data[0]	Output	PIN_V16	4A	B4A_N0	PIN_V16	2.5 V		12mA (default)	1 (default)		
empty	Output	PIN_Y21	5A	B5A_N0	PIN_Y21	2.5 V		12mA (default)	1 (default)		
full	Output	PIN_W21	5A	B5A_N0	PIN_W21	2.5 V		12mA (default)	1 (default)		
in[7]	Input	PIN_AC9	3A	B3A_N0	PIN_AC9	2.5 V		12mA (default)			
in[6]	Input	PIN_AE11	3A	B3A_N0	PIN_AE11	2.5 V		12mA (default)			
in[5]	Input	PIN_AD12	3A	B3A_N0	PIN_AD12	2.5 V		12mA (default)			
in[4]	Input	PIN_AD11	3A	B3A_N0	PIN_AD11	2.5 V		12mA (default)			
in[3]	Input	PIN_AF10	3A	B3A_N0	PIN_AF10	2.5 V		12mA (default)			
in[2]	Input	PIN_AF9	3A	B3A_N0	PIN_AF9	2.5 V		12mA (default)			
in[1]	Input	PIN_AC12	3A	B3A_N0	PIN_AC12	2.5 V		12mA (default)			
in[0]	Input	PIN_AB12	3A	B3A_N0	PIN_AB12	2.5 V		12mA (default)			
read_enable_button	Input	PIN_AA15	3B	B3B_N0	PIN_AA15	2.5 V		12mA (default)			
reset	Input	PIN_AE12	3A	B3A_N0	PIN_AE12	2.5 V		12mA (default)			
write_enable_button	Input	PIN_AA14	3B	B3B_N0	PIN_AA14	2.5 V		12mA (default)			
<<new node>>											