Assignment - 6

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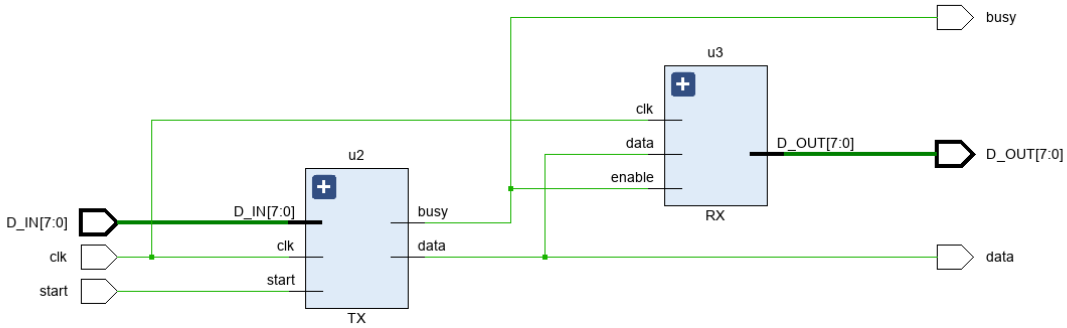
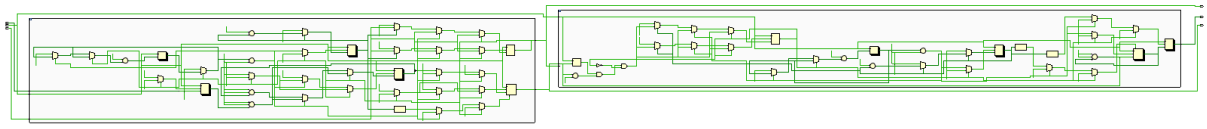
Question1

This circuit is a communication circuit which uses UART. It has receiver (RX) and transmitter (TX) modules. Input is 8 bit length data and output is as input.

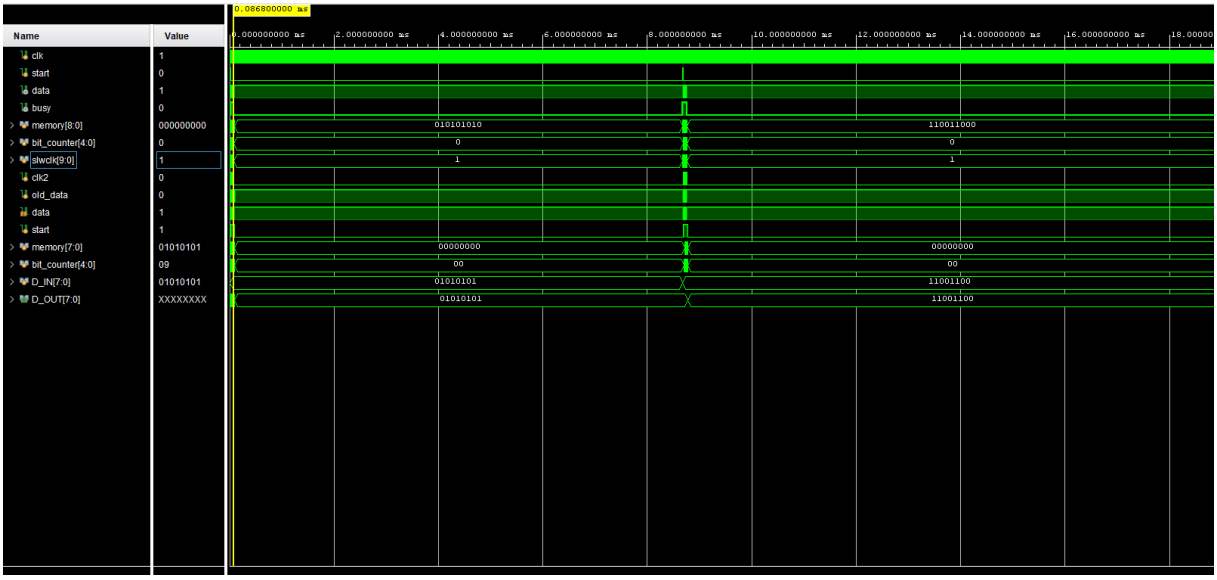
RTL Schematic:





Testbench results:

As it seems from testbench results, data transmitter and data reciever behaves correctly.



Timing Report:

Timing — **Setup** | Hold | Pulse Width

Worst Negative Slack (WNS):	-1.159 ns
Total Negative Slack (TNS):	-11.223 ns
Number of Failing Endpoints:	10
Total Number of Endpoints:	127

Implemented Timing Report

Utilization Reports:

Hierarchy

Name	Slice LUTs (303600)	Slice Registers (607200)	Slice (75900)	LUT as Logic (303600)	Bonded IOB (600)	BUFGCTRL (32)
question1	54	66	23	54	20	1
u2 (TX)	31	33	12	31	0	0
u3 (RX)	23	33	11	23	0	0

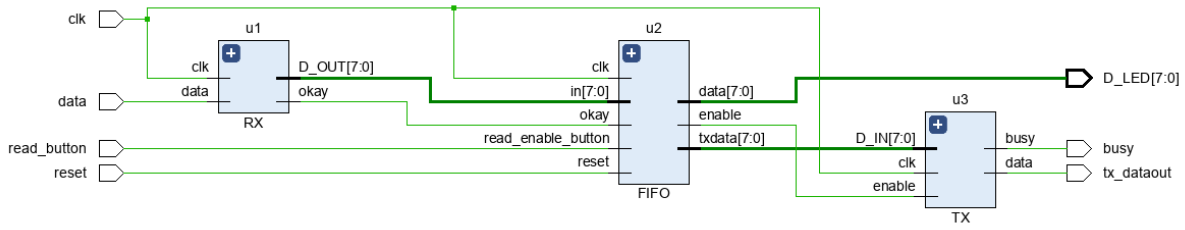
Name	Slice LUTs (303600)	Slice Registers (607200)	Slice (75900)	LUT as Logic (303600)	Bonded IOB (600)	BUFGCTRL (32)
question1	0.02%	0.01%	0.03%	0.02%	3.33%	3.13%
u2 (TX)	0.01%	<0.01%	0.02%	0.01%	0.00%	0.00%
u3 (RX)	<0.01%	<0.01%	0.01%	<0.01%	0.00%	0.00%

Question2:

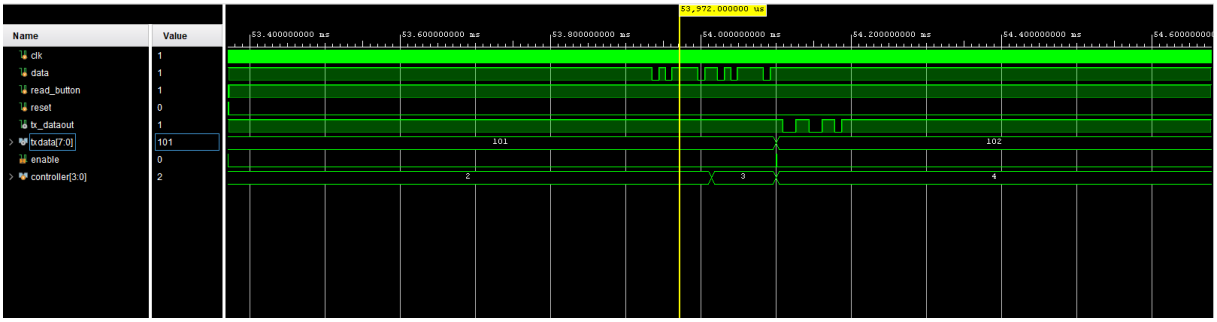
In this question, i connected my fifo and rx-tx modules together. Used RX to get data from keyboard and writed these datas to the FIFO. FIFO has a read button and i can read the ASCII code of the keyboard input from leds. When FIFO is empty, TX sends an ‘e’ signal to the computer. When FIFO is full, TX sends a ‘f’ signal to the computer.

I choosed 115.200

RTL Schematic



As it seems in the testbench, when FIFO reaches full, TX input changes to ‘f’ and sends just 1 “f” signal to the computer.



For T = 8ns, timing report:

Fmax = 109.122MHz

Timing — **Setup** | Hold | Pulse Width

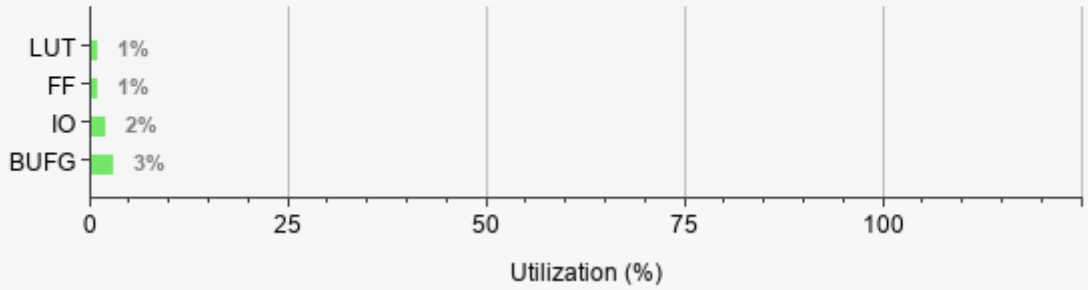
Worst Negative Slack (WNS):	-1.164 ns
Total Negative Slack (TNS):	-11.449 ns
Number of Failing Endpoints:	10
Total Number of Endpoints:	299

Implemented Timing Report

Utilization Report:

Utilization — Post-Synthesis | **Post-Implementation**

Graph | Table



Utilization — Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	101	303600	0.03
FF	157	607200	0.03
IO	14	600	2.33
BUFG	1	32	3.13

PIN PLAN

D_LED[7]	Output	PIN_W20	5A	B5A_N0	PIN_W20	2.5 V		12mA (default)	1 (default)
D_LED[6]	Output	PIN_Y19	4A	B4A_N0	PIN_Y19	2.5 V		12mA (default)	1 (default)
D_LED[5]	Output	PIN_W19	4A	B4A_N0	PIN_W19	2.5 V		12mA (default)	1 (default)
D_LED[4]	Output	PIN_W17	4A	B4A_N0	PIN_W17	2.5 V		12mA (default)	1 (default)
D_LED[3]	Output	PIN_V18	4A	B4A_N0	PIN_V18	2.5 V		12mA (default)	1 (default)
D_LED[2]	Output	PIN_V17	4A	B4A_N0	PIN_V17	2.5 V		12mA (default)	1 (default)
D_LED[1]	Output	PIN_W16	4A	B4A_N0	PIN_W16	2.5 V		12mA (default)	1 (default)
D_LED[0]	Output	PIN_V16	4A	B4A_N0	PIN_V16	2.5 V		12mA (default)	1 (default)
busy	Output				PIN_AJ19	2.5 V (default)		12mA (default)	1 (default)
clk	Input	PIN_AA16	4A	B4A_N0	PIN_AA16	2.5 V		12mA (default)	
data	Input	PIN_AE22	4A	B4A_N0	PIN_AE22	2.5 V		12mA (default)	
read_button	Input	PIN_AA14	3B	B3B_N0	PIN_AA14	2.5 V		12mA (default)	
reset	Input	PIN_AB12	3A	B3A_N0	PIN_AB12	2.5 V		12mA (default)	
tx_dataout	Output	PIN_AA20	4A	B4A_N0	PIN_AA20	2.5 V		12mA (default)	1 (default)
<<new node>>									