1 Embedded Systems

Which of the following is TRUE regarding embedded systems?
Select one alternative:

Power consumption is not an important design criterion for embedded systems as they are small.

An embedded system is designed for broad range of applications so that it can be used anywhere.

They are programmable by the end user.

Embedded systems often have fixed performance requirements.

2 ISA

Which of the following is NOT defined by an Instruction Set Architecture (ISA)?
Select one alternative:

Number of registers.

Instruction format (or encoding).

Cache size.

All of the above are defined by the ISA.

3 Stack usage

What is the Stack used for?
Select one alternative:

Stack can be used to pass parameters to a function.

Stack can be used to store local variables within a function.

Stack is used to save the callee-saved registers.

Stack is used for all of the above.

4 Assembly code debug

Find the bug in the following function call to “addNum” function in ARM Thumb-2 assembly code (the corresponding C code is also provided).
Note: In ARM Thumb-2, r15 is PC and r14 is LR (link register).

C Code:

```
int addNum (int a, int b) {
    return a+b;
}
main() {
```

Assembly Code:

```
addNum:    add    r0, r0, r1
           mov    r15, r14

main:      mov    r0, #5
```

```
    int x=5, y=10;                  mov   r1, #10
    addNum(x, y);                   bl    addNum
}
```

Select one alternative:

The parameters are not passed correctly to the “addNum” function.

The return address is not stored correctly, so the “addNum” function will never return to the main function.

Both of the above are bugs.

There is no bug in the function call.

5 Memory mapped I/O

Why is memory mapped I/O potentially a bigger problem on machines with 32-bit addresses than on machines with 64-bit addresses?

Select one alternative:

Machines with 64-bit addresses are faster.

64-bit machines transfer more data in a single cycle, therefore, the overhead is lower.

Machines with 32-bit addresses have smaller memory space, therefore, they lose higher fraction of their memory to I/O.

Memory mapped I/O is a bigger problem in machines with 64-bit addresses than in 32-bit address machines.

6 Direct Memory Access

What is the main benefit of DMA (Direct Memory Access)?

Select one alternative:

It allow CPU to replace polling with interrupts.

It relieves CPU from controlling the data transfer between memory and I/O devices.

It allows CPU to access caches and memory at a higher speed.

It allows CPU to access memory at a higher speed.

7 CPU Design

Which one of the following first three statements is FALSE regarding the advantages of a pipelined processor over single cycle processor design? If all three are true, choose the fourth option.

Select one alternative:

Pipelining reduces the cycle time, hence a pipelined processor can run at a higher frequency.

Pipelining reduces the clocks per instructions (CPI), hence execution time is also reduced.

Pipelining improves hardware utilization as fetch, decode, and execute hardware is used by different instructions simultaneously.

All of the above are true.

8 Memory Technologies

What is the main advantage of SRAM over DRAM?

Select one alternative:

SRAM is faster than DRAM.

SRAM is cheaper than DRAM.

SRAM is denser than DRAM. Therefore, it can store more bits in the same area.

None of the above.

9 Cache basics

How do caches help in improving CPU performance?

Select one alternative:

By keeping the most frequently used data in a fast memory.

By providing large and fast memory for all data.

By making the register file larger to hold more data in it.

All of above.

10 Direct mapped caches

Do direct mapped caches need a replacement policy? If yes, which replacement policy will provide higher hit rate: LRU or FIFO?

Select one alternative:

LRU (Least Recently Used) because it replaces a block that is not likely to be used in the near future.

FIFO (First In First Out) because it is easier to implement.

It depends on the cache access pattern; LRU is better for some access patterns and FIFO is better for others.

Direct mapped caches do not need a replacement policy.

11 Cache addressing

How many bits are needed for Tag, Index, and Byte Offset in an 8KB 2-way set associative cache with 8 byte block size, assuming 32-bit addresses.

Select one alternative:

Tag: 16, Index: 13, Byte Offset: 3.

Tag: 20, Index: 9, Byte Offset: 3.

Tag: 19, Index: 10, Byte Offset: 3.

None of the above.

12 Virtual memory

Which one of the following first three statements is FALSE regarding Virtual Memory (VM)? If all three are true, choose the fourth option.

Select one alternative:

VM allows physical memory to be smaller than the programs virtual address space.

VM allows multiple programs to share limited physical memory.

VM prevents Operating System to access memory used by the user programs.

All the above statements are true.

13 Memory addressing

Calculate the number of bits needed to represent "virtual page number", "page offset", and "physical page number" assuming 32-bit virtual addresses, 2KB page size, and 1GB of physical memory.

Select one alternative:

Not enough information to calculate the number of bits.

Virtual page number: 21 bits, Page Offset: 11 bits, Physical page number: 19 bits

Virtual page number: 21 bits, Page Offset: 11 bits, Physical page number: 21 bits

None of the above.

14 Pointers in C

What is the correct implementation of the following function that sets the value of the given variable “number” to the square of its original value?

```
void square(int *number)
{
// implementation here
}
```

Select one alternative:

*number *= *number;

number *= number;

*number *= &number;

*number *= number;

15 **Structures in C**

What is the correct C syntax to access the field “value” in struct “node” through the variable “myList”?

```
struct node {
   int value;
   int count;
};
struct list {
   struct node *listHead;
   int size;
};
struct list myList;
```

Select one alternative:

myList.listHead.value

myList->listHead.value

myList.listHead->value

myList ->listHead->value

16 **Bit operations in C**

What is the value of variable 'a' after executing the following code sequence?
Note: ^ denotes XOR operation.

```
unsigned char a = 0x00;
a ^= 0x01;
if( a & 0xF ) {
   a |= 0x10;
}
```

Select one alternative:

0x00

0x10

0x01

0x11

17 Testing

You have a program that allocates and deallocates memory. You suspect that there is a memory leak. Which kind of testing will tell you if there is indeed a memory leak?

Select one alternative:

- Static analysis
- Run-time analysis
- Code coverage testing
- None of the above.

18 Datatypes in C

You have an array of 180 elements. Which of the following data type can be used to store an index to the array using the minimum space in memory?

Select one alternative:

- uint16_t
- int16_t
- int8_t
- uint8_t

19 Compilation

Consider the following complete file "foo.c"

```
// File start
#include<stdio.h>
int foo_bar(int x);

int main(int argc, char *argv[]) {
   int i=0, b=0;
   b = foo_bar(i);
   return b;
}
//File end
```

On the command line, when the user types "gcc –o foo foo.c" to compile foo.c and generate the binary executable foo, which error message, if any, is generated?

Select one alternative:

- The compiler issues an error, because the symbol foo_bar is not defined.
- The linker issues an error, because the symbol foo_bar is not defined.
- The loader issues an error, because the symbol foo_bar is not defined.
- The symbol foo_bar is defined and there is no error.

20 Compiler optimizations

Which one of the following first three statements is FALSE about function lining? If all three are false, choose the fourth option.

Select one alternative:

Function inlining reduces the size of the executable file.

Function inlining increases function call overhead (cost of passing parameters and results etc.)

Function inlining requires loop unrolling.

All of the above statements are false.

21 Register allocation (Compiler)

The following C code needs to be compiled for a RISC processor with a load-store architecture. In this architecture, an instruction cannot use the same register as both a source and a destination operand. Assume that a variable is loaded into a register the first time it is used in the code and written back to memory after the last time it is used in the code. What is the minimum number of registers needed for this code?

```
w = a + b;
x = c + d;
y = x + e;
z = w -  x;
```

Select one alternative:

2

3

4

5

22 Operating Systems

Which one of the following statements is FALSE regarding process state transition (in Operating System)?

Select one alternative:

A process can go from “ready” state to “running” state.

A process can never go from “blocked” to “running” state.

A process can never go from “running” to “ready” state.

A process can go from “blocked” to “ready” state.

23 Operating Systems (IPC)

Which of the following is NOT a valid mechanism for inter process communication?
Select one alternative:

- Signals.
- Message passing.
- Shared memory.
- All of the above are valid mechanisms for inter process communication.

24 Energy and Power

What does a larger battery provide?
Select one alternative:

- Ability to use more energy
- Ability to use more power.
- Higher performance.
- All of above.

25 Clock gating

What is the primary goal of Clock Gating?
Select one alternative:

- Reduce static power consumption
- Send the clock signal to every gate on the chip.
- Provide higher performance.
- Reduce dynamic power consumption.