CSE435 Introduction to EDA & Testing - Spring 2022

Homework Assignment #5

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1. (20%) A circuit has the truth table of Table 1. When there is a fault (faults) on the circuit, the faulty truth table becomes Table 2. Try to derive tests to detect the fault (faults).

CD \ AB	00	01	11	10
00	1			
01		1	1	
11				1
10			1	1

Table 1

CD \ AB	00	01	11	10
00				
01		1	1	
11				
10	1		1	1

Table 2

Solution: Compare two truth tables, we can tell the circuit has stuck-at-0 fault at output when input {A, B, C, D} equals {0, 0, 0, 0} or {1, 0, 1, 1}. The circuit also has stuck-at-1 fault at output when the input equals {0, 0, 1, 0}.

Answers: {{0, 0, 0, 0}, {1, 0, 1, 1}, {0, 0, 1, 0}}

2. (80%) Generate a test for the fault f-sa1 in Figure 1 by the following FOUR methods. Be sure to give the **key steps to show the features of every algorithm**, and also **draw the decision trees** for each case.
   (a) (20%) Use the **Boolean difference method** to derive all the test patterns to detect the fault f-sa1.
   (b) (20%) Generate a test for the fault f-sa1 by using **D-algorithm**.
   (c) (20%) Generate a test for the fault f-sa1 by using **9-V Algorithm**.
   (d) (20%) Generate a test for the fault f-sa1 by using **PODEM algorithm**.

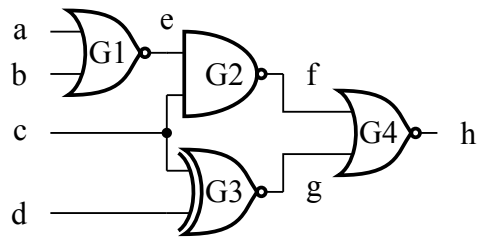

Figure 1