CSE435 Introduction to EDA & Testing - Spring 2022

Homework Assignment #2

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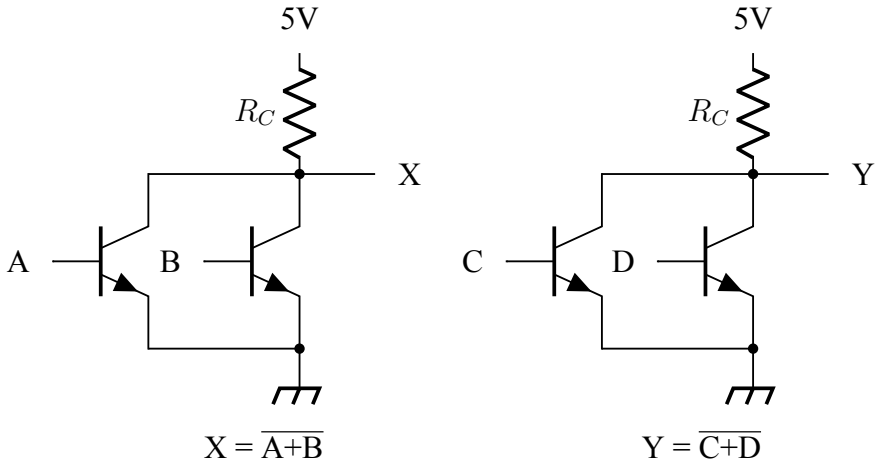
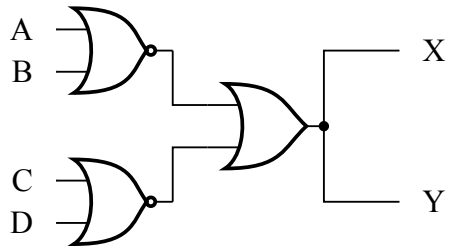
1. (25%) For ECL NOR gates as shown, if the outputs of two NOR gates short together, analyze electrically the resultant output behavior (wired AND? wired OR). Explain why?



Solution: In emitter-coupled logic (ECL) circuits, the bridging fault leads to wired OR behavior. The resultant logic relation would become X = Y = $\overline{A+B}$ + $\overline{C+D}$. The equivalent logic circuit is shown below.



2. (25%) In Problem 1, if there is a defect that the value of R_C of the gate X = $\overline{A+B}$ is increased by 100 times. If the patterns can be applied to A, B and the output can be observed at X, derive a test pattern to detect this defect.

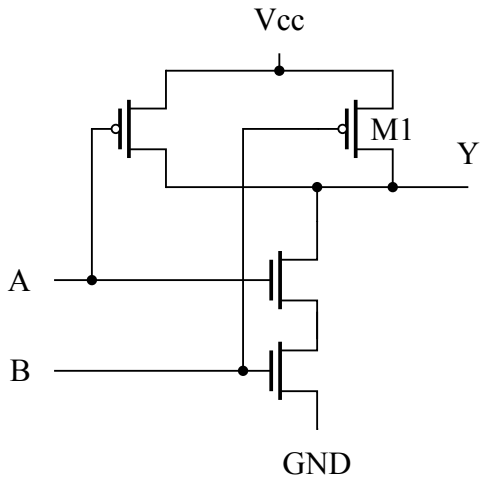
Solution: When R_C is abnormally high, the output would become slow to charge, which leads to the gate-delay fault. The time required to charge the capacitor τ, which can be

formulated as $\tau = RC$, where R is the resistance, and C is the capacitance, thus $\tau \propto R$. The delay is increased by 100 times as well.

To test the charging delay fault, we should first clear the output by setting (A, B) to (0, 1), (1, 0), or (1, 1). At the second time frame, we set (A, B) to (0, 0) to charge the circuit and observe the output to test if it produces significant delay.

Answer: At time frame 1, (A, B) = (0, 1), (1, 0), or (1, 1). At time frame 2, (A, B) = (0, 0).

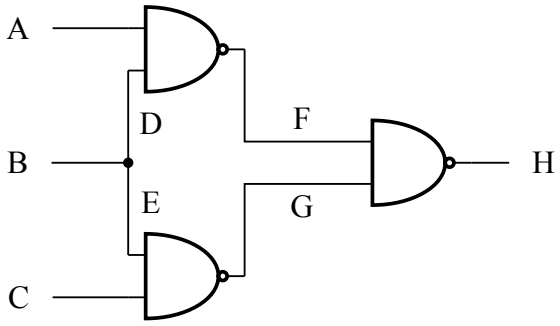
3. (25%) Derive test patterns to detect the transistor M1 stuck-open fault in the following NAND gate.



Solution: The stuck-open fault in the charging unit (pull-up, PU) makes the output never charged to 1 after discharged to 0. For example, at the first time frame, we discharge the circuit by setting (A, B) to (1, 1). Then we switch B to 0. If the transistor M1 functioned normally, it should charge the output since the ground wire is cut-off by an NMOS. If 0 is instead observed at Y, then there's a stuck-open fault at M1.

Answer: At time frame 1, (A, B) = (1, 1). At time frame 2, (A, B) = (1, 0).

4. (25%) Try to derive test pattern for the fault F(sa0). For the derived pattern, try to identify what other multiple faults of multipliticity = 2 can be detected.



Solution: In order to find the stuck-at-0 fault at F, G must be non-dominant, which is 1, and F must be 1. G's value of 1 indicates $\overline{A \cdot B} = 1$; F's value of 1 indicates $\overline{B \cdot C} = 1$. (A, B, C) can be either ($\times$, 0, $\times$) or (0, 1, 0), where $\times$ denotes the don't-care condition.

F(sa0) is equivalent to G(sa0) and H(sa1). With multiplicity = 2, the identical test pattern can detect

- F(sa0) and G(sa0)
- F(sa0) and H(sa1)
- G(sa0) and H(sa1)