國 立 中 山 大 學
資 訊 工 程 學 系 所

Introduction to EDA&Testing – Fall, 2022

Homework Assignment #5
Due Date: April 27, 2022

Please note: MUST SHOW YOUR SOLUTION PROCESS.
Without detailed solution process, only answers are NOT acceptable.

1. (20%) A circuit has the truth table of Table 1a. When there is a fault (faults) on the circuit, the faulty truth table becomes Table 1b. Try to derive tests to detect the fault (faults).

CD \ AB	00	01	11	10
00	1			
01		1	1	
11				1
10			1	1

Table 1a

CD \ AB	00	01	11	10
00				
01		1	1	
11				
10	1		1	1

Table 1b

2. (80%) Generate a test for the fault f-sa1 in Figure 1 by the following FOUR methods. Be sure to give the **key steps to show the features of every algorithm**, and also **draw the decision trees** for each case.

   (a) (20%) Use the **Boolean difference method** to derive all the test patterns to detect the fault f-sa1,

   (b) (20%) Generate a test for the fault f-sa1 by using **D-algorithm**,

   (c) (20%) Generate a test for the fault f-sa1 by using **9-V Algorithm,**

   (d) (20%) Generate a test for the fault f-sa1 by using **PODEM algorithm**, respectively.

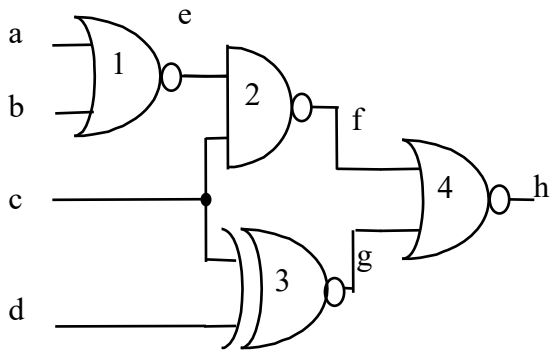

Figure 1