## CSE435 Introduction to EDA & Testing - Spring 2022

## Homework Assignment #1 Shao-Hsuan Chu - B073040018

1. (25%) If the yield of good dice is 90%, and we want a defect level not to exceed 0.1%, what level of testing in terms of fault coverage must be achieved?

**Solution:** The defect level **DL** can be obtained by **DL** =  $1 - \mathbf{Y}^{1-\mathbf{T}}$ , where **Y** is the yield, indicating the manufacturing capability, and **T** is the fault coverage, indicating the testing capability.

$$0.001 \ge 1 - 0.9^{1-T}$$

$$0.9^{1-T} \ge 1 - 0.001$$

$$0.9^{1-T} \ge 0.999$$

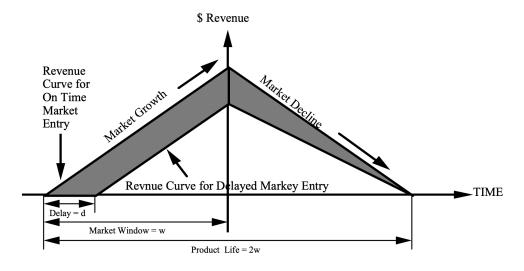
$$\log_{0.9} 0.9^{1-T} \le \log_{0.9} 0.999$$

$$1 - \mathbf{T} \le 0.0095$$

$$\mathbf{T} \ge 0.9905 = 99.05\%$$

**Answer:** The fault coverage Y must be at least 99.05%

2. (50%) Given the market entry time verse revenue curves as shown in Figure 1, fill in the following formula



(a) (25%) Lost Revenue = Total Expected Revenue \* [ ]. The answer should be in term of d and w. d is the delay entry, 2w is the product life. The two market growth rates are the same.

**Solution:** The Lost Revenue **LR** equals to the absolute difference between the Total Expected Revenue **TER** and the Total Actual Revenue **TAR**. Denote the market growth rates as r, the Lost Revenue can be obtained by

$$\begin{aligned} \mathbf{TER} &= \frac{1}{2}(2w)(w)r = (w^2)r \\ \mathbf{TAR} &= \frac{1}{2}(2w-d)(w-d)r = (w^2 - \frac{3}{2}wd + \frac{1}{2}d^2)r \\ \mathbf{LR} &= \mathbf{TER} - \mathbf{TAR} \\ \mathbf{LR} &= (\frac{3}{2}wd - \frac{1}{2}d^2)r \\ \mathbf{LR} &= \mathbf{TER} \times \frac{(\frac{3}{2}wd - \frac{1}{2}d^2)r}{\mathbf{TER}} \\ \mathbf{LR} &= \mathbf{TER} \times \frac{\frac{3}{2}wd - \frac{1}{2}d^2}{w^2} \end{aligned}$$

**Answer:**  $(\frac{3}{2}wd - \frac{1}{2}d^2)/w^2$ 

(b) (25%) Given a product with total expected revenue \$100M, product life is 20 months. What is the revenue loss due to the one month late to the market?

**Solution:** Substitute the given algebras inside the formula above.

$$2w = 20$$

$$w = 10$$

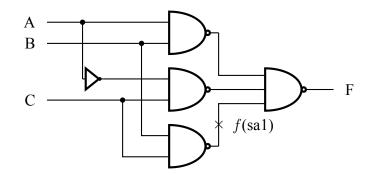
$$d = 1$$

$$\mathbf{LR} = 100\mathbf{M} \times (\frac{3}{2} \times 10 \times 1 - \frac{1}{2}1^2)/10^2$$

$$\mathbf{LR} = 14.5\mathbf{M}$$

Answer: 14.5M

3. (25%) Try to derive the test pattern for the fault f (sa1). Explain your result. Try to simplify the circuit.



**Solution:** In order to find the stuck-at-1 fault, the first and second (top-down order) inputs of the final **NAND** gate must be non-dominant, which is 1, and the third input must be 0. The third input's value of 0 indicates  $\overline{B\cdot C}=0$  and thus B=C=1. We then need A=0 to make the first input 1. However, we also want A=1 to make the second input 1, which contradicts the requirement above. As a result, this fault is not discoverable, i.e., a redundant fault.

Answer: The test pattern does not exist.

Simplified circuit with stuck-at-1 fault:

