CME 433 Lab 3

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1. Before implement combinational logic
   Fmax = 79.92 MHz
   Total of logic elements: 678
   Registers: 50

After implement combinational logic

Slow ROM
   Fmax = 17.94 MHz
   Total of logic elements: 1192
   Registers: 50
   Critical path: instruction decoder
   Simulation time = ~7us

Slow ROM Pipe1
   Fmax = 18.49 MHz
   Total of logic elements : 1202
   Register: 50
   Critical path: program memory
   Simulation time = ~11 us

Slow ROM pipe 2
   Fmax= 20.55MHz
   Total of logic elements: 1201
   Register: 51
   Critical path: Instruction decoder
   Simulation time = ~ 13us

Microprocessor after implement 2 combinational logics

	Fmax	Restricted Fmax	Clock Name
1	17.94 MHz	17.94 MHz	clk

Fmax

Flow Summary

<<Filter>>

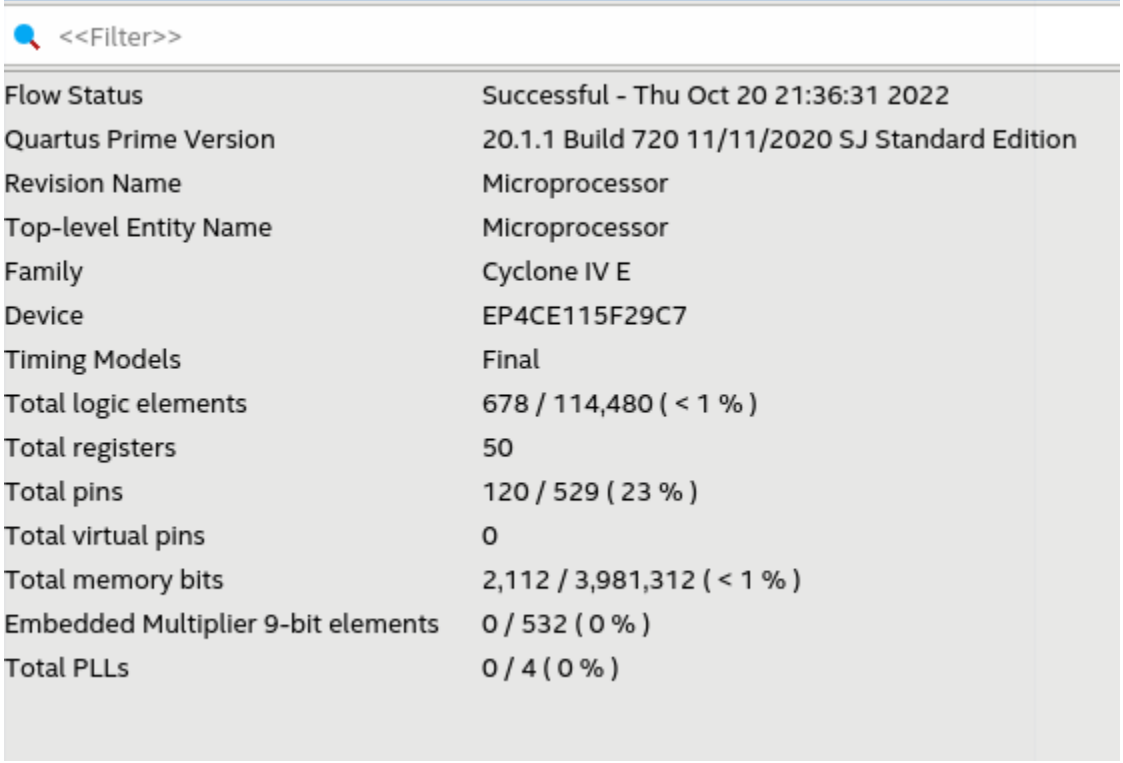
Flow Status	Successful - Thu Oct 20 21:44:48 2022
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Standard Edition
Revision Name	Microprocessor
Top-level Entity Name	Microprocessor
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	1,192 / 114,480 (1 %)
Total registers	50
Total pins	128 / 529 (24 %)
Total virtual pins	0
Total memory bits	2,112 / 3,981,312 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Synthesis data

ck	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
75	program_memory:prog_me...1a0~porta_address_reg0	instruction_decoder:instr_decoder|ir[7]	clk	clk	0.500	-0.482	27.392
10	program_memory:prog_me...1a0~porta_address_reg0	instruction_decoder:instr_decoder|ir[6]	clk	clk	0.500	-0.482	27.227
56	program_memory:prog_me...1a0~porta_address_reg0	instruction_decoder:instr_decoder|ir[5]	clk	clk	0.500	-0.482	26.983
23	program_memory:prog_me...1a0~porta_address_reg0	instruction_decoder:instr_decoder|ir[4]	clk	clk	0.500	-0.479	26.743
44	program_memory:prog_me...1a0~porta_address_reg0	instruction_decoder:instr_decoder|LS_nibble_of_ir[3]	clk	clk	0.500	-0.478	26.665
27	program_memory:prog_me...1a0~porta_address_reg0	instruction_decoder:instr_decoder|LS_nibble_of_ir[1]	clk	clk	0.500	-0.097	26.829
07	program_memory:prog_me...1a0~porta_address_reg0	instruction_decoder:instr_decoder|LS_nibble_of_ir[0]	clk	clk	0.500	-0.071	26.635
50	instruction_decoder:instr_decoder|ir[4]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.331	26.811
34	program_memory:prog_me...1a0~porta_address_reg0	instruction_decoder:instr_decoder|LS_nibble_of_ir[2]	clk	clk	0.500	-0.113	26.270
00	program_sequencer:prog_sequencer|pc[1]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.344	26.474
98	program_sequencer:prog_sequencer|pc[3]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.344	26.472
38	instruction_decoder:instr_decoder|ir[7]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.334	26.452
24	program_sequencer:prog_sequencer|pc[0]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.344	26.398
03	computational_unit:comp_unit|r_eq_0	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	-0.089	25.944
02	instruction_decoder:instr_decoder|ir[5]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.334	26.356
09	program_sequencer:prog_sequencer|pc[2]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.344	26.283
56	instruction_decoder:instr_decoder|ir[6]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.334	26.230
74	sync_reset	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.343	26.147

Critical path of slow ROM

Microprocessor before implement 2 combinational logics



<<Filter>>	
Flow Status	Successful - Thu Oct 20 21:36:31 2022
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Standard Edition
Revision Name	Microprocessor
Top-level Entity Name	Microprocessor
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	678 / 114,480 (< 1 %)
Total registers	50
Total pins	120 / 529 (23 %)
Total virtual pins	0
Total memory bits	2,112 / 3,981,312 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Synthesis data

	Fmax	Restricted Fmax	Clock Name
1	79.92 MHz	79.92 MHz	clk

Fmax clock

Microprocessor after implement pipe1

Flow Summary

<<Filter>>

Flow Status	Successful - Fri Oct 21 08:52:29 2022
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Standard Edition
Revision Name	Microprocessor
Top-level Entity Name	Microprocessor
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	1,202 / 114,480 (1 %)
Total registers	50
Total pins	120 / 529 (23 %)
Total virtual pins	0
Total memory bits	2,112 / 3,981,312 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Synthesis data

<<Filter>>

	Fmax	Restricted Fmax	Clock Name
1	18.49 MHz	18.49 MHz	clk

Fmax

w 1200mV 0C Model Setup: 'clk'

<<Filter>>

From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
instruction_decoder:instr_decoder|ir[5]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.329	27.402
instruction_decoder:instr_decoder|ir[7]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.329	27.380
instruction_decoder:instr_decoder|ir[4]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.329	27.219
instruction_decoder:instr_decoder|ir[6]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.329	27.153
data_pipe[4]	instruction_decoder:instr_decoder|ir[4]	clk	clk	1.000	-0.316	26.967
data_pipe[3]	instruction_decoder:instr_decoder|LS_nibble_of_ir[3]	clk	clk	1.000	-0.316	26.778
program_sequencer:prog_sequencer|pc[0]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.328	26.926
program_sequencer:prog_sequencer|pc[1]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.328	26.844
data_pipe[0]	instruction_decoder:instr_decoder|LS_nibble_of_ir[0]	clk	clk	1.000	0.067	27.046
program_sequencer:prog_sequencer|pc[2]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.328	26.811
data_pipe[5]	instruction_decoder:instr_decoder|ir[5]	clk	clk	1.000	-0.316	26.516
computational_unit:comp_unit|r_eq_0	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.329	26.688
data_pipe[2]	instruction_decoder:instr_decoder|LS_nibble_of_ir[2]	clk	clk	1.000	-0.316	26.484
program_sequencer:prog_sequencer|pc[3]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.328	26.519
data_pipe[1]	instruction_decoder:instr_decoder|LS_nibble_of_ir[1]	clk	clk	1.000	0.067	26.724
sync_reset	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.329	26.437
program_sequencer:prog_sequencer|pc[4]	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.328	26.361
data_pipe[6]	instruction_decoder:instr_decoder|ir[6]	clk	clk	1.000	-0.316	26.108

Critical path

Microprocessor after implement pipe 2

Simulation result

Flow Summary

<<Filter>>

Flow Status	Successful - Fri Oct 21 09:31:18 2022
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Standard Edition
Revision Name	Microprocessor
Top-level Entity Name	Microprocessor
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	1,201 / 114,480 (1 %)
Total registers	51
Total pins	120 / 529 (23 %)
Total virtual pins	0
Total memory bits	2,112 / 3,981,312 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Synthesis data

<<Filter>>

	Fmax	Restricted Fmax	Clock Name
1	20.55 MHz	20.55 MHz	clk

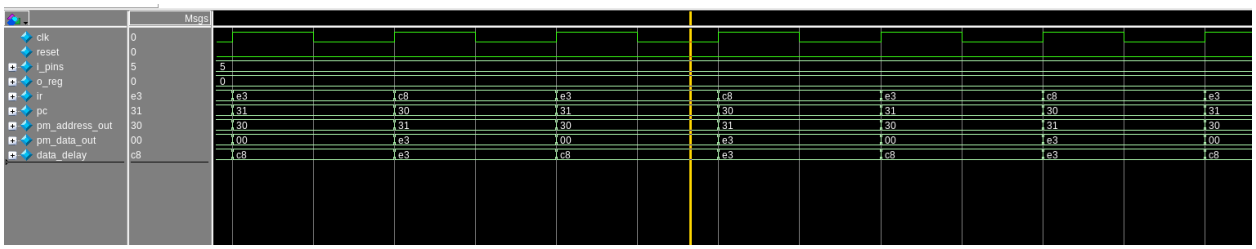
Fmax

	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
	instruction_decoder:instr_decoder|ir[7]	clk	clk	1.000	-0.323	26.965
	instruction_decoder:instr_decoder|ir[6]	clk	clk	1.000	-0.317	26.768
	instruction_decoder:instr_decoder|ir[5]	clk	clk	1.000	-0.317	26.371
	instruction_decoder:instr_decoder|LS_nibble_of_ir[1]	clk	clk	1.000	-0.317	26.264
	instruction_decoder:instr_decoder|LS_nibble_of_ir[3]	clk	clk	1.000	-0.323	26.104
	instruction_decoder:instr_decoder|ir[4]	clk	clk	1.000	-0.317	26.077
	instruction_decoder:instr_decoder|LS_nibble_of_ir[0]	clk	clk	1.000	-0.323	25.188
	instruction_decoder:instr_decoder|LS_nibble_of_ir[2]	clk	clk	1.000	-0.323	24.934
	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	-0.048	24.311
	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.330	24.678
	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	-0.056	24.228
	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	-0.063	24.118
	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	-0.089	23.916
	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.331	24.303
	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	0.330	24.252
	program_memory:prog_mem|altsyncram:...ted|ram_block1a0~porta_address_reg0	clk	clk	0.500	-0.076	23.841
]	computational_unit:comp_unit|r_eq_0	clk	clk	1.000	-0.035	9.981
]	computational_unit:comp_unit|r[2]	clk	clk	1.000	-0.035	9.358

Critical path

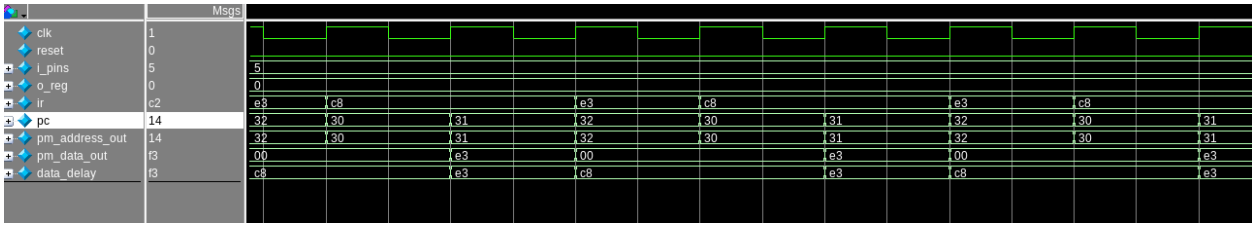
2. Trade off of the hardware utilization: Implementation of pipeline increases maximum frequency overtime,also means more delay time. Even though adding more hardware or implementing more logic gates will increase the function of hardware, it will also slow down microprocessors by increasing maximum frequency.

3.
Disadvantage:
Implementing pipelines increases the complexity of hardware design. Instruction latency will be increased in pipelined processors. In addition, it is difficult to predict the throughput of a pipelined processor. The more pipeline, the worsen hazard for branching instructions.
Advantage:
Increase the number of instructions executed simultaneously. It will also increase performance of the CPU, making ALU faster.
4.
Pipeline 1 simulation wave



Ir = c8 stay for 1 clock cycle

Pipeline 2 simulation waveform



Ir = c8 stay for 2 clock cycle

Suspending the microprocessor:

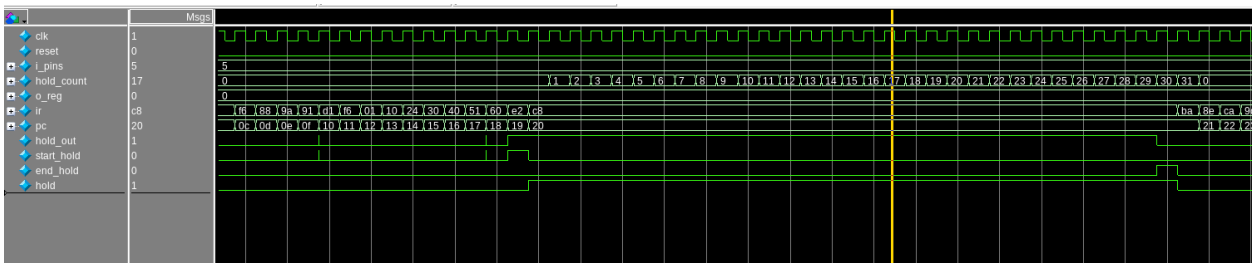
1.First the waveform of hold_count shows proper count from 0 to 31 (32 bits).

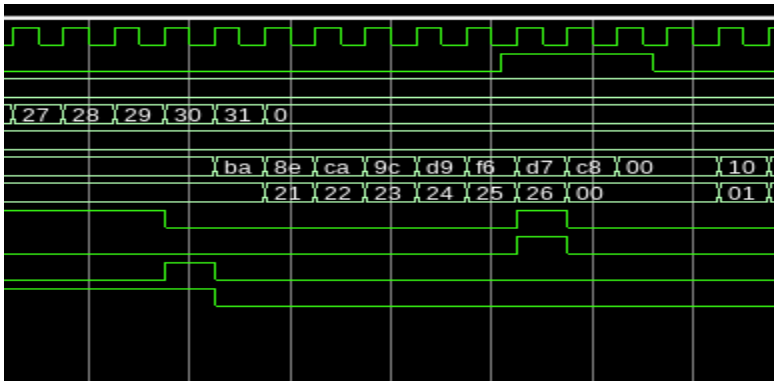
Second, the wave form starts to hold when pc = 19 and ir =e2(po[7:5] != pm[7:5])

E2 = 1110 0010

19 = 0001 1001

2





3 The cache size should be 32 x 8 bits because it counts 32 and data is 8 bits.