CME 433
Lab 4

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Single Line Cache

1. There are some advantage and disadvantage using cache:
    a. Advantage of cache:
        i. Store all data and instructions frequently used by the CPU, therefore increasing the performance of the CPU
        ii. Data access time of the cache memory is less than primary memory.
    b. Disadvantage of cache:
        i. More expensive than primary memory and secondary memory.
        ii. Just store data temporarily.
        iii. Consistency problems because data in the cache may be different than real data from primary memory.
        iv. All the data stored will be destroyed when the computer is turned off.
2. The disadvantages with the implementation: The reason to implement cache is to decrease data access time. However after suspending the whole microprocessor to reload the cache, we don't see that benefit we describe about. It slows down the microprocessor.
3. To overcome these disadvantages, we should not suspend the whole microprocessor, instead we should suspend the partial part which requires memory.
4. The whole stimulation required 657 us when i reach e7

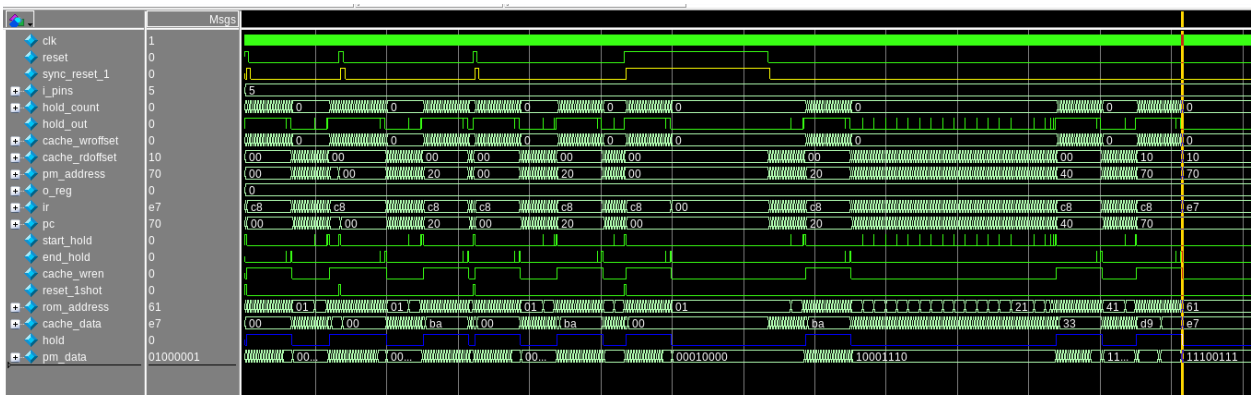

Figure 1: Single Line Cache Entire simulation

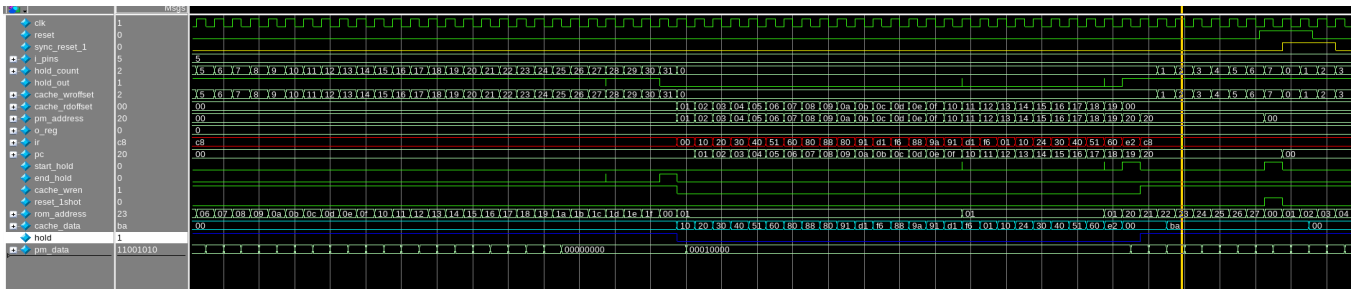

Figure 2: Single Line Cache Detail about suspending microprocessor

Cache_data was ready for reading from cache memory when cache_wren disable.

Cache_data was written into cache memory when the microprocessor was suspended and cache_wren enabled.

Microprocessor was suspended for a 32 clock cycle. During that time, rom_address was written into cache memory.

Cache Memory Benefits

1.
Program execution time without cache: 1142.5 us
Program execution time with cache: 845.5 us
Because a program with cache has execution time faster, it is better. The trade off is that when a program executes with cache, it is required to implement suspending microprocessors for every 128 clock cycle to write data into cache. At that time a microprocessor can not do anything until instructions have been written into cache memory.
2.
Programs containing loops would make the single-line cache version of the microprocessor to perform better than the one without any cache because the microprocessor is only required to load the cache once and it can read data from the cache as many times as required. On the other hand, sequential statements would favor the opposite version because new instructions are constantly required. The downside is that it will slowing down the execution time overall.
3. Snap shots

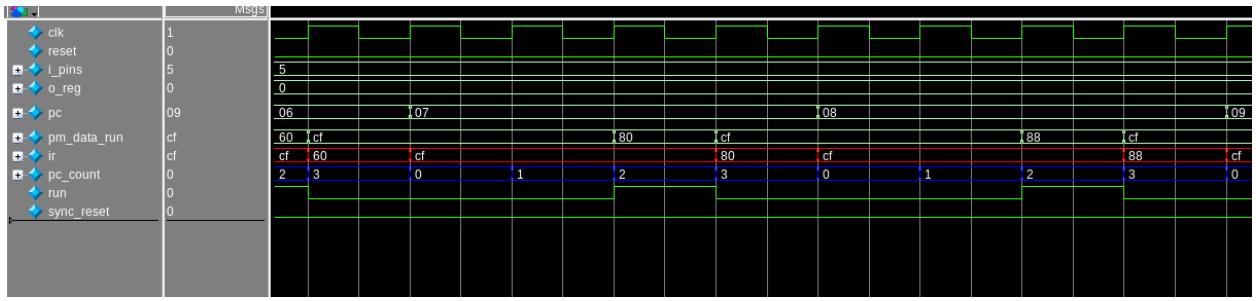

Figure 3: Cache Memory Benefits - rom_more_clk

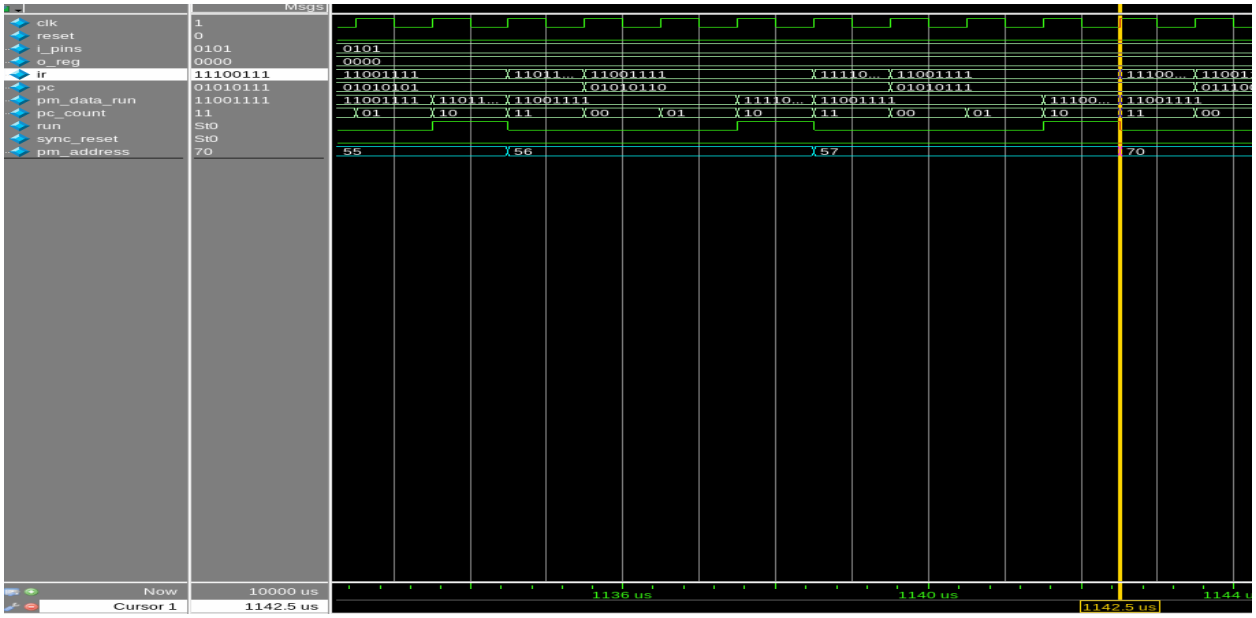

Figure 4: rom_more_clk execute time

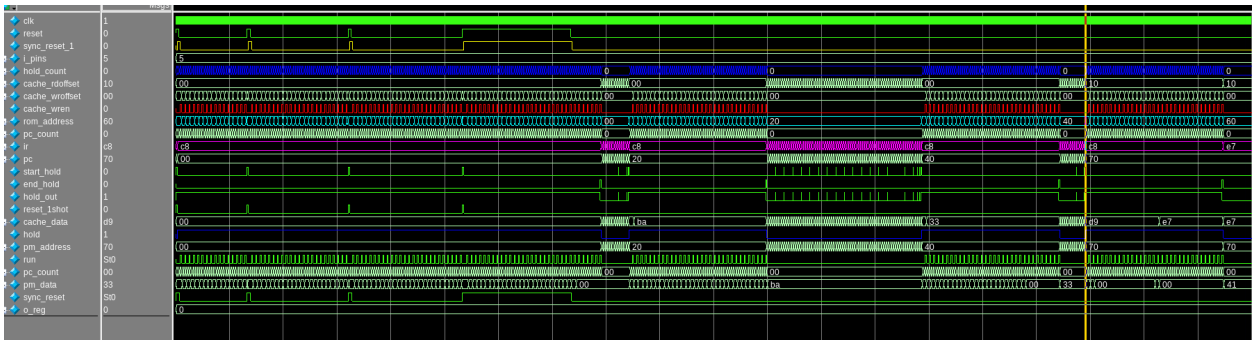

Figure 5: rom_more_clk_cache whole simulation

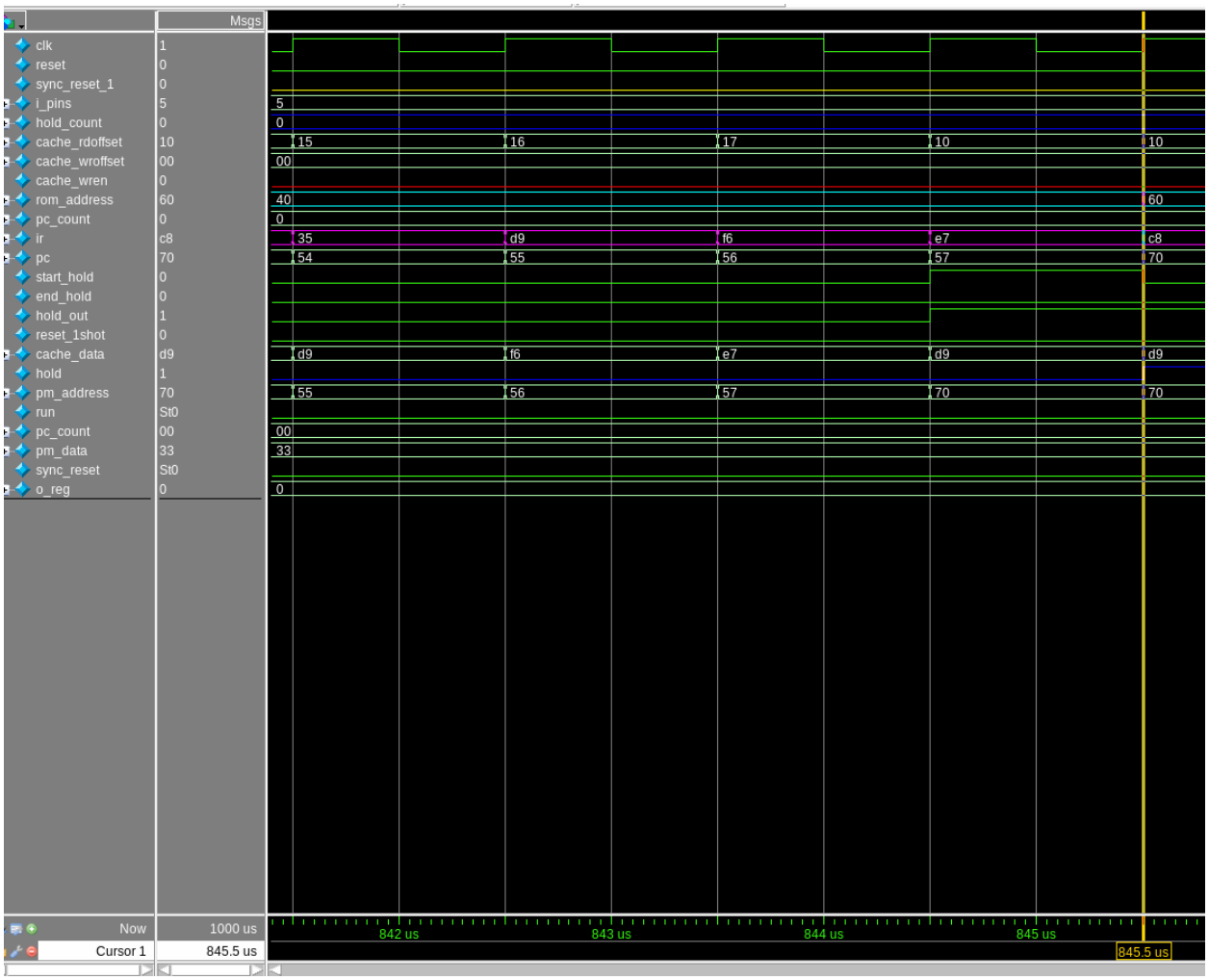

Figure 6: time for execute instruction at pm_address = 8'H70 for the first time

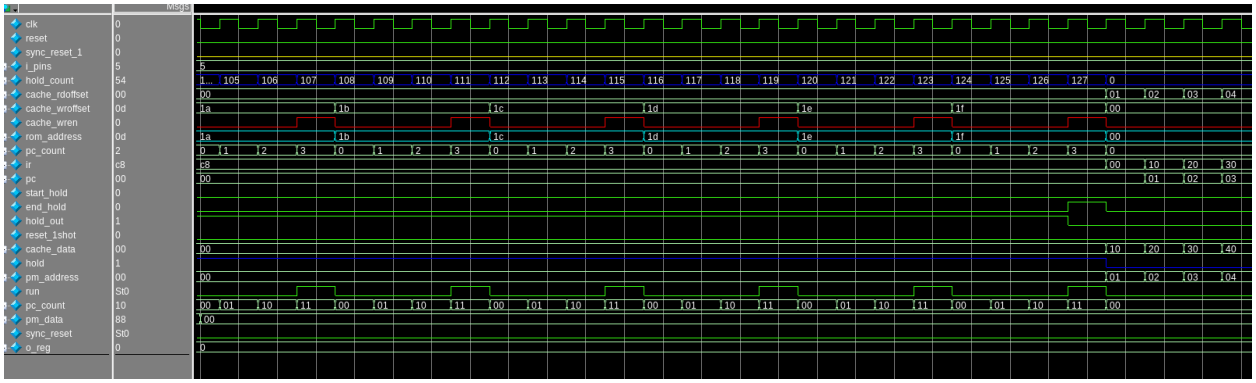

Figure 7 : rom_more_clk_cache, hold period 32 instructions was written into cache

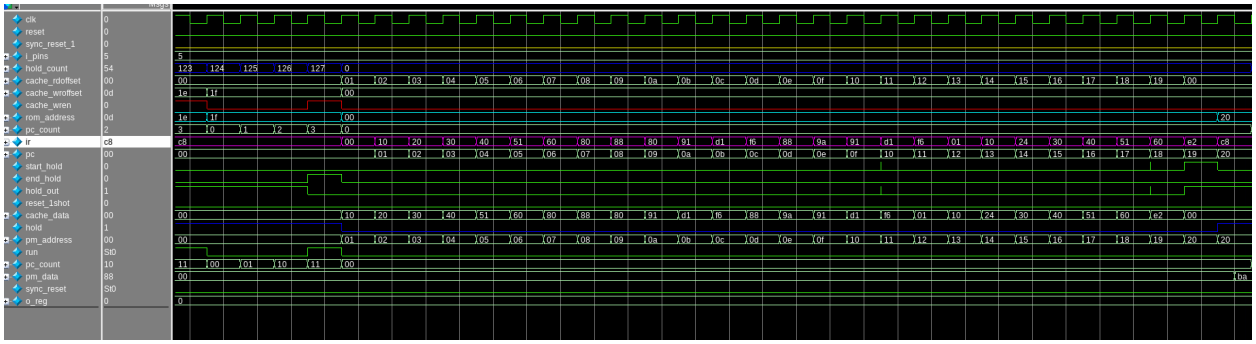

Figure 8: rom_more_clk_cache, data was readed when microprocessor was not suspended

- From rom_more_clk: According to figure 3 we can see ir = 8'HCF whenever pc_count = 3 and instruction register executed every 4 clock cycles.
- In figure 7: microprocessor was suspended for 128 clock cycles. At this time hold is on, for every 4 clock cycles, 32 instructions were written into cache.
- In figure 8: microprocessor was not suspended, at this time cache_wren was disable and data was read from cache.