Carry-Lookahead Adder

Objectives

In this lab, students will design a 32-bit carry-lookahead adder. Students will start with building smaller adder units and use them as a building block for larger adders. By the end of this lab, students should be able to:

- Understand the advantages and disadvantages of different types of adders (i.e. ripple carry, carry-lookahead, carry-save, etc.)
- Design and build a 1-bit, 4-bit, 16-bit and 32-bit carry-lookahead adder.

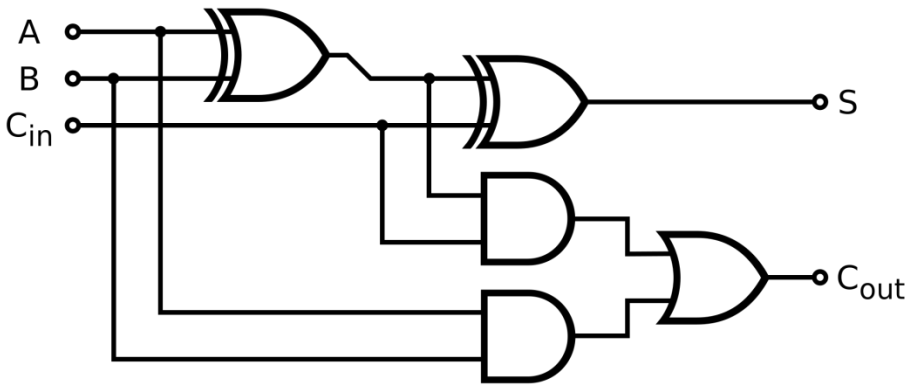
Preliminaries

Students should be familiar with the design of carry lookahead adders. More information can be found in Appendix C of the textbook "Computer Organization and Design: The hardware/software interface" by Patterson and Hennessy (the contents of Appendix C is in the CD).

Procedure

Ripple-Carry Adder

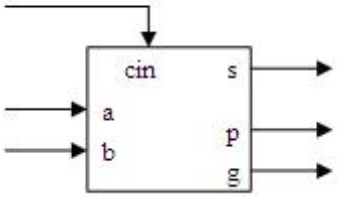
1. In Verilog HDL, build a 1-bit full adder using the following block diagram.



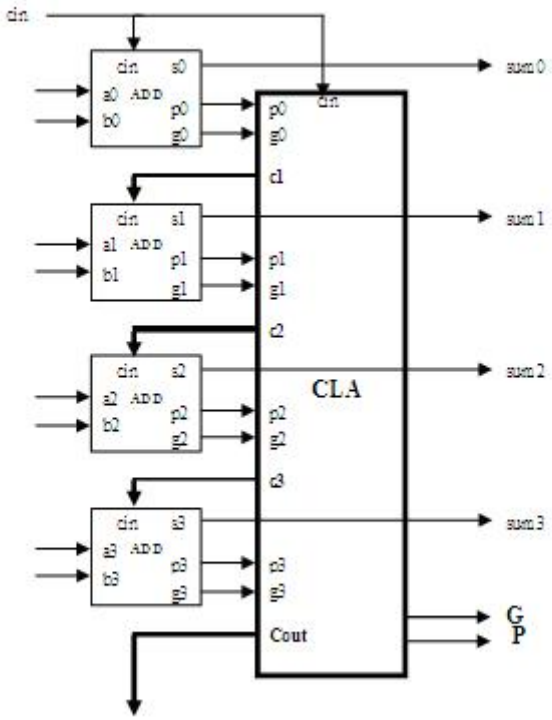
2. Using the 1-bit full adder, build a 32-bit ripple-carry adder.
3. Since FPGAs are synchronous designs, register all input and output signals of the adder.
4. Compile the design in Quartus Prime for the Cyclone IV EP4CE115F29 FPGA.
5. Simulate the resultant design using ModelSim to verify its functionality.
6. Record the hardware resource utilization and the maximum clock frequency of the design.

Carry-Lookahead Adder

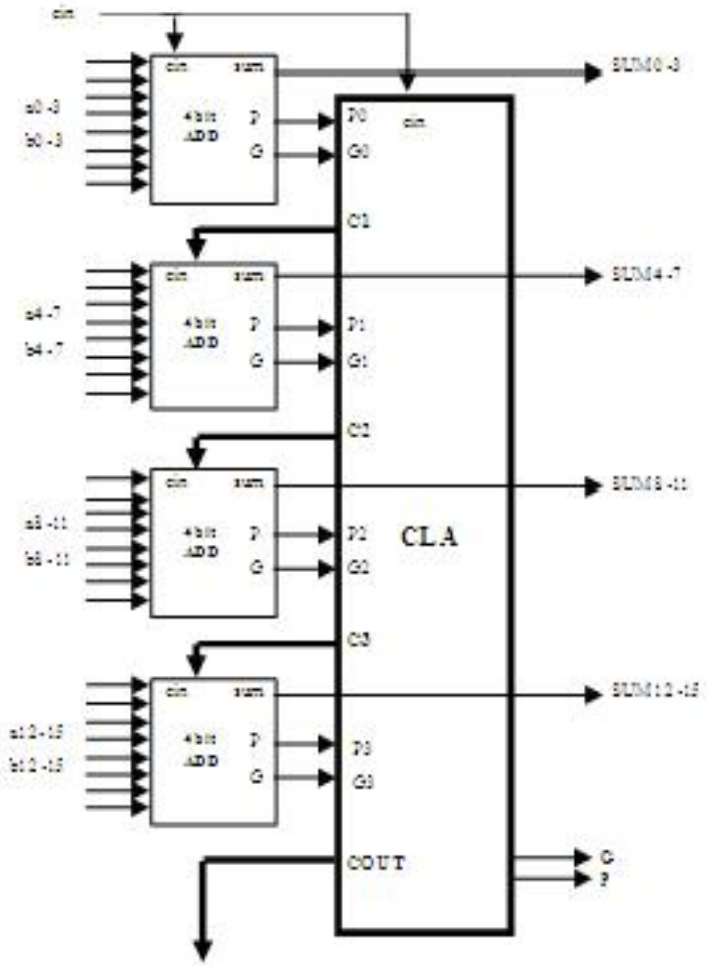
1. Design a 1-bit adder with 3 inputs and 3 outputs as follows, where s is the sum, p is the propagate signal and g is the generate signal.



2. Design a 4-bit CLA adder (figure below)
    a. This adder will take a, b, and cin inputs and generate sum, G, P, and Cout outputs.
    b. To build a 4-bit CLA adder, put 4 1-bit adders together with a CLA unit. The CLA unit generates the four carry signals (c1 – c4). It takes the first carry in, and the propagate and generate outputs from the four 1-bit adders, and uses them to create the carries. So you will need to generate c1 through c4 as outputs.



3. Design a 16-bit carry-lookahead adder. The expression for generating 16 carries in your CLA would get quite long. To avoid this we are going to use a hierarchical design for the 16-bit adder by using 4 4-bit adders and one CLA as shown in the figure below.



4. Extend your design to implement a 32-bit adder using 8 4-bit adders and redesign the CLA unit.
    a. Be sure to register all input and outputs as in the ripple-carry adder.
5. Compile the 32-bit carry-lookahead adder in Quartus Prime and choose the same FPGA as the ripple-carry adder.
6. Simulate the design in ModelSim to verify its functionality.
7. Note the hardware resource utilization and maximum clock frequency of the carry-lookahead adder and compare to the results of the ripple-carry adder.

Deliverables

Provide a formal report including the compilation results and the timing delay of the 32-bit ripple-carry and and carry-lookahead adders. Provide an analysis and explanation of the observations. Please be concise on the writing of the report.