Device Under Test:

Arithmetic Logic Unit

The device-under-test is a simple arithmetic logic unit (ALU) device with asynchronous reset. The device has two 8-bit inputs, alu_a_in and alu_b_in, for operands, and an 8-bit output, alu_y_out, for result. A complete list of the ports is showed below.

```
module alu(
  input        clk,
  input        reset,
  input  [7:0] alu_a_in, alu_b_in , // ALU 8-bit inputs
  input  [3:0] alu_opcode_in,       // ALU selection input
  output [7:0] alu_y_out,           // ALU 8-bit output
  output       alu_co_out           // Carryout flag
);
```

The opcodes of the ALU are listed below. The result of every operation is generated in one clock cycle.

0000	Addition	1000	Logical AND
0001	Subtraction	1001	Logical OR
0010	Multiplication	1010	Logical XOR
0011	Division	1011	Logical NOR
0100	Logical shift left	1100	Logical NAND
0101	Logic shift right	1101	Logical XNOR
0110	Rotate left	1110	A > B
0111	Rotate right	1111	A = B

In addition to conveying the carry resulting from an addition operation, the alu_co_out also indicates overflow for multiplication operation and underflow for division operation. In case of overflow, alu_y_out only gives the 8-bit value of LSB and alu_co_out is set to 1'b1. In case of underflow, alu_y_out is zero and alu_co_out is set to 1'b1. The result of divide-by-zero is simulator dependent, which is normally X.