Rutgers, the State University of New Jersey

Independent Study / Special Problems

FPGA Design - 8086 CPU

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I Summary

The 8086 is a 16-bit microprocessor that was released in 1978, the x86 architecture used on the CPU is still used to this day albeit in a 32bit version. The 8086 came as a 40 pin Dual In-line Package that could be used in various products such as the original IBM PC. Since the design is over 30 years old, all relevant patents have since expired and the designs have become open for free use and modification.

For this Independent Study, an 8086 processor will be implemented on an Altera DE0 Field Programmable Gate Array (FPGA) development board. An FPGA is a tool that is used for quickly prototyping and developing new hardware designs without the need for expensive fabrication plants and custom made chips. Instead, the FPGA chip (in this case a Cyclone III 3C16 FPGA) simulates hardware which can then interface with the intended product or design.

The final goal for this study is to create an 8086 processor on the Altera DE0 development board and then run MS-DOS, Microsoft's original command line operating system, in order to obtain a fully functioning computer with keyboard input and VGA output.

II Completed Work

In order to begin working on the project necessary research was completed as to the various requirements for completing this project. It was determined that an FPGA capable of at least 256 bytes of internal ROM and more than 9,000 logical elements or LE' s. As an added convenience, it was important to select a board that would be able to handle my project inputs and outputs such as PS2 keyboard and VGA output in order to spend more time on the study and not building miscellaneous hardware. From this research, it was determined that the Altera DE0 development board sufficiently the project needs with over 15,000 LE's, a VGA port, a PS2 port, buttons, LEDs, switches, and USB interface. Another important addition to the board is it's SD card slot which would be used to store the MS-DOS files.

This study has been sponsored by the Altera University Program in which they have provided an Altera DE0 development board as well as an Altera DE0-Nano development boards at no cost. This makes the projects overall required budget $0 since the sponsorship includes the relevant packages for creating hardware on the chip.

III Ongoing Progress

The next stages for the project is to begin work with the open source project "Zet Processor" which includes a modified version of the 8086 processor design by the OpenCores community. Once the processor is loaded, work with begin to install MS-DOS. This will be achieved by custom mapping a bios into memory and then instructing it to load the operating system. Finally once the operating system is installed, PS2 keyboard input and VGA output will be enabled to show the fully working operating system. If time permits additional software such as vintage games will be loaded to showcase the processors capabilities.

IV Appendix

Full specifications for Altera DE0 development board:

- FPGA
  - Cyclone III 3C16 FPGA
  - 15,408 LEs
  - 56 M9K Embedded Memory Blocks
  - 504K total RAM bits
  - 56 embedded multipliers
  - 4 PLLs
  - 346 user I/O pins
  - FineLine BGA 484-pin package
- Memory
  - SDRAM
    - One 8-Mbyte Single Data Rate Synchronous Dynamic RAM memory chip
  - Flash memory
    - 4-Mbyte NOR Flash memory
    - Support Byte (8-bits)/Word (16-bits) mode
  - SD card socket
    - Provides both SPI and SD 1-bit mode SD Card access
- Interface
  - Built-in USB Blaster circuit
    - On-board USB Blaster for programming
    - Using the Altera EPM240 CPLD
  - Altera Serial Configuration device
    - Altera EPCS4 serial EEPROM chip
  - Pushbutton switches
    - 3 pushbutton switches
  - Slide switches
    - 10 Slide switches
  - General User Interfaces
    - 10 Green color LEDs
    - 4 seven-segment displays
  - Clock inputs
    - 50-MHz oscillator
  - VGA output
    - Uses a 4-bit resistor-network DAC

    - With 15-pin high-density D-sub connector
    - Supports up to 1280x1024 at 60-Hz refresh rate
  - Serial ports
    - One RS-232 port (Without DB-9 serial connector)
    - One PS/2 port
  - Two 40-pin expansion headers
    - 72 Cyclone III I/O pins, as well as 8 power and ground lines, are brought out to two 40-pin expansion connectors
    - 40-pin header is designed to accept a standard 40-pin ribbon cable used for IDE hard drives

Available x86 Instructions: `http://zet.aluzina.org/index.php/Zet_status`

References

Altera University Program: `http://www.altera.com/education/univ/unv-index.html`
Altera DE0 development board: `http://www.altera.com/education/univ/materials/boards/de0/unv-de0-board.html`
Open Cores Project: `http://opencores.org/`
Zet Processor project: `http://zet.aluzina.org/index.php/Zet_processor`
Zet Processor source code: `https://github.com/marmolejo/zet`
Zero-Board-Computer: `https://github.com/donnaware/ZBC---The-Zero-Board-Computer`