

Elie Rosen

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Summary

U.S. citizen with security clearance, looking for full-time work in the areas of ASIC and FPGA front end design. Currently residing near Baltimore, MD and willing to relocate. Primary skills include; System Verilog, VHDL, Clock Domain Crossings, UVM, C/C++/C#, common scripting languages (Tcl, Python, Perl, UNIX), and protocols (JESD, PCIe, ONFI, GIGE, SFPDP) with a wide range of experience with multiple vendor tools.

Experience

Northrop Grumman - Mission Systems

LINTHICUM HEIGHTS, MD

ASIC Design and Verification Engineer

July '15 – Present

Anti-tamper processing implementation and verification • Experience with ARM architecture, AMBA, and cache design. • Experience with vendor IP integration and verification • Creation of custom scripts to increase team productivity • Designed gate-level verification flow to be used to verify entire design with back annotation • Automated and designed scripts to verify and resolve clock domain crossing issues • Implemented automated LINT checking across design

FPGA Design Engineer

Primary integration engineer for a radar system front end processor utilizing Vertex 7 series FPGAs. Implemented a JESD 204B serial RX path • Validated and corrected the DSP pipeline to ensure mathematical correctness • Implemented and designed a coherent SFPDP protocol for transmission of radar samples between panels and the radar processor • Maintained internal registers and documentation accordingly

Internal Professional Activities

- High School Innovation Challenge (HSIC) mentor to eight Ft. Meade High School students
- Professional Development Program Navigator to three recently hired engineers

Teledyne Lecroy

CHESTNUT RIDGE, NY

Digital IC Design Intern

May '14 – Aug '14

Designed the digital front-end of a 12-bit Analog/Digital converter for use in mid-range to high-end digital oscilloscopes. Worked with various communication protocols and standards including: SPI, JTAG, and JESD at the hardware implementation level. Implemented UVM test sequences and agents to verify overall system design. Created scripts for increased productivity in Cadence. Maintained accurate and detailed documentation for all completed work.

Rutgers University Electrical & Computer Engineering Department

PISCATAWAY, NJ

Teaching Assistant

June '13 – May '15

ECE 492/519: Hardware/Software Design of Embedded Systems • Developed the instructional lab for a new course at Rutgers based on the Altera Cyclone series FPGAs that includes topics on Flip-Flops and Latches, Addition Systems, Finite State Machines, ALUs, Ethernet, VGA, Nand Flash, and SRAM.

Expected student outcome: A complex understanding of FPGAs and their use in industry including advanced knowledge of the VHDL hardware description language and proper testing and verification techniques for implementing functional hardware.

Siemens Industry, Inc.

DALLAS, TX

Electrical and Controls Automation Engineer Intern

May '12 – Aug '12

Programmed Schneider Modicon Quantum PLC to build [Baggage Handling System \(BHS\)](#) for Minneapolis St. Paul airport • Designed [Human Machine Interface \(HMI\)](#) used for overview of BHS system health and operator controls • Created tools to generate documentation and test plans from databases with over 10,000 entries • Primary presenter of the [Factory Acceptance Test](#) to client; enabling project to enter the next stage of development

Education

Rutgers, the State University of New Jersey

NEW BRUNSWICK, NJ

Masters of Science in Computer Engineering • GPA: 3.83/4.00

2013 – 2015

Rutgers, the State University of New Jersey

NEW BRUNSWICK, NJ

Bachelor of Science in Electrical & Computer Engineering

2009 – 2013

Minor: Entrepreneurship • GPA: 3.17/4.00