# Elie Rosen

elie.rosen@bltinc.com Office: 888.945.4691

## Summary

U.S. citizen with security clearance,Primary skills include; System Verilog, VHDL, Clock Domain Crossings, UVM, C/C++/C#, common scripting languages (Tcl, Python, Perl, UNIX), and protocols (JESD, PCIe, ONFI, GIGE, SFPDP) with a wide range of experience with multiple vendor tools.

## Experience

### Bottom Line Technologies, Inc. — Ellicott City, MD

**Project Engineer** *Nov '17 – Present*

Certified Xilinx Trainer with extensive background in Xilinx UltraScale+ Zynq MPSoC/RFSoC, UltraScale+ and 7 Series architecture, and high-performance FPGA design techniques • Project Lead for a RFSoC VPX COTS based design • Designed and verified HW/SW for a dual MPSoC VPX switch card to support over 400 Gbps of HSSIO • Architected and Designed a controller to synchronize audio between multiple mobile devices • Created Linux drivers to support the Xilinx XDMA PCIe IP Core

### Northrop Grumman - Mission Systems — Linthicum Heights, MD

**ASIC Design and Verification Engineer** *July '15 – Oct '17*

Anti-tamper processing implementation and verification • Experience with ARM architecture, AMBA, and cache design. • Experience with vendor IP integration and verification • Creation of custom scripts to increase team productivity • Designed gate-level verification flow to be used to verify entire design with back annotation • Automated and designed scripts to verify and resolve clock domain crossing issues • Implemented automated LINT checking across design

**FPGA Design Engineer**

Primary integration engineer for a radar system front end processor utilizing Vertex 7 series FPGAs. Implemented a JESD 204B serial RX path • Validated and corrected the DSP pipeline to ensure mathematical correctness • Implemented and designed a coherent SFPDP protocol for transmission of radar samples between panels and the radar processor • Maintained internal registers and documentation accordingly

**Internal Professional Activities**

- High School Innovation Challenge (HSIC) mentor to eight Ft. Meade High School students
- Professional Development Program Navigator to three recently hired engineers

### Teledyne Lecroy — Chestnut Ridge, NY

**Digital IC Design Intern** *May '14 – Aug '14*

Designed the digital front-end of a 12-bit Analog/Digital converter for use in mid-range to high-end digital oscilloscopes. Worked with various communication protocols and standards including: SPI, JTAG, and JESD at the hardware implementation level. Implemented UVM test sequences and agents to verify overall system design. Created scripts for increased productivity in Cadence. Maintained accurate and detailed documentation for all completed work.

### Rutgers University Electrical & Computer Engineering Department — Piscataway, NJ

**Teaching Assistant** *June '13 – May '15*

**ECE 492/519: Hardware/Software Design of Embedded Systems** • Developed the instructional lab for a new course at Rutgers based on the Altera Cyclone series FPGAs that includes topics on Flip-Flops and Latches, Addition Systems, Finite State Machines, ALUs, Ethernet, VGA, Nand Flash, and SRAM.

### Siemens Industry, Inc. — Dallas, TX

**Electrical and Controls Automation Engineer Intern** *May '12 – Aug '12*

Programmed Schneider Modicon Quantum PLC to build Baggage Handling System (BHS) for Minneapolis St. Paul airport • Designed Human Machine Interface (HMI) used for overview of BHS system health and operator controls • Created tools to generate documentation and test plans from databases with over 10,000 entries • Primary presenter of the Factory Acceptance Test to client; enabling project to enter the next stage of development

## Education

### Rutgers, the State University of New Jersey — New Brunswick, NJ

**Masters of Science in Computer Engineering • GPA: 3.83/4.00** *2013 – 2015*

Rutgers, the State University of New Jersey — New Brunswick, NJ
**Bachelor of Science in Electrical & Computer Engineering** — *2009 – 2013*
**Minor: Entrepreneurship • GPA: 3.17/4.00**