

Elie Rosen

<http://linkedin.com/in/elierosen>

elie@mylifeiscomputers.net

<http://www.mylifeiscomputers.net>

Employment Interest

My experiences and hobbies have allowed me to sharpen my hardware engineering skills in these areas: VLSI, FPGAs, ASICs, Embedded Systems, Robotics, and Computer Vision. I am willing to relocate for a full-time position.

Skills & Projects

Programming Languages: System Verilog, UVM, VHDL, Perl, C, C++, C#, LaTeX, MySQL, x86 Assembly

FPGA, PCB, and VLSI: Xilinx Vivado HLS, Altera Quartus II, Cadence Design and Simulation Tools

Project Portfolio: Computer Vision, FPGAs, Robotics, and more at <http://erosen.github.io>

Experience

Teledyne Lecroy

CHESTNUT RIDGE, NY

Digital IC Design Intern

May '14 – Aug '14

Designed the digital front-end of a 12-bit Analog/Digital converter for use in mid-range to high-end digital oscilloscopes. Worked with various communication protocols and standards including; SPI, JTAG, and JESD at the hardware implementation level. Implemented UVM test sequences and agents to verify overall system design. Created scripts for increased productivity in Cadence. Maintained accurate and detailed documentation for all completed work.

Rutgers University Electrical & Computer Engineering Department

PISCATAWAY, NJ

Teaching Assistant

June '13 – Present

ECE 492/519: Hardware/Software Design of Embedded Systems • Developed the instructional lab for a new course at Rutgers based on the Altera DE2-115 FPGA Development Board that includes topics on Flip-Flops and Latches, Addition Systems, Finite State Machines, ALUs, Ethernet, VGA, and RAM.
Expected student outcome: A complex understanding of FPGAs and their use in industry including advanced knowledge of the VHDL hardware description language and proper testing and verification techniques for implementing functional hardware.

Siemens Industry, Inc.

DALLAS, TX

Electrical and Controls Automation Engineer – Intern

May '12 – Aug '12

Programmed Schneider Modicon Quantum PLC to build **Baggage Handling System (BHS)** for Minneapolis St. Paul airport • Designed **Human Machine Interface (HMI)** used for overview of BHS system health and operator controls • Created tools to generate documentation and test plans from databases with over 10,000 entries • Primary presenter of the **Factory Acceptance Test** to client; enabling project to enter the next stage of development

Professional Activities

- IEEE MGA Young Professionals / Student Activities Liaison & STEP Coordinator (May '13 – Present)
- IEEE Princeton / Central Jersey Young Professionals Chair (June '13 – Present)
- Co-Founded, the Rutgers School of Engineering Academic Integrity Task Force (Sept '12 – May '13)
- Rutgers Entrepreneurial Society (Sept '09 – May '11)
- Webmaster, Engineering Governing Council (Sept '10 – '11)

Education

Rutgers, the State University of New Jersey

NEW BRUNSWICK, NJ

Masters of Science in Computer Engineering • GPA: 3.83/4.00

2013 – May '15 (expected)

Relevant coursework: Computer Architecture, Transistor Circuit Design, and VLSI

Rutgers, the State University of New Jersey

NEW BRUNSWICK, NJ

Bachelor of Science in Electrical & Computer Engineering

2009 – May '13

Minor: Entrepreneurship • GPA: 3.17/4.00

Relevant coursework: Computer Architecture, Digital Electronics, Digital Logic Design, Digital Systems Design, Discrete Mathematics, Operating Systems, and Robotics & Computer Vision