Standard Cell Template

AOI

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Introduction and Physical Properties

Cell Description

An AOI circuit implements two or more AND operations and OR operation. The logical representation for 2-1AOI is (A+B).C In this Lab experiment we are trying to model the AOI logic using the lengths and widths already used in the Lab experiment 2 and lab experiment 3 and then drive different fan outs using the AOI DUT. The loads are also derived from the previous lab experiments.

At first the AIO schematics with various fan-outs are drawn and then layouts are drawn in the layout editor. Then DRC report is generated to check if the design violates any design rules defined for a process and LVS report is generated to verify the schematics against the layout drawn. The PEX report gives the parasitic extraction which gives a better model to perform the analysis for delay and power.

Cell Symbol

We used the standard logic symbols for the assigned standard cells. The symbols are then extracted for the AOI, Inverter and the loads.

Standard Cell Template

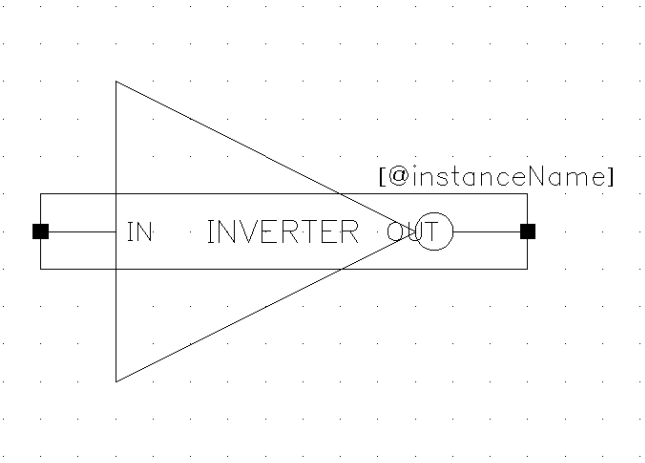

Figure 1: Example Logic Symbol from NCSU Digital Parts. All symbols are 1in tall.

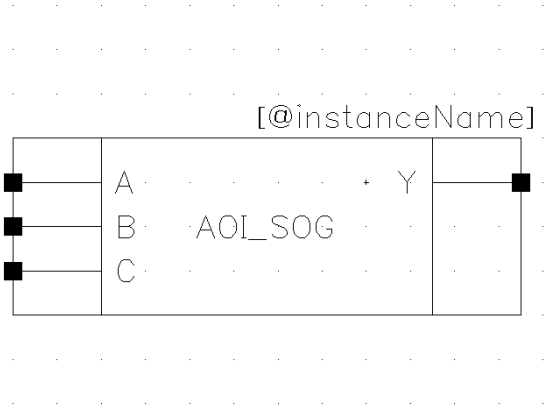

Figure 2: Symbol of AOI

Cell Truth Table

Complete the truth table for all cell outputs using {0, 1} for the input low and high, respectively and {L, H} for the output low and high, respectively. Repeat rows and columns as needed.

A	B	C	Y
0	0	0	L
0	0	1	L
0	1	0	L
0	1	1	H
1	0	0	L

1	0	1	H
1	1	0	L
1	1	1	H

Table 1: Truth Table

Cell Schematic Diagram

Prepare Encapsulated Postscript of the schematic for publication (Cadence has this option in the Virtuoso schematic design). Do not use a screen shot or create Encapsulated Postscript of the raw schematic. For each "publication schematic" in NSCU CDK remove the transistor width and length, model name etc. but leave the instance names of the pins and transistor. This makes the schematic easier to read.

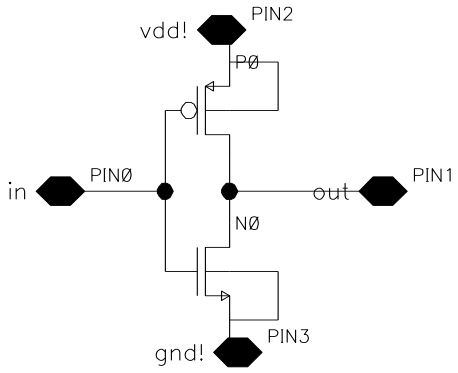

Figure 2: Example Schematic from NCSU CDK Publication Schematic. All schematic figure are 2in tall.

Standard Cell Template

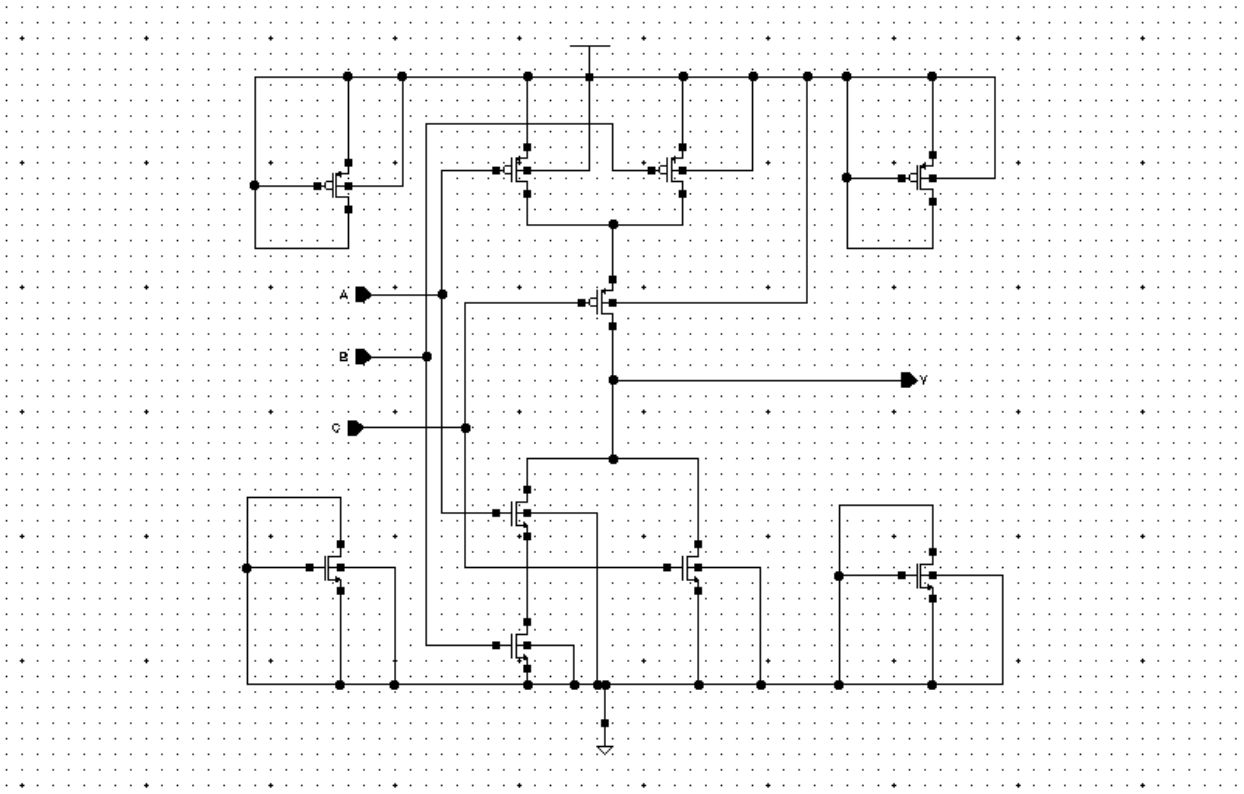

Figure 3: Transistor level of AOI Sea of Gates

Cell Layout Diagram and Dimensions

Save a color or black and white layout of the cell in EPS (i.e. Encapsulated Postscript) format. The cell dimensions are saved in both lambda (λ) and microns (μm). Record the transistor length and width dimensions (nm).
[Repeat the transistor row as needed.]

Cell Physical Dimensions		
	X	Y
Cell Dimension in λ		
Cell Dimension in μm		
Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
P0	50	945
N0	50	425

Table 1.2 Dimensions of the DUT for full custom

Cell Physical Dimensions

Standard Cell Template

Cell Physical Dimensions		
	X	Y
Cell Dimension in λ		
Cell Dimension in μm		
Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
P0	50	270
N0	50	180

Table 1.3 Dimensions of the DUT for sea of gates

Cell Physical Dimensions		
	X	Y
Cell Dimension in λ		
Cell Dimension in μm		
Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
P0	50	270
N0	50	180

Table 1.4 Dimensions of the fanouts for full custom

Cell Physical Dimensions		
	X	Y
Cell Dimension in λ		
Cell Dimension in μm		
Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
P0	50	270
N0	50	180

Table 1.5 Dimensions of the fanouts for sea of gates

Input and Output Parasitic Capacitance Table

From the schematic calculate each input's capacitance normalized to the nominal inverter (your inverter standard cell) by the width of the transistor or drain area as needed. This entry should be an integer fraction similar to Weste and Harris.

Standard Cell Template

[Note the normalization is to a standard inverter (the standard cell inverter INV1X). Repeat the rows as needed.]

Computed Cell Input Capacitance	
Input Name	**Capacitance (/Cinv)**
Output Name	**Capacitance (/Cinv)**

Performance Analysis

Rise and Fall Times

[Note: It is highly desirable to split the simulation work load among the team members so that each team member learns how to use the tools.]

FOx denotes output loads. The loads are defined by the number of identical logic gates. Use 20%-80% swings for the output rise and fall entries. Use a 1.2V power supply.

For each output load in the table complete transient simulations. Remember to include a CMOS non-inverting buffer between the ideal voltage source and the logic gate driving the FOx load. Note rise t_r / fall t_f times are at the input to the logic gate driving the load, **not** the rise/fall times for the input ideal voltage source.

Complete the number needed copies (copies = No. input stacks x No. outputs) of the table below.

For multi-input gates, complete tables for each transistor stack (i.e. each branch connected to the output) using the stack's worst case single controlling input transition in the stack. Label the tables with worst case input in each stack and the output. Replace **X** below with the signal name.

Input X: Output Rise Time Data t_r (ns)					
Input rise/fall time (ns)	Output Load (FOx) 0	1	2	4	8
0.04					

Input X: Output Rise Time Data t_r (ns)					
0.06					

Table 1.5 Rise time for full custom

Input X: Output Rise Time Data t_r (ns)					
Input rise/fall time (ns)	Output Load (FOx) 0	1	2	4	8
0.04	0.2272	0.0697	0.0913	0.1443	0.2624
0.06					

Table 1.6 Rise time for sea of gates

Stack Input Combination: ***Replace with Boolean Product***

Stack S, Input X: Output Fall Time Data t_f (ns)					
Input rise/fall time (ns)	Output Load (FOx) 0	1	2	4	8
0.04					
0.06					

Table 1.7 Fall time for full custom

Stack S, Input X: Output Fall Time Data t_f (ns)					
Input rise/fall time (ns)	Output Load (FOx) 0	1	2	4	8
0.04	0.1503	0.0538	0.067	0.0982	0.1601
0.06					

Table 1.8 Fall time for sea of gates

Stack Input Combination: ***Replace with Boolean Product***

Propagation Delays

For the range of output loads shown in the table simulate propagation delays (low to high t_{plh} and high to low t_{phl}) for the stack's worst case single controlling input transition. The input controlling the output is the same input reported in the rise and fall time section. Use a 1.2V power supply and timing measurements start when input to the logic gate driving the FOx load crosses the 50% of the rail and stop when the logic gate driving output crosses 50% of the rail. Negative values are entered as 0.

Standard Cell Template

Label the tables with the Boolean product (e.g. AB) of the transistor stack and the output. Complete copies of the table below for each branch connected to the output.

Data Worst Case Low to High Propagation Delay Data t_{plh} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	0.1034	0.1087	0.11404	0.11293	0.14805
0.06					

Table 1.9 tplh for full custom

Data Worst Case Low to High Propagation Delay Data t_{plh} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	0.1762	0.0692	0.0834	0.1129	0.1711
0.06					

Table 1.10 tplh for sea of gates

Worse Case Input Combination: ***Replace with Boolean Product***

Data Worst Case High to Low Propagation Delay Data t_{phl} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8
0.04	0.09369	0.09737	0.10089	0.1251	0.12109
0.06					

Table 1.11 tphl for full custom

Data Worst Case High to Low Propagation Delay Data t_{phl} (ns)					
Input rise/fall time (ns)	Output Load (FOx)				
	0	1	2	4	8

Standard Cell Template

Data Worst Case High to Low Propagation Delay Data t_{phl} (ns)					
0.04	0.1212	0.0481	0.0584	0.0779	0.1172
0.06					

Table 1.12 tphl for sea of gates

Worse Case Input Combination: ***Replace with Boolean Product***

From each row of the slew rate data compute the best fit linear propagation delay equation for low-to-high T_{plh} (h) and high-to-low T_{phl} (h). The model predicts a delay, in nanoseconds, as a function of the output load, *h*, *Cout/Cin =FOx*. The model line is parameterized by a slope, *m*, and an intercept, *b*. The units of *m* are (*ns/FOx*) and the units of *b* are *ns*.

Complete the table below by increasing the number of rows for multiple input gates. The row labeled **All data** is the computed slope and intercept after combining data from all slew rates.

Complete the **Model** row for the gate using the assumptions and methods of the linear delay model from Weste and Harris. Only skewed standard cells will have different values propagation models for rising and falling inputs.

All data means combine the results for both slew rates into a single model.

Discuss in your own words the differences in the calibration and the Weste Harris linear delay model. Discuss the differences in high-to-low versus low-to-high models.

Data Model Propagation Delay Equation $T_{pd}(h) = b + m \cdot h$				
Input Slew Rate (ns)	Rising Logical Effort (m_r)	Falling Logical Effort (m_f)	Parasitic Rising Delay (b_r)	Parasitic Falling Delay (b_r)
0.04				
0.06				
All data				

In the table below normalize the model for the T_{pd} (h) results of the table above to give the logical effort model *D(h)* described in Weste and Harris. *D(h)* is a unitless value and predicts the delay as multiples of the standard inverter delay.

Standard Cell Template

Normalization is based on the observed CMOS inverter parasitic delay, b_{inv}. *Recall* ***all data*** $p_{inv} \equiv 1$.

Inverter Normalized Data Model Propagation Delay Equation $D(h) = p + g \cdot h$				
Input Slew Rate (ns)	Rising Logical Effort (g_r)	Falling Logical Effort (g_f)	Parasitic Rising Delay (p_r)	Parasitic Falling Delay (p_r)
0.04				
0.06				
All data				
W&H Model				

Power-Delay

Simulate the cell for a sequence of input combinations based on the Gray code and compute the time averaged power (mW), average delay (ns), and average power-delay product (mW ns = pJ). The Gray code restricts the simulations to single input transitions and ignores the large number of multiple input change combinations. Use the same slew rate for all input transitions. Use equal output loads for multiple output gates. Use a period of 2X maximum output delay with FO=8.

Average Power Data (mW)					
Input Slew (ns)	Output Load (FOx) 0	1	2	4	8
0.04				$5.251\ e^{-3}$	
0.06					

Table 1.13 Average power data for full custom

Average Delay Data (ns)					
Input Slew (ns)	Output Load (FOx) 0	1	2	4	8
0.04				0.120015	

Average Delay Data (ns)					
0.06					

Table 1.14 Average delay data for full custom

Average Power-Delay Data (pJ)					
Input Slew (ns)	Output Load (FOx) 0	1	2	4	8
0.04				0.630198 e^{-3}	
0.06					

Table 1.15 Average power- delay data for full custom

Average Power Data (mW)					
Input Slew (ns)	Output Load (FOx) 0	1	2	4	8
0.04				25.33 e^{-3}	
0.06					

Table 1.16 Average power data for sea of gates

Average Delay Data (ns)					
Input Slew (ns)	Output Load (FOx) 0	1	2	4	8
0.04				0.1015	
0.06					

Table 1.17 Average delay data for sea of gates

Average Power-Delay Data (pJ)					
Input Slew (ns)	Output Load (FOx) 0	1	2	4	8
0.04				2.570995 e^{-3}	
0.06					

Table 1.18 Average power- delay data for sea of gates

SEA OF GATES :

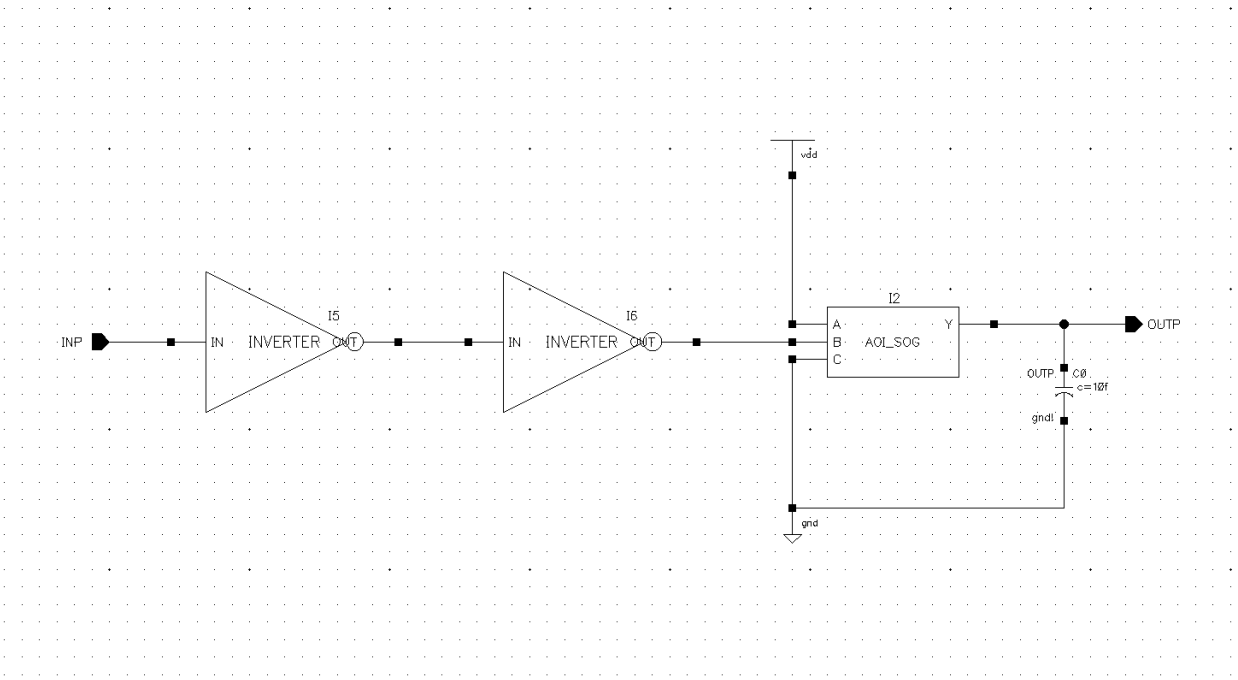

Figure 4: Schematics of AOI_SOG with no load (FO0)

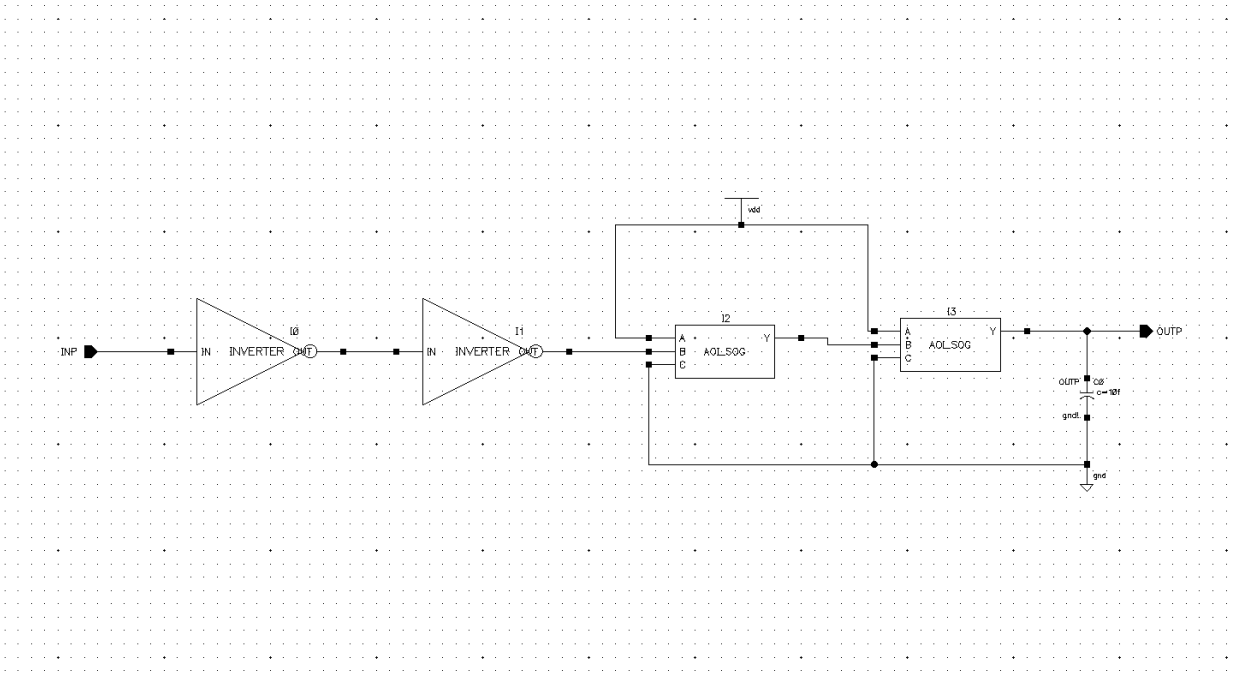

Figure 5: Schematics of AOI_SOG with one fanout (FO1)

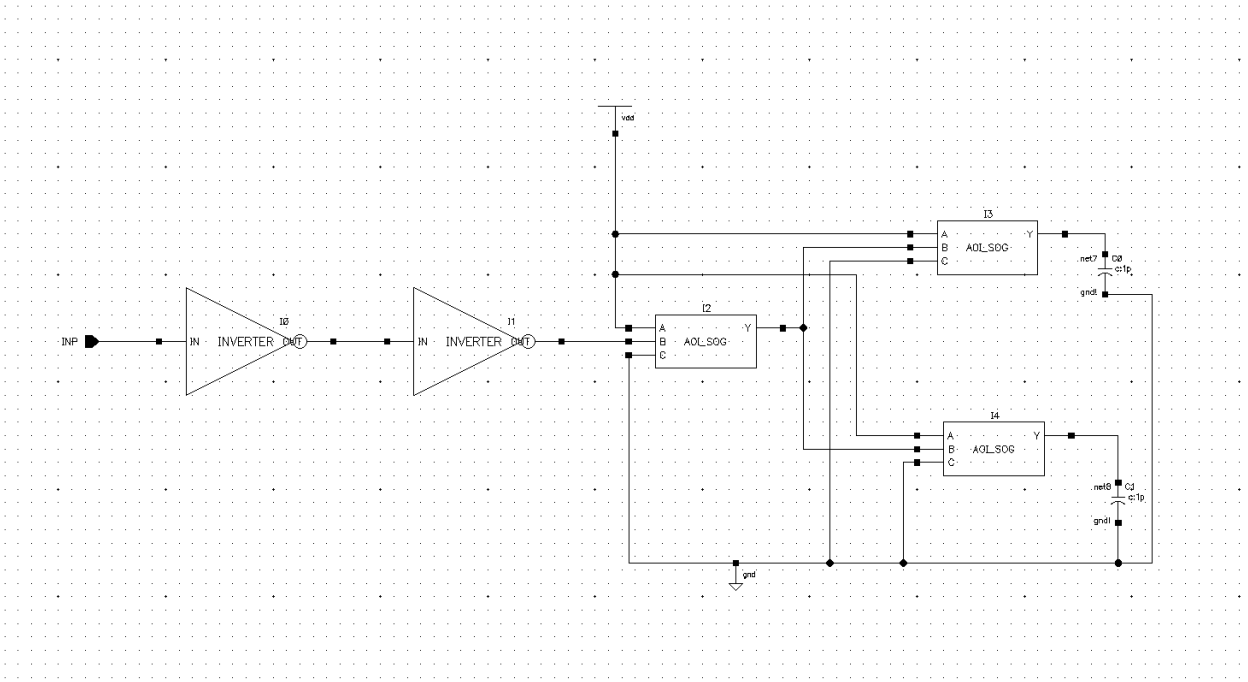

Figure 6: Schematics of AOI_SOG with two fanouts (FO2)

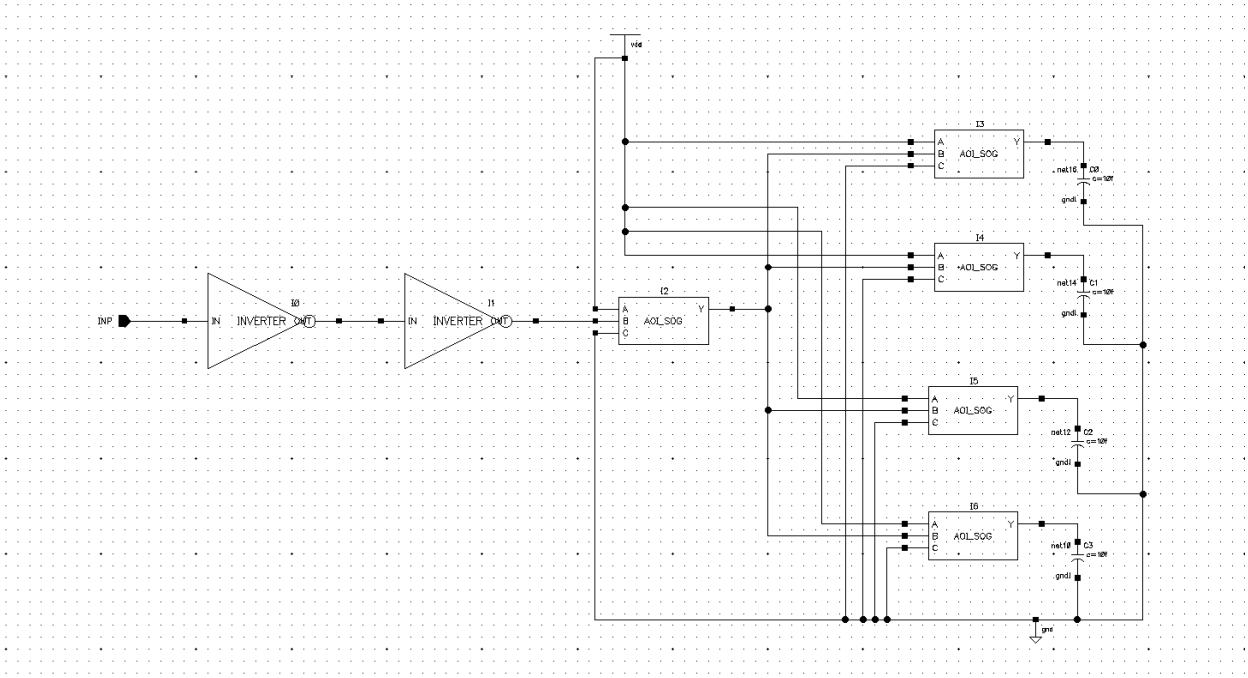

Figure 7: Schematics of AOI_SOG with four fanouts (FO4)

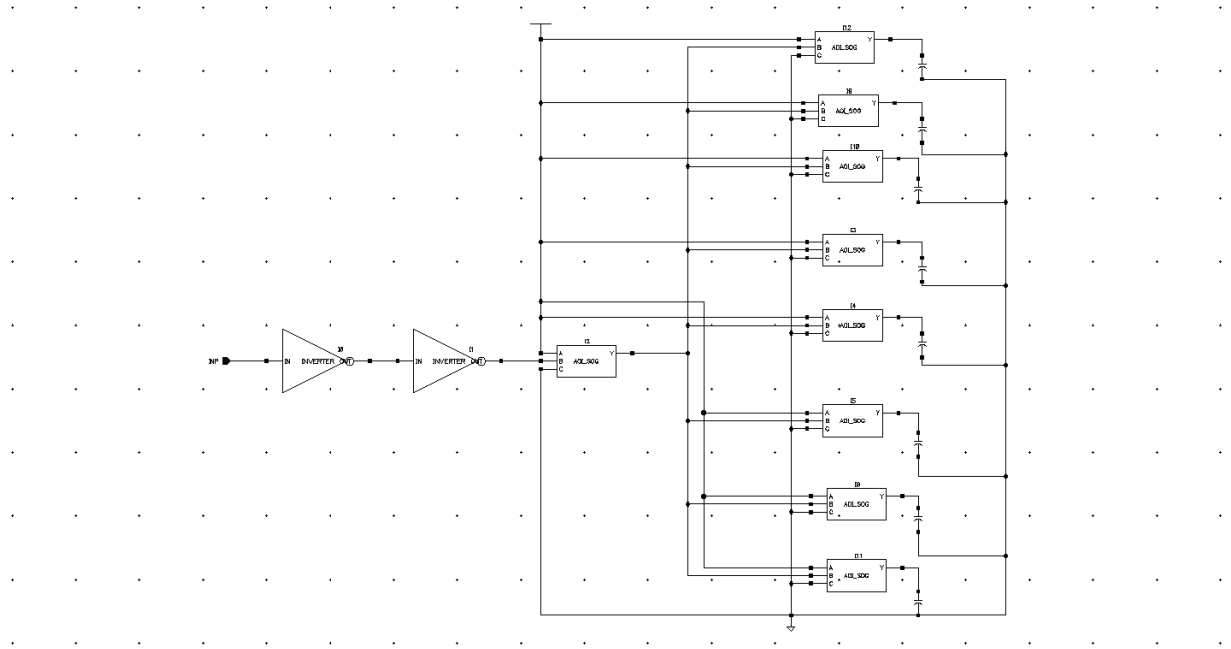

Figure 8: Schematics of AOI_SOG with eight fanouts (FO8)

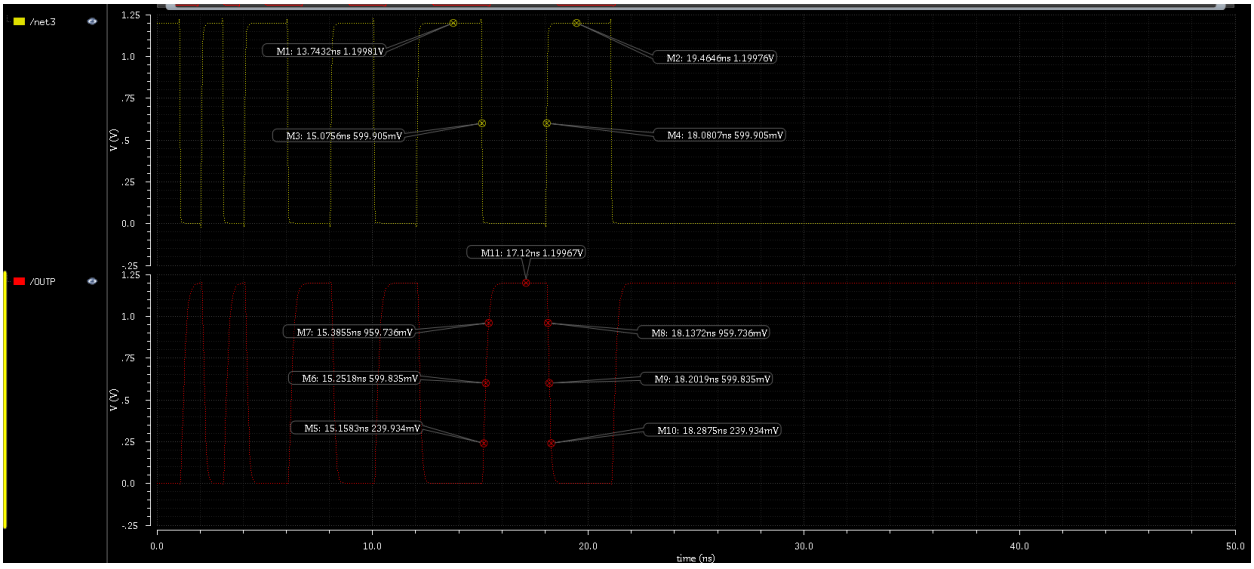

Figure 9: Transient Analysis of AOI with no load (FO0)

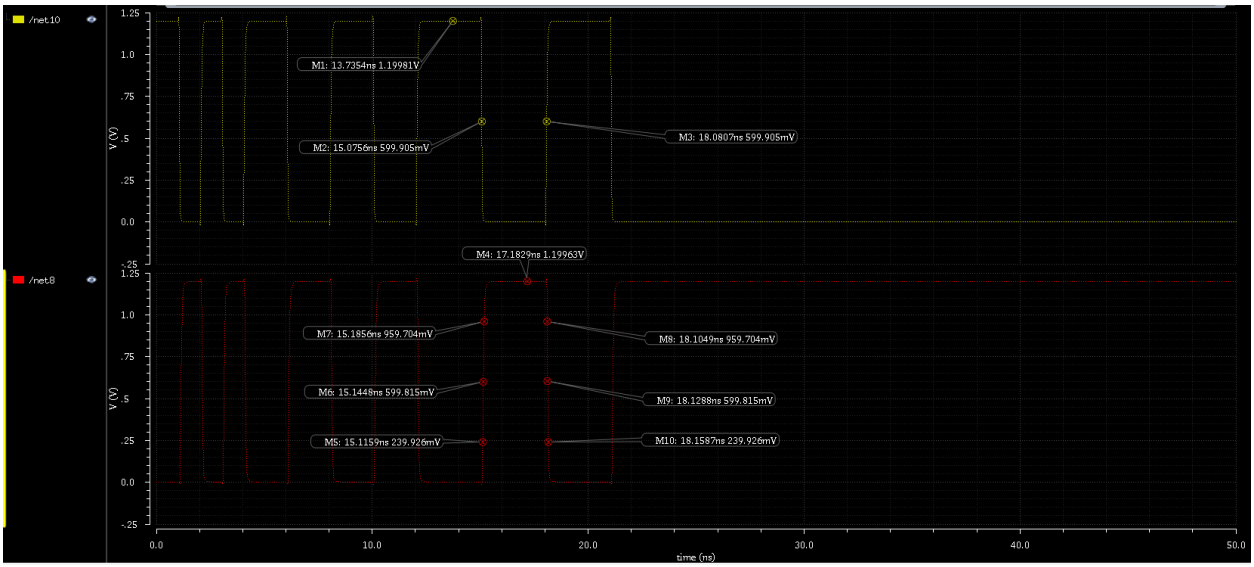

Figure 10: Transient Analysis of AOI with one fanout (FO1)

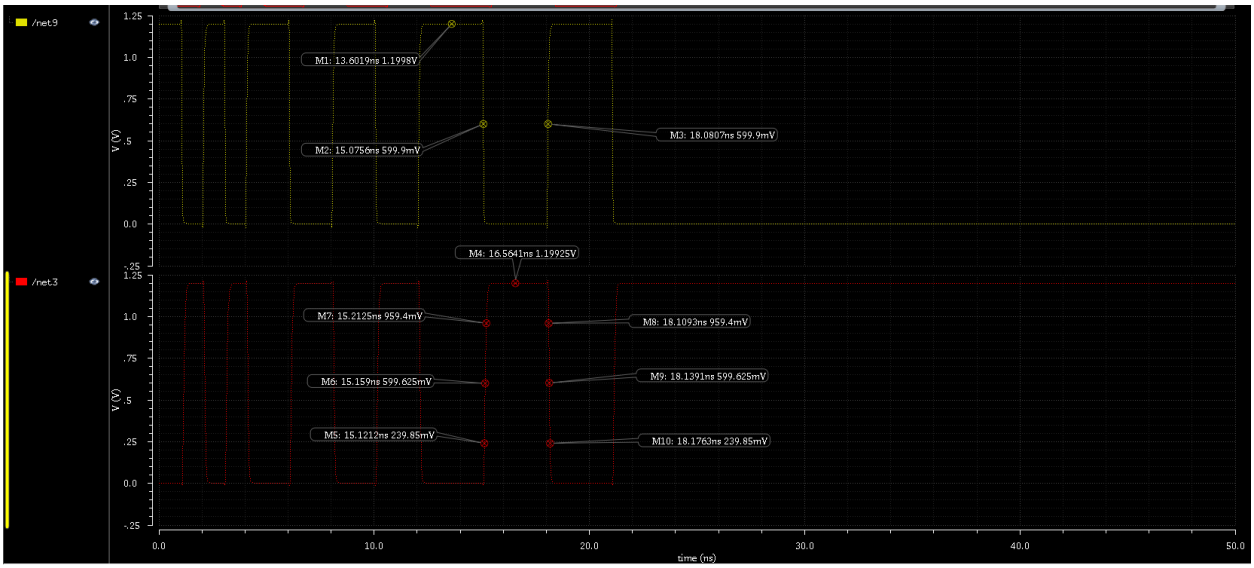

Figure 11: Transient Analysis of AOI with two fanouts (FO2)

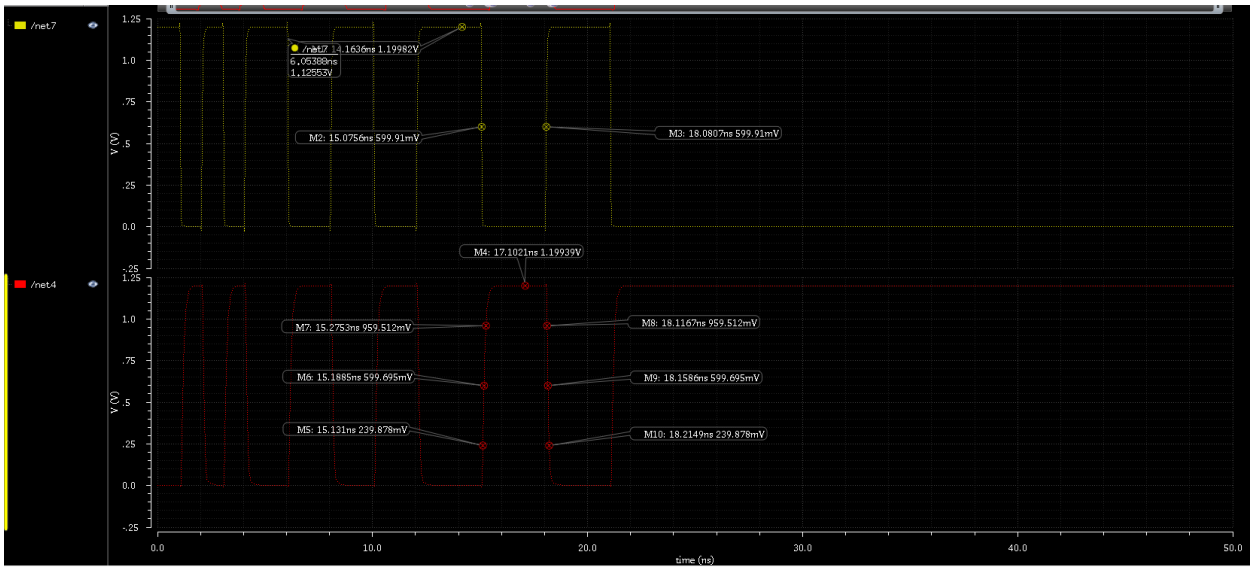

Figure 12: Transient Analysis of AOI with four fanouts (FO4)

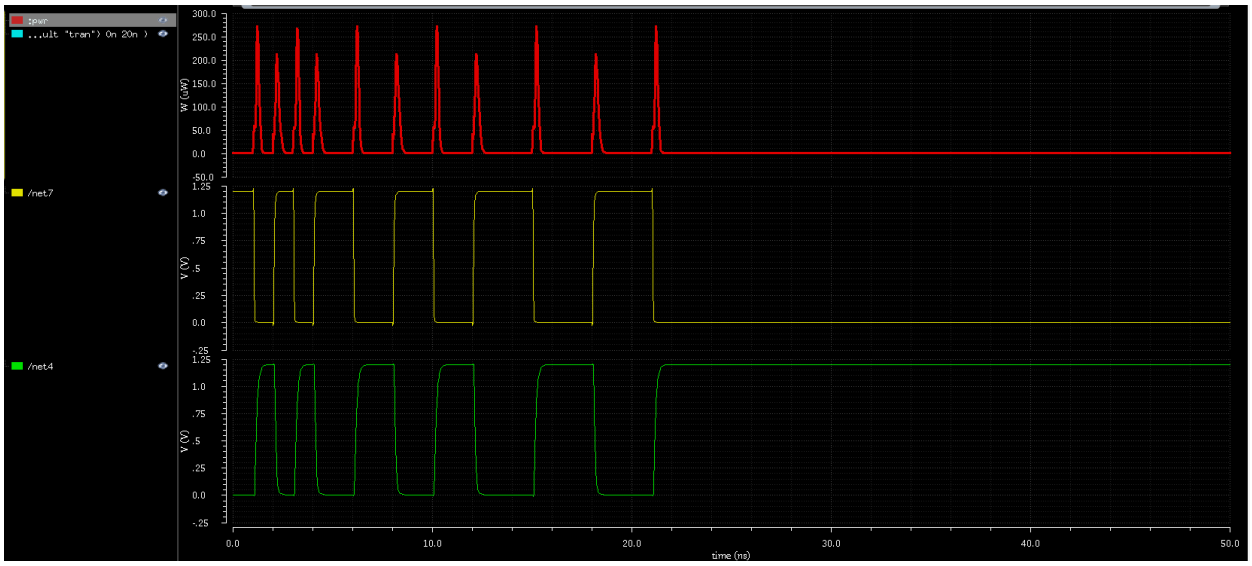

Figure 13: Power Graph of AOI with four fanouts (FO4)

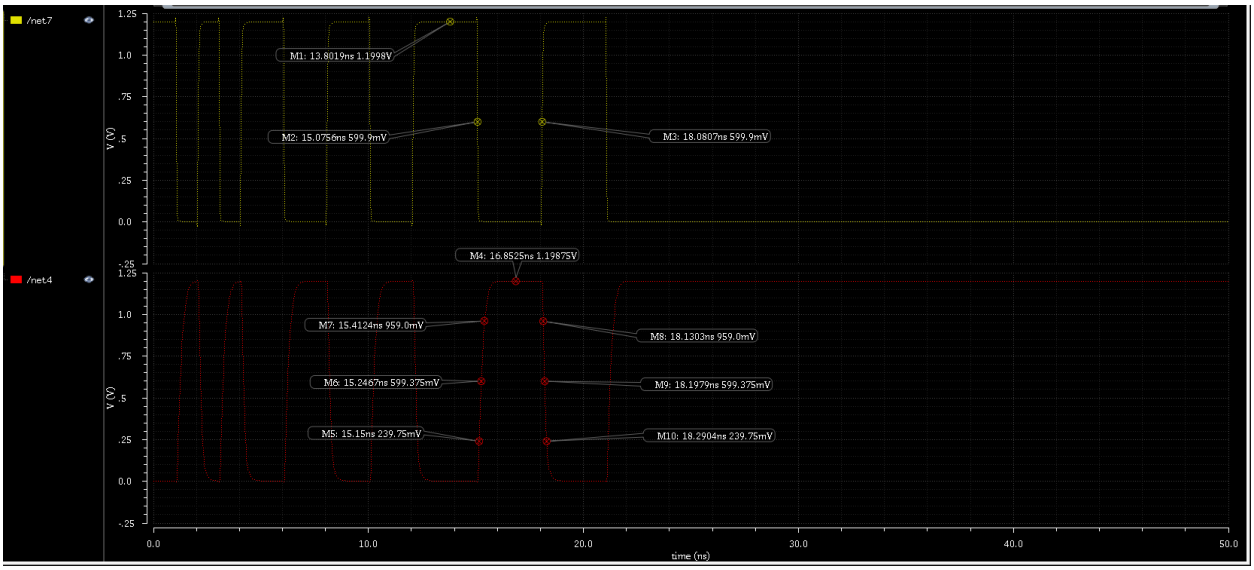

Figure 14: Transient Analysis of AOI with eight fanouts (FO8)

FULL CUSTOM :

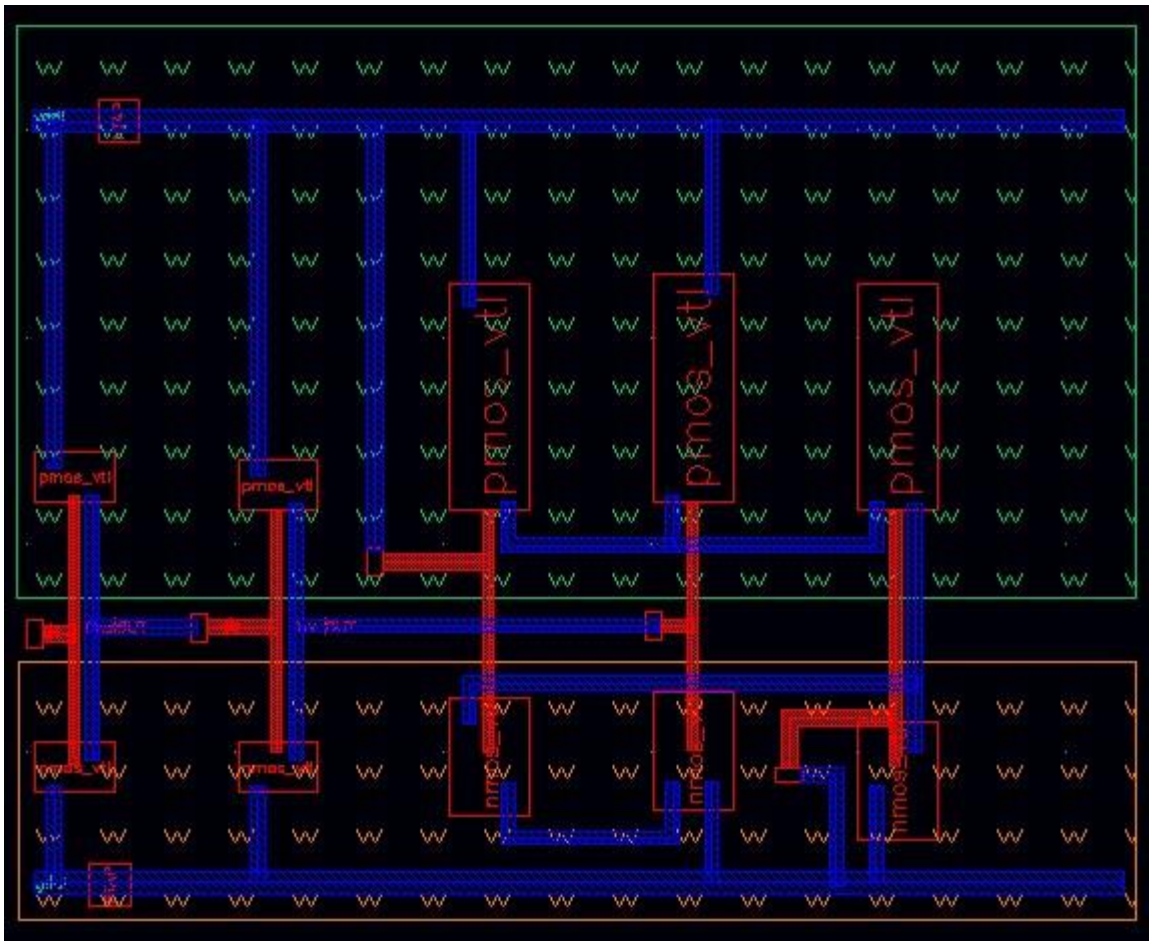

Figure 15: Layout of AOI with no load (FO0)

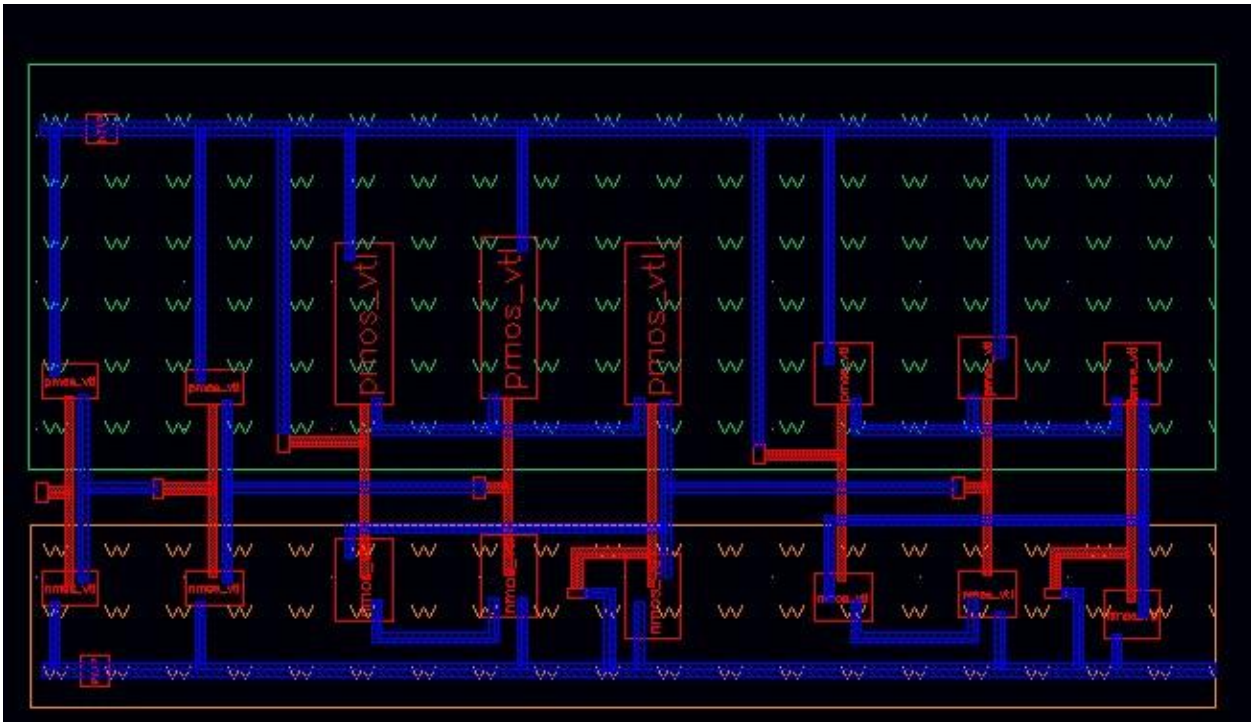

Figure 16: Layout of AOI with one fanout (FO1)

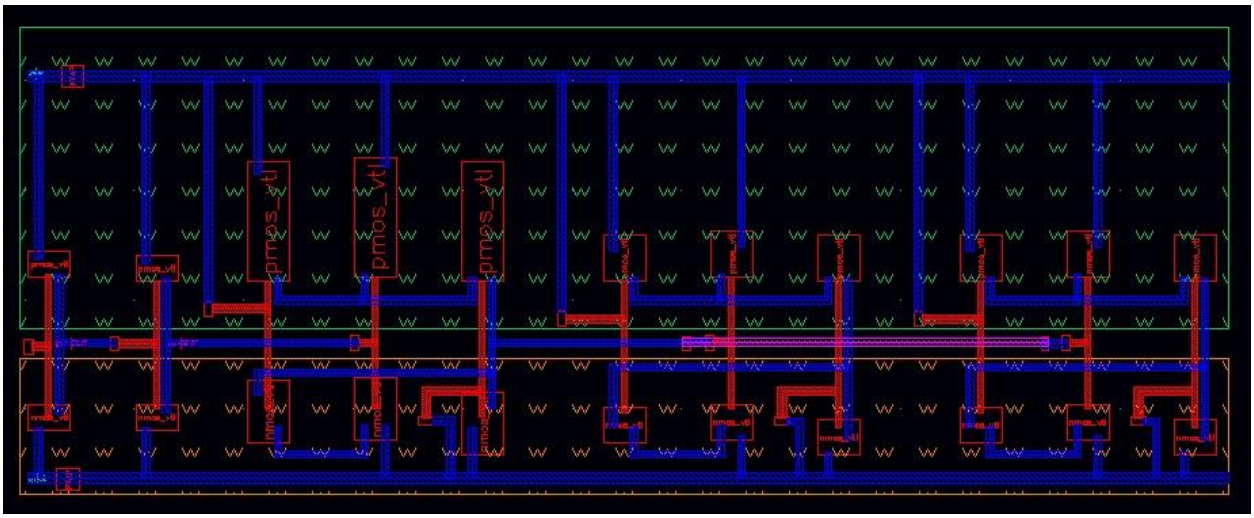

Figure 17: Layout of AOI with two fanouts (FO2)

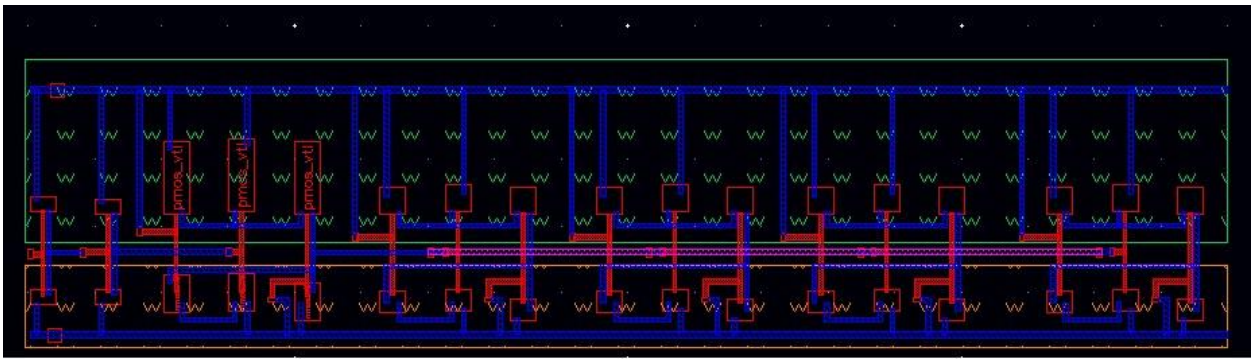

Figure 18: Layout of AOI with four fanouts (FO4)

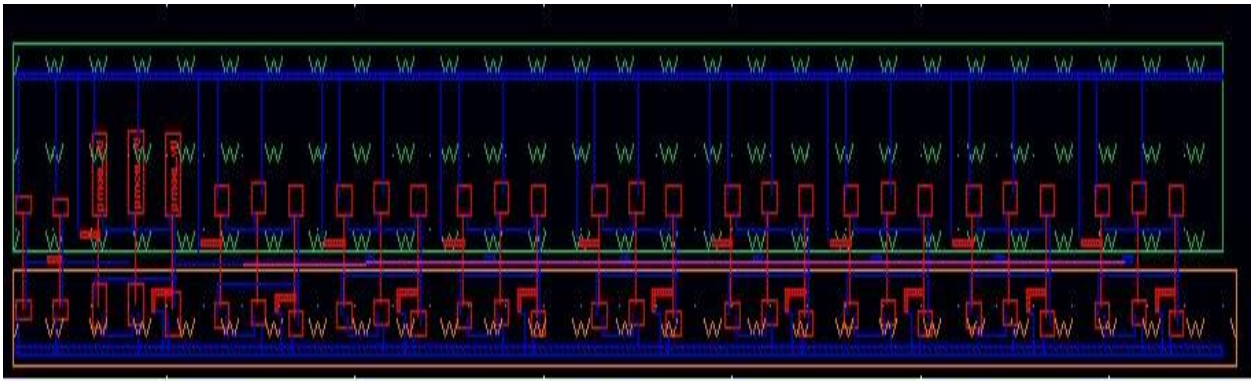

Figure 19: Layout of AOI with eight fanouts (FO8)

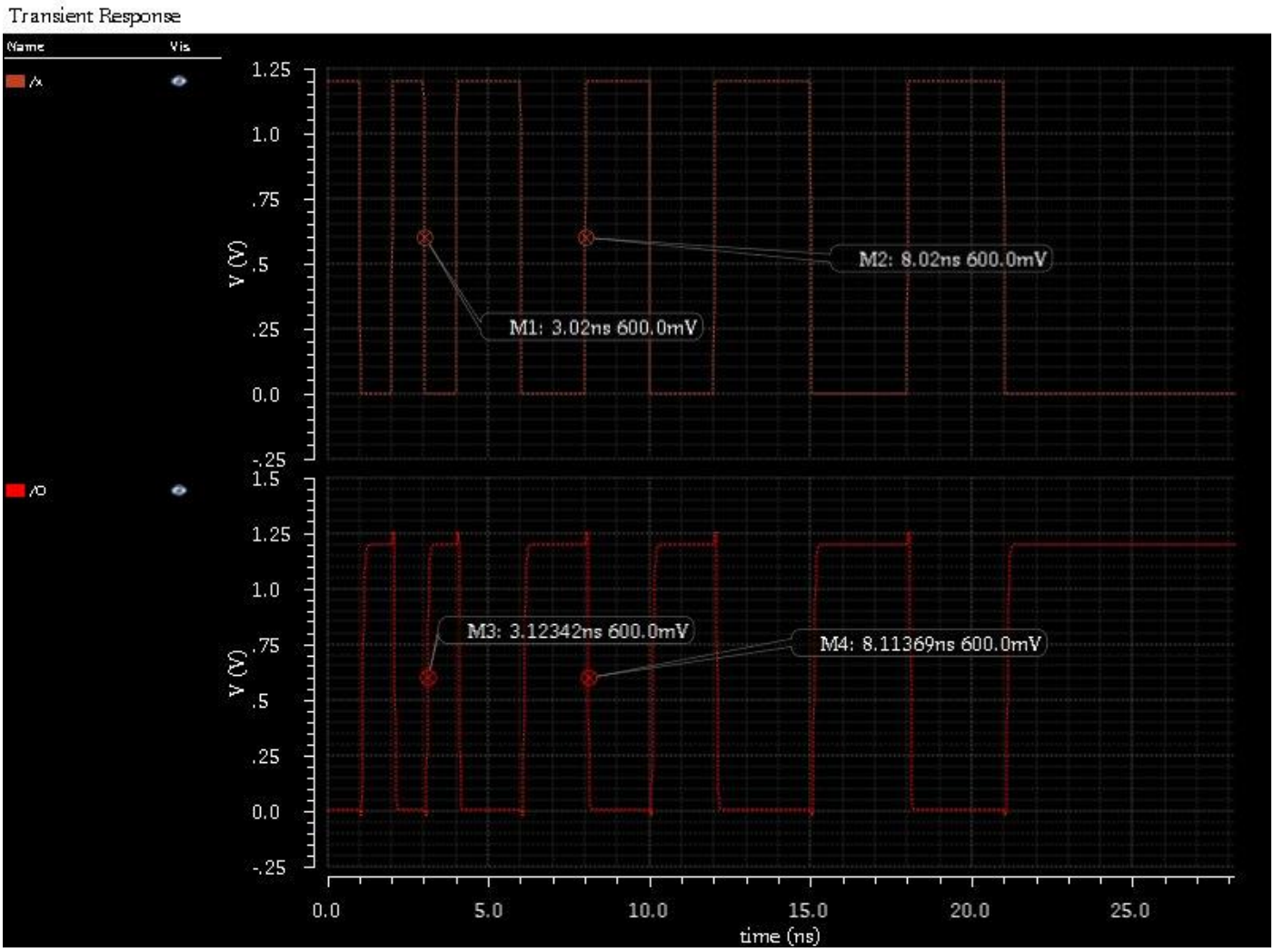

Figure 20: Transient Analysis of AOI with no load (FO0)

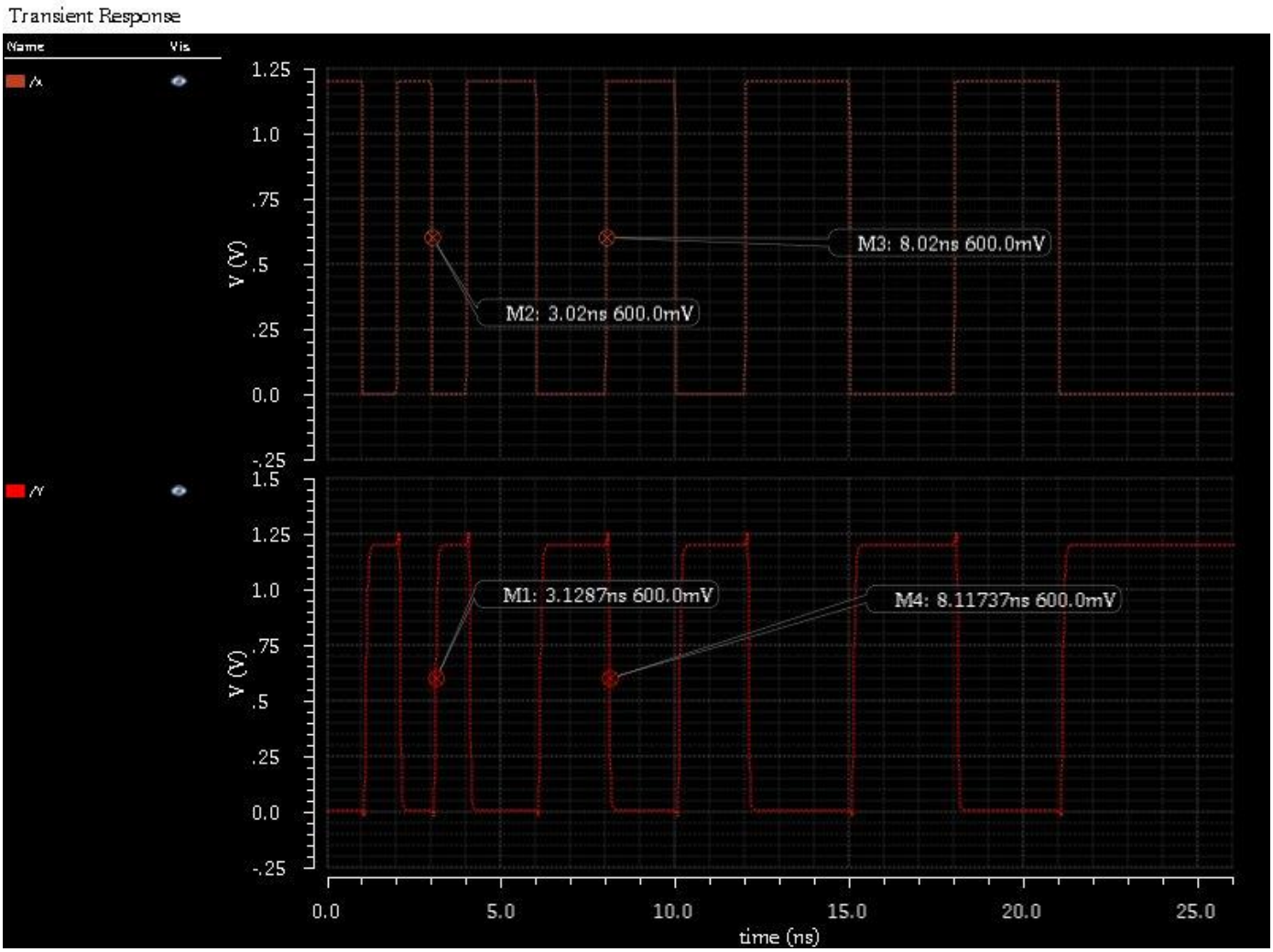

Figure 21: Transient Analysis of AOI with one fanout (FO1)

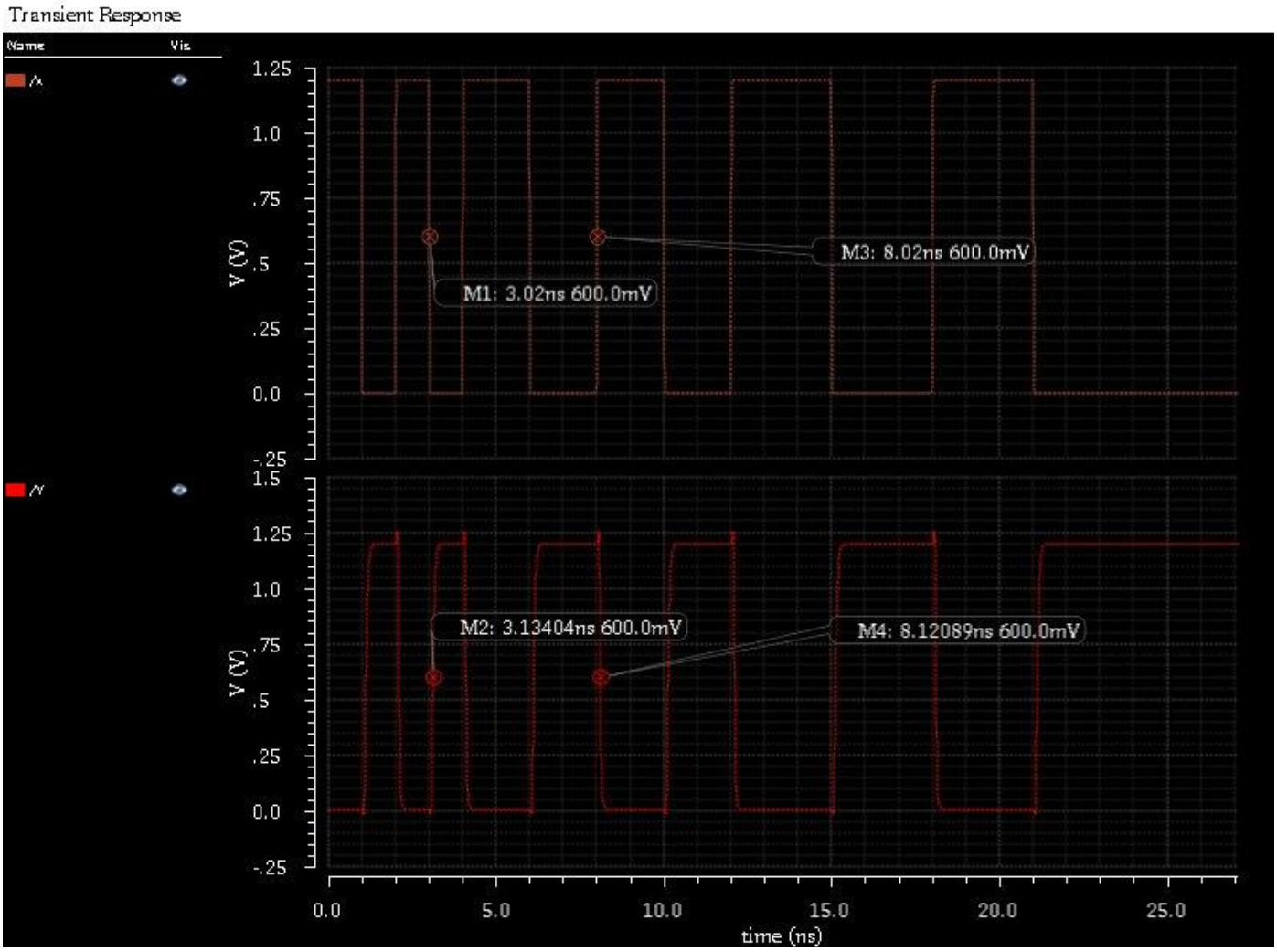

Figure 22: Transient Analysis of AOI with two fanouts (FO2)

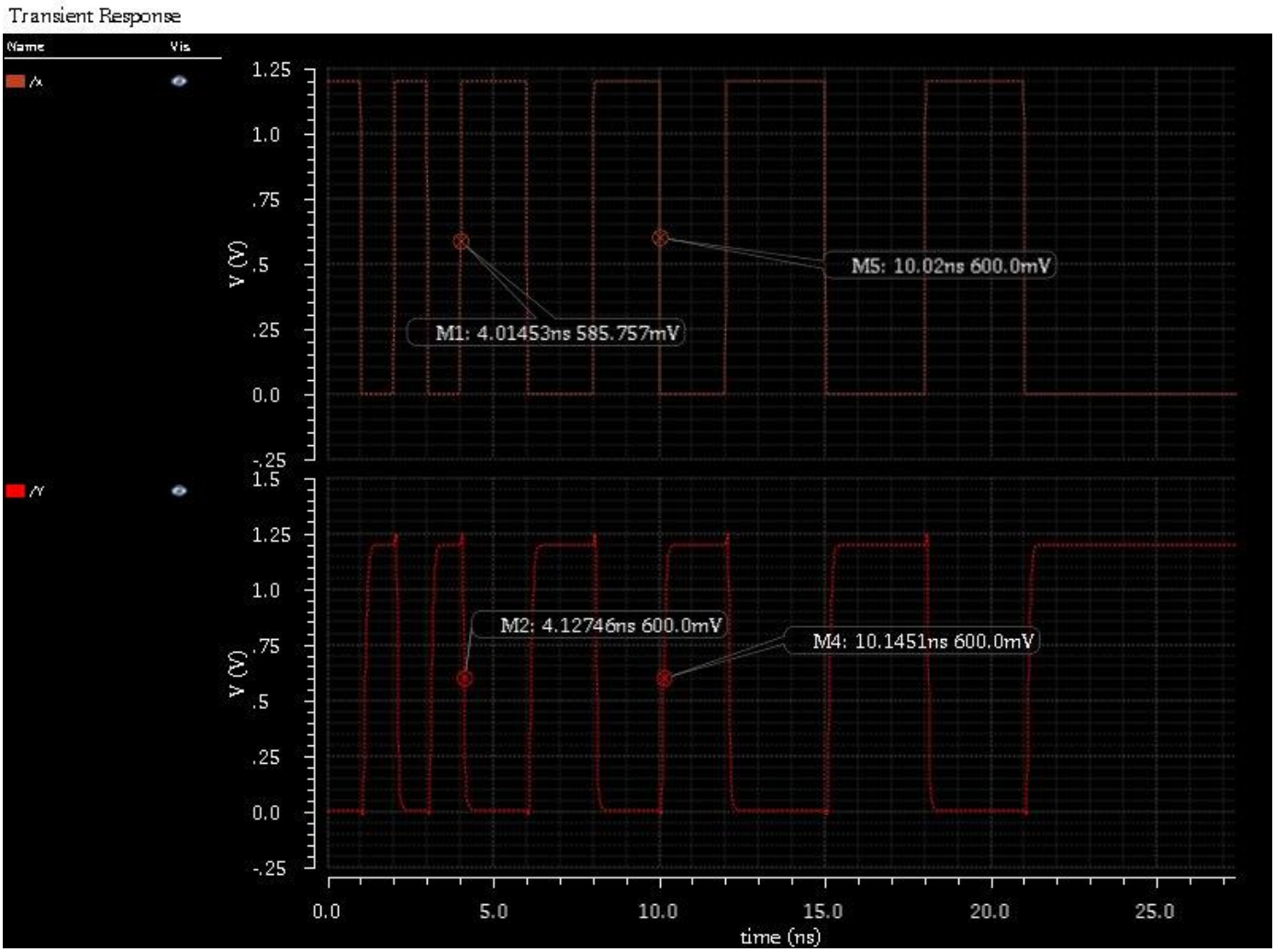

Figure 23: Transient Analysis and Power data of AOI with four fanouts (FO4)

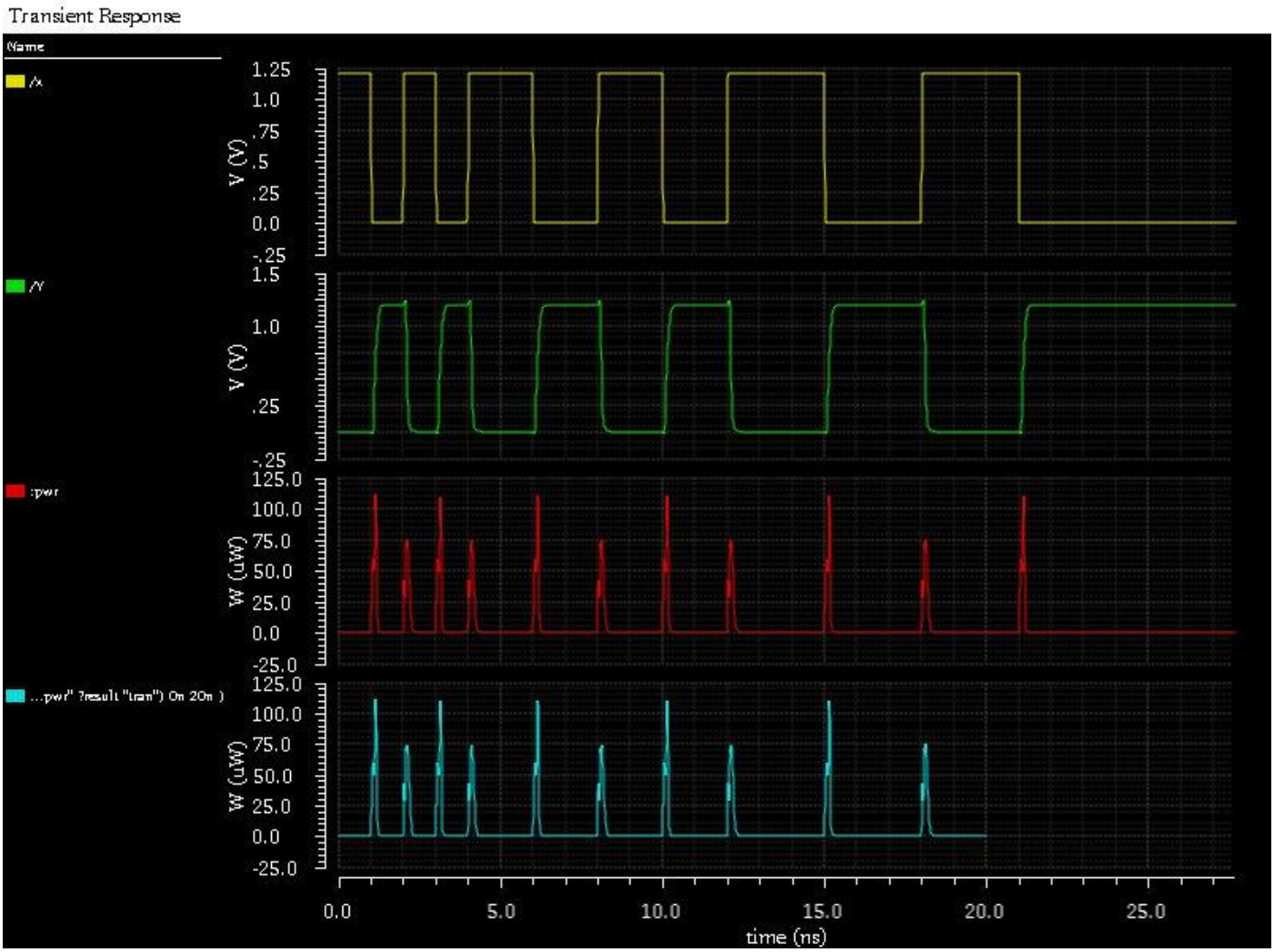

Figure 24: Power data of AOI with four fanouts (FO4)

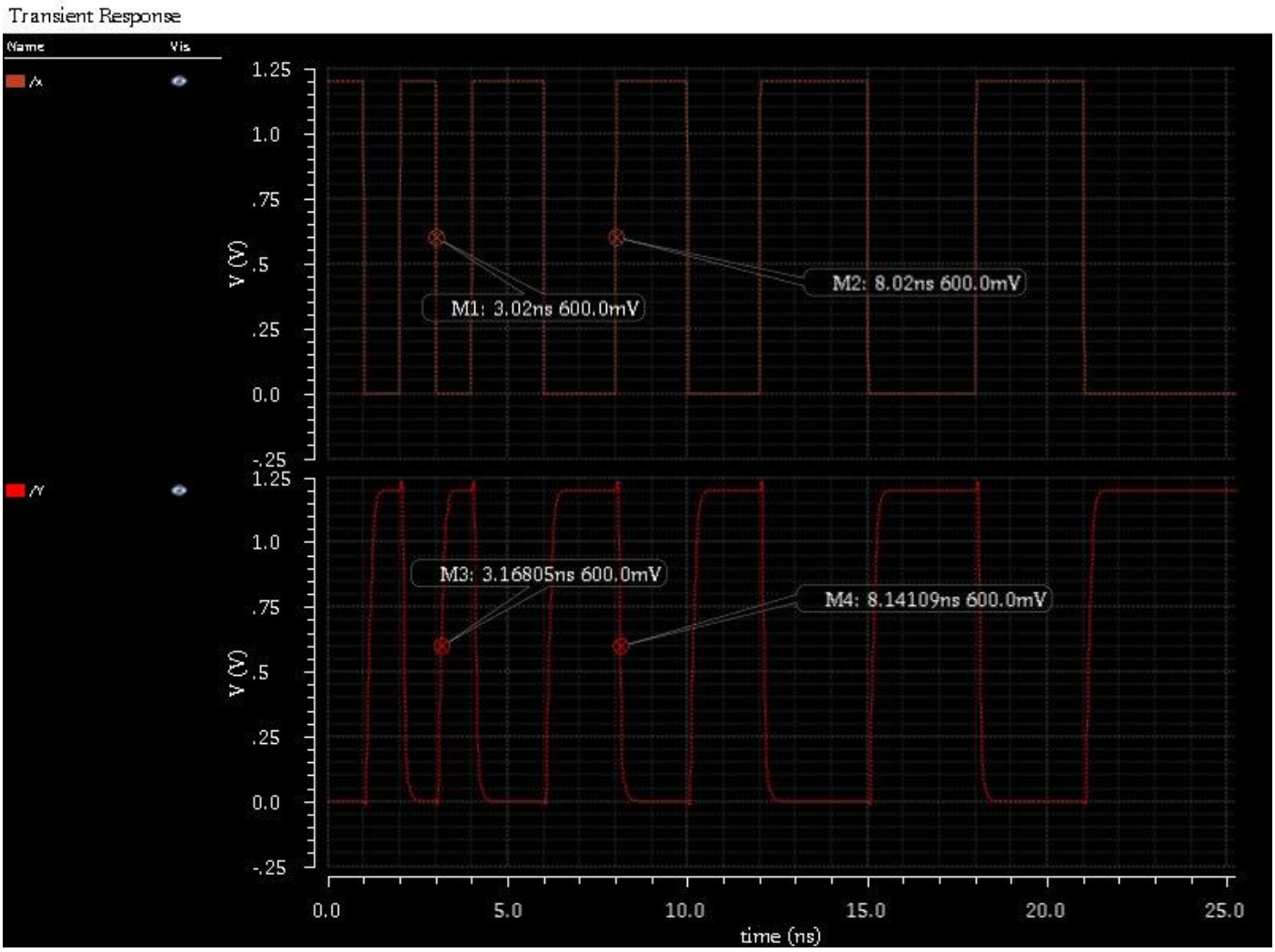

Figure 25: Transient Analysis of AOI with eight fanouts (FO8)

DRC Reports for Full Custom :

FO0

```
================================================================================
============
=== CALIBRE::DRC-F SUMMARY REPORT
===
Execution Date/Time:       Mon Mar 13 21:04:27 2017
Calibre Version:           v2013.2_35.25    Wed Jul 3 15:43:57 PDT
2013
Rule File Pathname:        /u/haranadh/cadence/DRC-
files/_calibreDRC.rul_
Rule File Title:
Layout System:             GDS
Layout Path(s):            AOI_Custom_FO0.calibre.db
Layout Primary Cell:       AOI_Custom_FO0
Current Directory:         /u/haranadh/cadence/DRC-files
User Name:                 haranadh
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      AOI_Custom_FO0.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       AOI_Custom_FO0.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID
= NO
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:         COMMENT TEXT + RULE FILE INFORMATION
Layers:                    MEMORY-BASED
Keep Empty Checks:         YES
--------------------------------------------------------------------------
------------
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------------
------------
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ...... TOTAL Original Geometry Count = 7
LAYER nwell ...... TOTAL Original Geometry Count = 7
LAYER active ..... TOTAL Original Geometry Count = 72
LAYER poly ....... TOTAL Original Geometry Count = 45
LAYER pimplant ... TOTAL Original Geometry Count = 6
LAYER nimplant ... TOTAL Original Geometry Count = 6
LAYER vth ........ TOTAL Original Geometry Count = 0
LAYER vtg ........ TOTAL Original Geometry Count = 0
```

```
LAYER metal1 ..... TOTAL Original Geometry Count = 48
LAYER metal2 ..... TOTAL Original Geometry Count = 0
LAYER metal3 ..... TOTAL Original Geometry Count = 0
LAYER metal4 ..... TOTAL Original Geometry Count = 0
LAYER metal5 ..... TOTAL Original Geometry Count = 0
LAYER metal6 ..... TOTAL Original Geometry Count = 0
LAYER metal7 ..... TOTAL Original Geometry Count = 0
LAYER metal8 ..... TOTAL Original Geometry Count = 0
LAYER metal9 ..... TOTAL Original Geometry Count = 0
LAYER metal10 .... TOTAL Original Geometry Count = 0
LAYER contact .... TOTAL Original Geometry Count = 75
LAYER via1 ....... TOTAL Original Geometry Count = 0
LAYER via2 ....... TOTAL Original Geometry Count = 0
LAYER via3 ....... TOTAL Original Geometry Count = 0
LAYER via4 ....... TOTAL Original Geometry Count = 0
LAYER via5 ....... TOTAL Original Geometry Count = 0
LAYER via6 ....... TOTAL Original Geometry Count = 0
LAYER via7 ....... TOTAL Original Geometry Count = 0
LAYER via8 ....... TOTAL Original Geometry Count = 0
LAYER via9 ....... TOTAL Original Geometry Count = 0
---------------------------------------------------------------------
------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK Well.1 ...... TOTAL Result Count = 0
RULECHECK Well.2 ...... TOTAL Result Count = 0
RULECHECK Well.4 ...... TOTAL Result Count = 0
RULECHECK Poly.1 ...... TOTAL Result Count = 0
RULECHECK Poly.2 ...... TOTAL Result Count = 0
RULECHECK Poly.3 ...... TOTAL Result Count = 0
RULECHECK Poly.4 ...... TOTAL Result Count = 0
RULECHECK Poly.5 ...... TOTAL Result Count = 0
RULECHECK Poly.6 ...... TOTAL Result Count = 0
RULECHECK Active.1 .... TOTAL Result Count = 0
RULECHECK Active.2 .... TOTAL Result Count = 0
RULECHECK Active.3 .... TOTAL Result Count = 0
RULECHECK Active.4 .... TOTAL Result Count = 0
RULECHECK Implant.1 ... TOTAL Result Count = 0
RULECHECK Implant.2 ... TOTAL Result Count = 0
RULECHECK Implant.3 ... TOTAL Result Count = 0
RULECHECK Implant.4 ... TOTAL Result Count = 0
RULECHECK Implant.6 ... TOTAL Result Count = 0
RULECHECK Contact.1 ... TOTAL Result Count = 0
RULECHECK Contact.2 ... TOTAL Result Count = 0
RULECHECK Contact.3 ... TOTAL Result Count = 0
RULECHECK Contact.4 ... TOTAL Result Count = 0
RULECHECK Contact.5 ... TOTAL Result Count = 0
RULECHECK Contact.6 ... TOTAL Result Count = 0
RULECHECK Metal1.1 .... TOTAL Result Count = 0
RULECHECK Metal1.2 .... TOTAL Result Count = 0
RULECHECK Metal1.3 .... TOTAL Result Count = 0
RULECHECK Metal1.4 .... TOTAL Result Count = 0
```

```
RULECHECK Via1.1 ..... TOTAL Result Count = 0
RULECHECK Via1.2 ..... TOTAL Result Count = 0
RULECHECK Via1.3 ..... TOTAL Result Count = 0
RULECHECK Via1.4 ..... TOTAL Result Count = 0
RULECHECK Metal2.1 .... TOTAL Result Count = 0
RULECHECK Metal2.2 .... TOTAL Result Count = 0
RULECHECK Metal2.3 .... TOTAL Result Count = 0
RULECHECK Metal2.4 .... TOTAL Result Count = 0
RULECHECK Via2.1 ..... TOTAL Result Count = 0
RULECHECK Via2.2 ..... TOTAL Result Count = 0
RULECHECK Via2.3 ..... TOTAL Result Count = 0
RULECHECK Via2.4 ..... TOTAL Result Count = 0
RULECHECK Metal3.1 .... TOTAL Result Count = 0
RULECHECK Metal3.2 .... TOTAL Result Count = 0
RULECHECK Metal3.3 .... TOTAL Result Count = 0
RULECHECK Metal3.4 .... TOTAL Result Count = 0
RULECHECK Via3.1 ..... TOTAL Result Count = 0
RULECHECK Via3.2 ..... TOTAL Result Count = 0
RULECHECK Via3.3 ..... TOTAL Result Count = 0
RULECHECK Via3.4 ..... TOTAL Result Count = 0
RULECHECK Metal4.1 .... TOTAL Result Count = 0
RULECHECK Metal4.2 .... TOTAL Result Count = 0
RULECHECK Metal4.3 .... TOTAL Result Count = 0
RULECHECK Via4.1 ..... TOTAL Result Count = 0
RULECHECK Via4.2 ..... TOTAL Result Count = 0
RULECHECK Via4.3 ..... TOTAL Result Count = 0
RULECHECK Via4.4 ..... TOTAL Result Count = 0
RULECHECK Metal5.1 .... TOTAL Result Count = 0
RULECHECK Metal5.2 .... TOTAL Result Count = 0
RULECHECK Metal5.3 .... TOTAL Result Count = 0
RULECHECK Via5.1 ..... TOTAL Result Count = 0
RULECHECK Via5.2 ..... TOTAL Result Count = 0
RULECHECK Via5.3 ..... TOTAL Result Count = 0
RULECHECK Via5.4 ..... TOTAL Result Count = 0
RULECHECK Metal6.1 .... TOTAL Result Count = 0
RULECHECK Metal6.2 .... TOTAL Result Count = 0
RULECHECK Metal6.3 .... TOTAL Result Count = 0
RULECHECK Via6.1 ..... TOTAL Result Count = 0
RULECHECK Via6.2 ..... TOTAL Result Count = 0
RULECHECK Via6.3 ..... TOTAL Result Count = 0
RULECHECK Via6.4 ..... TOTAL Result Count = 0
RULECHECK Metal7.1 .... TOTAL Result Count = 0
RULECHECK Metal7.2 .... TOTAL Result Count = 0
RULECHECK Metal7.3 .... TOTAL Result Count = 0
RULECHECK Via7.1 ..... TOTAL Result Count = 0
RULECHECK Via7.2 ..... TOTAL Result Count = 0
RULECHECK Via7.3 ..... TOTAL Result Count = 0
RULECHECK Via7.4 ..... TOTAL Result Count = 0
RULECHECK Metal8.1 .... TOTAL Result Count = 0
RULECHECK Metal8.2 .... TOTAL Result Count = 0
RULECHECK Metal8.3 .... TOTAL Result Count = 0
RULECHECK Via8.1 ..... TOTAL Result Count = 0
```

```
RULECHECK Via8.2 ..... TOTAL Result Count = 0
RULECHECK Via8.3 ..... TOTAL Result Count = 0
RULECHECK Via8.4 ..... TOTAL Result Count = 0
RULECHECK Metal9.1 .... TOTAL Result Count = 0
RULECHECK Metal9.2 .... TOTAL Result Count = 0
RULECHECK Metal9.3 .... TOTAL Result Count = 0
RULECHECK Via9.1 ..... TOTAL Result Count = 0
RULECHECK Via9.2 ..... TOTAL Result Count = 0
RULECHECK Via9.3 ..... TOTAL Result Count = 0
RULECHECK Via9.4 ..... TOTAL Result Count = 0
RULECHECK Metal10.1 ... TOTAL Result Count = 0
RULECHECK Metal10.2 ... TOTAL Result Count = 0
RULECHECK Metal10.3 ... TOTAL Result Count = 0
RULECHECK Metal1.5 .... TOTAL Result Count = 0
RULECHECK Metal1.6 .... TOTAL Result Count = 0
RULECHECK Metal1.7 .... TOTAL Result Count = 0
RULECHECK Metal1.8 .... TOTAL Result Count = 0
RULECHECK Metal1.9 .... TOTAL Result Count = 0
RULECHECK Metal2.5 .... TOTAL Result Count = 0
RULECHECK Metal2.6 .... TOTAL Result Count = 0
RULECHECK Metal2.7 .... TOTAL Result Count = 0
RULECHECK Metal2.8 .... TOTAL Result Count = 0
RULECHECK Metal2.9 .... TOTAL Result Count = 0
RULECHECK Metal3.5 .... TOTAL Result Count = 0
RULECHECK Metal3.6 .... TOTAL Result Count = 0
RULECHECK Metal3.7 .... TOTAL Result Count = 0
RULECHECK Metal3.8 .... TOTAL Result Count = 0
RULECHECK Metal3.9 .... TOTAL Result Count = 0
RULECHECK Metal4.5 .... TOTAL Result Count = 0
RULECHECK Metal4.6 .... TOTAL Result Count = 0
RULECHECK Metal4.7 .... TOTAL Result Count = 0
RULECHECK Metal4.8 .... TOTAL Result Count = 0
RULECHECK Metal5.5 .... TOTAL Result Count = 0
RULECHECK Metal5.6 .... TOTAL Result Count = 0
RULECHECK Metal5.7 .... TOTAL Result Count = 0
RULECHECK Metal5.8 .... TOTAL Result Count = 0
RULECHECK Metal6.5 .... TOTAL Result Count = 0
RULECHECK Metal6.6 .... TOTAL Result Count = 0
RULECHECK Metal6.7 .... TOTAL Result Count = 0
RULECHECK Metal6.8 .... TOTAL Result Count = 0
RULECHECK Metal7.5 .... TOTAL Result Count = 0
RULECHECK Metal7.6 .... TOTAL Result Count = 0
RULECHECK Metal7.7 .... TOTAL Result Count = 0
RULECHECK Metal8.5 .... TOTAL Result Count = 0
RULECHECK Metal8.6 .... TOTAL Result Count = 0
RULECHECK Metal8.7 .... TOTAL Result Count = 0
RULECHECK Metal9.5 .... TOTAL Result Count = 0
RULECHECK Metal9.6 .... TOTAL Result Count = 0
RULECHECK Metal10.5 ... TOTAL Result Count = 0
RULECHECK Metal10.6 ... TOTAL Result Count = 0
RULECHECK Grid.1 ..... TOTAL Result Count = 0
RULECHECK Grid.2 ..... TOTAL Result Count = 0
```

```
RULECHECK Grid.3 ..... TOTAL Result Count = 0
RULECHECK Grid.4 ..... TOTAL Result Count = 0
RULECHECK Grid.5 ..... TOTAL Result Count = 0
RULECHECK Grid.6 ..... TOTAL Result Count = 0
RULECHECK Grid.7 ..... TOTAL Result Count = 0
RULECHECK Grid.8 ..... TOTAL Result Count = 0
RULECHECK Grid.9 ..... TOTAL Result Count = 0
RULECHECK Grid.10 ..... TOTAL Result Count = 0
RULECHECK Grid.11 ..... TOTAL Result Count = 0
RULECHECK Grid.12 ..... TOTAL Result Count = 0
RULECHECK Grid.13 ..... TOTAL Result Count = 0
RULECHECK Grid.14 ..... TOTAL Result Count = 0
RULECHECK Grid.15 ..... TOTAL Result Count = 0
RULECHECK Grid.16 ..... TOTAL Result Count = 0
RULECHECK Grid.17 ..... TOTAL Result Count = 0
RULECHECK Grid.18 ..... TOTAL Result Count = 0
RULECHECK Grid.19 ..... TOTAL Result Count = 0
RULECHECK Grid.20 ..... TOTAL Result Count = 0
RULECHECK Grid.21 ..... TOTAL Result Count = 0
RULECHECK Grid.22 ..... TOTAL Result Count = 0
RULECHECK Grid.23 ..... TOTAL Result Count = 0
RULECHECK Grid.24 ..... TOTAL Result Count = 0
RULECHECK Grid.25 ..... TOTAL Result Count = 0
RULECHECK Grid.26 ..... TOTAL Result Count = 0
------------------------------------------------------------------------
------------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 266
TOTAL DRC RuleChecks Executed:   156
TOTAL DRC Results Generated:     0
```

FO1

```
========================================================================
============
=== CALIBRE::DRC-F SUMMARY REPORT
===
Execution Date/Time:       Mon Mar 13 21:18:11 2017
Calibre Version:           v2013.2_35.25    Wed Jul 3 15:43:57 PDT
2013
Rule File Pathname:        /u/haranadh/cadence/DRC-
files/_calibreDRC.rul_
```

```
Rule File Title:
Layout System:              GDS
Layout Path(s):             AOI_Custom_FO1.calibre.db
Layout Primary Cell:        AOI_Custom_FO1
Current Directory:          /u/haranadh/cadence/DRC-files
User Name:                  haranadh
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:    4096
DRC Results Database:       AOI_Custom_FO1.drc.results (ASCII)
Layout Depth:               ALL
Text Depth:                 PRIMARY
Summary Report File:        AOI_Custom_FO1.drc.summary (REPLACE)
Geometry Flagging:          ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID
= NO
                            NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:          COMMENT TEXT + RULE FILE INFORMATION
Layers:                     MEMORY-BASED
Keep Empty Checks:          YES
--------------------------------------------------------------------
------------
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------
------------
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ...... TOTAL Original Geometry Count = 10
LAYER nwell ...... TOTAL Original Geometry Count = 10
LAYER active ..... TOTAL Original Geometry Count = 114
LAYER poly ....... TOTAL Original Geometry Count = 72
LAYER pimplant ... TOTAL Original Geometry Count = 9
LAYER nimplant ... TOTAL Original Geometry Count = 9
LAYER vth ........ TOTAL Original Geometry Count = 0
LAYER vtg ........ TOTAL Original Geometry Count = 0
LAYER metal1 ..... TOTAL Original Geometry Count = 75
LAYER metal2 ..... TOTAL Original Geometry Count = 0
LAYER metal3 ..... TOTAL Original Geometry Count = 0
LAYER metal4 ..... TOTAL Original Geometry Count = 0
LAYER metal5 ..... TOTAL Original Geometry Count = 0
LAYER metal6 ..... TOTAL Original Geometry Count = 0
LAYER metal7 ..... TOTAL Original Geometry Count = 0
LAYER metal8 ..... TOTAL Original Geometry Count = 0
LAYER metal9 ..... TOTAL Original Geometry Count = 0
LAYER metal10 .... TOTAL Original Geometry Count = 0
LAYER contact .... TOTAL Original Geometry Count = 96
LAYER via1 ....... TOTAL Original Geometry Count = 0
LAYER via2 ....... TOTAL Original Geometry Count = 0
LAYER via3 ....... TOTAL Original Geometry Count = 0
LAYER via4 ....... TOTAL Original Geometry Count = 0
LAYER via5 ....... TOTAL Original Geometry Count = 0
LAYER via6 ....... TOTAL Original Geometry Count = 0
```

```
LAYER via7 ....... TOTAL Original Geometry Count = 0
LAYER via8 ....... TOTAL Original Geometry Count = 0
LAYER via9 ....... TOTAL Original Geometry Count = 0
---------------------------------------------------------------------
------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK Well.1 ..... TOTAL Result Count = 0
RULECHECK Well.2 ..... TOTAL Result Count = 0
RULECHECK Well.4 ..... TOTAL Result Count = 0
RULECHECK Poly.1 ..... TOTAL Result Count = 0
RULECHECK Poly.2 ..... TOTAL Result Count = 0
RULECHECK Poly.3 ..... TOTAL Result Count = 0
RULECHECK Poly.4 ..... TOTAL Result Count = 0
RULECHECK Poly.5 ..... TOTAL Result Count = 0
RULECHECK Poly.6 ..... TOTAL Result Count = 0
RULECHECK Active.1 .... TOTAL Result Count = 0
RULECHECK Active.2 .... TOTAL Result Count = 0
RULECHECK Active.3 .... TOTAL Result Count = 0
RULECHECK Active.4 .... TOTAL Result Count = 0
RULECHECK Implant.1 ... TOTAL Result Count = 0
RULECHECK Implant.2 ... TOTAL Result Count = 0
RULECHECK Implant.3 ... TOTAL Result Count = 0
RULECHECK Implant.4 ... TOTAL Result Count = 0
RULECHECK Implant.6 ... TOTAL Result Count = 0
RULECHECK Contact.1 ... TOTAL Result Count = 0
RULECHECK Contact.2 ... TOTAL Result Count = 0
RULECHECK Contact.3 ... TOTAL Result Count = 0
RULECHECK Contact.4 ... TOTAL Result Count = 0
RULECHECK Contact.5 ... TOTAL Result Count = 0
RULECHECK Contact.6 ... TOTAL Result Count = 0
RULECHECK Metal1.1 .... TOTAL Result Count = 0
RULECHECK Metal1.2 .... TOTAL Result Count = 0
RULECHECK Metal1.3 .... TOTAL Result Count = 0
RULECHECK Metal1.4 .... TOTAL Result Count = 0
RULECHECK Via1.1 ..... TOTAL Result Count = 0
RULECHECK Via1.2 ..... TOTAL Result Count = 0
RULECHECK Via1.3 ..... TOTAL Result Count = 0
RULECHECK Via1.4 ..... TOTAL Result Count = 0
RULECHECK Metal2.1 .... TOTAL Result Count = 0
RULECHECK Metal2.2 .... TOTAL Result Count = 0
RULECHECK Metal2.3 .... TOTAL Result Count = 0
RULECHECK Metal2.4 .... TOTAL Result Count = 0
RULECHECK Via2.1 ..... TOTAL Result Count = 0
RULECHECK Via2.2 ..... TOTAL Result Count = 0
RULECHECK Via2.3 ..... TOTAL Result Count = 0
RULECHECK Via2.4 ..... TOTAL Result Count = 0
RULECHECK Metal3.1 .... TOTAL Result Count = 0
RULECHECK Metal3.2 .... TOTAL Result Count = 0
RULECHECK Metal3.3 .... TOTAL Result Count = 0
RULECHECK Metal3.4 .... TOTAL Result Count = 0
RULECHECK Via3.1 ..... TOTAL Result Count = 0
```

```
RULECHECK Via3.2 ..... TOTAL Result Count = 0
RULECHECK Via3.3 ..... TOTAL Result Count = 0
RULECHECK Via3.4 ..... TOTAL Result Count = 0
RULECHECK Metal4.1 .... TOTAL Result Count = 0
RULECHECK Metal4.2 .... TOTAL Result Count = 0
RULECHECK Metal4.3 .... TOTAL Result Count = 0
RULECHECK Via4.1 ..... TOTAL Result Count = 0
RULECHECK Via4.2 ..... TOTAL Result Count = 0
RULECHECK Via4.3 ..... TOTAL Result Count = 0
RULECHECK Via4.4 ..... TOTAL Result Count = 0
RULECHECK Metal5.1 .... TOTAL Result Count = 0
RULECHECK Metal5.2 .... TOTAL Result Count = 0
RULECHECK Metal5.3 .... TOTAL Result Count = 0
RULECHECK Via5.1 ..... TOTAL Result Count = 0
RULECHECK Via5.2 ..... TOTAL Result Count = 0
RULECHECK Via5.3 ..... TOTAL Result Count = 0
RULECHECK Via5.4 ..... TOTAL Result Count = 0
RULECHECK Metal6.1 .... TOTAL Result Count = 0
RULECHECK Metal6.2 .... TOTAL Result Count = 0
RULECHECK Metal6.3 .... TOTAL Result Count = 0
RULECHECK Via6.1 ..... TOTAL Result Count = 0
RULECHECK Via6.2 ..... TOTAL Result Count = 0
RULECHECK Via6.3 ..... TOTAL Result Count = 0
RULECHECK Via6.4 ..... TOTAL Result Count = 0
RULECHECK Metal7.1 .... TOTAL Result Count = 0
RULECHECK Metal7.2 .... TOTAL Result Count = 0
RULECHECK Metal7.3 .... TOTAL Result Count = 0
RULECHECK Via7.1 ..... TOTAL Result Count = 0
RULECHECK Via7.2 ..... TOTAL Result Count = 0
RULECHECK Via7.3 ..... TOTAL Result Count = 0
RULECHECK Via7.4 ..... TOTAL Result Count = 0
RULECHECK Metal8.1 .... TOTAL Result Count = 0
RULECHECK Metal8.2 .... TOTAL Result Count = 0
RULECHECK Metal8.3 .... TOTAL Result Count = 0
RULECHECK Via8.1 ..... TOTAL Result Count = 0
RULECHECK Via8.2 ..... TOTAL Result Count = 0
RULECHECK Via8.3 ..... TOTAL Result Count = 0
RULECHECK Via8.4 ..... TOTAL Result Count = 0
RULECHECK Metal9.1 .... TOTAL Result Count = 0
RULECHECK Metal9.2 .... TOTAL Result Count = 0
RULECHECK Metal9.3 .... TOTAL Result Count = 0
RULECHECK Via9.1 ..... TOTAL Result Count = 0
RULECHECK Via9.2 ..... TOTAL Result Count = 0
RULECHECK Via9.3 ..... TOTAL Result Count = 0
RULECHECK Via9.4 ..... TOTAL Result Count = 0
RULECHECK Metal10.1 ... TOTAL Result Count = 0
RULECHECK Metal10.2 ... TOTAL Result Count = 0
RULECHECK Metal10.3 ... TOTAL Result Count = 0
RULECHECK Metal1.5 .... TOTAL Result Count = 0
RULECHECK Metal1.6 .... TOTAL Result Count = 0
RULECHECK Metal1.7 .... TOTAL Result Count = 0
RULECHECK Metal1.8 .... TOTAL Result Count = 0
```

```
RULECHECK Metal1.9 .... TOTAL Result Count = 0
RULECHECK Metal2.5 .... TOTAL Result Count = 0
RULECHECK Metal2.6 .... TOTAL Result Count = 0
RULECHECK Metal2.7 .... TOTAL Result Count = 0
RULECHECK Metal2.8 .... TOTAL Result Count = 0
RULECHECK Metal2.9 .... TOTAL Result Count = 0
RULECHECK Metal3.5 .... TOTAL Result Count = 0
RULECHECK Metal3.6 .... TOTAL Result Count = 0
RULECHECK Metal3.7 .... TOTAL Result Count = 0
RULECHECK Metal3.8 .... TOTAL Result Count = 0
RULECHECK Metal3.9 .... TOTAL Result Count = 0
RULECHECK Metal4.5 .... TOTAL Result Count = 0
RULECHECK Metal4.6 .... TOTAL Result Count = 0
RULECHECK Metal4.7 .... TOTAL Result Count = 0
RULECHECK Metal4.8 .... TOTAL Result Count = 0
RULECHECK Metal5.5 .... TOTAL Result Count = 0
RULECHECK Metal5.6 .... TOTAL Result Count = 0
RULECHECK Metal5.7 .... TOTAL Result Count = 0
RULECHECK Metal5.8 .... TOTAL Result Count = 0
RULECHECK Metal6.5 .... TOTAL Result Count = 0
RULECHECK Metal6.6 .... TOTAL Result Count = 0
RULECHECK Metal6.7 .... TOTAL Result Count = 0
RULECHECK Metal6.8 .... TOTAL Result Count = 0
RULECHECK Metal7.5 .... TOTAL Result Count = 0
RULECHECK Metal7.6 .... TOTAL Result Count = 0
RULECHECK Metal7.7 .... TOTAL Result Count = 0
RULECHECK Metal8.5 .... TOTAL Result Count = 0
RULECHECK Metal8.6 .... TOTAL Result Count = 0
RULECHECK Metal8.7 .... TOTAL Result Count = 0
RULECHECK Metal9.5 .... TOTAL Result Count = 0
RULECHECK Metal9.6 .... TOTAL Result Count = 0
RULECHECK Metal10.5 ... TOTAL Result Count = 0
RULECHECK Metal10.6 ... TOTAL Result Count = 0
RULECHECK Grid.1 ...... TOTAL Result Count = 0
RULECHECK Grid.2 ...... TOTAL Result Count = 0
RULECHECK Grid.3 ...... TOTAL Result Count = 0
RULECHECK Grid.4 ...... TOTAL Result Count = 0
RULECHECK Grid.5 ...... TOTAL Result Count = 0
RULECHECK Grid.6 ...... TOTAL Result Count = 0
RULECHECK Grid.7 ...... TOTAL Result Count = 0
RULECHECK Grid.8 ...... TOTAL Result Count = 0
RULECHECK Grid.9 ...... TOTAL Result Count = 0
RULECHECK Grid.10 ..... TOTAL Result Count = 0
RULECHECK Grid.11 ..... TOTAL Result Count = 0
RULECHECK Grid.12 ..... TOTAL Result Count = 0
RULECHECK Grid.13 ..... TOTAL Result Count = 0
RULECHECK Grid.14 ..... TOTAL Result Count = 0
RULECHECK Grid.15 ..... TOTAL Result Count = 0
RULECHECK Grid.16 ..... TOTAL Result Count = 0
RULECHECK Grid.17 ..... TOTAL Result Count = 0
RULECHECK Grid.18 ..... TOTAL Result Count = 0
RULECHECK Grid.19 ..... TOTAL Result Count = 0
```

```
RULECHECK Grid.20 ..... TOTAL Result Count = 0
RULECHECK Grid.21 ..... TOTAL Result Count = 0
RULECHECK Grid.22 ..... TOTAL Result Count = 0
RULECHECK Grid.23 ..... TOTAL Result Count = 0
RULECHECK Grid.24 ..... TOTAL Result Count = 0
RULECHECK Grid.25 ..... TOTAL Result Count = 0
RULECHECK Grid.26 ..... TOTAL Result Count = 0
------------------------------------------------------------------------
------------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 395
TOTAL DRC RuleChecks Executed:   156
TOTAL DRC Results Generated:     0
```

FO2

```
========================================================================
============
=== CALIBRE::DRC-F SUMMARY REPORT
===
Execution Date/Time:       Mon Mar 13 21:30:53 2017
Calibre Version:           v2013.2_35.25    Wed Jul 3 15:43:57 PDT
2013
Rule File Pathname:        /u/haranadh/cadence/DRC-
files/_calibreDRC.rul_
Rule File Title:
Layout System:             GDS
Layout Path(s):            AOI_Custom_FO2.calibre.db
Layout Primary Cell:       AOI_Custom_FO2
Current Directory:         /u/haranadh/cadence/DRC-files
User Name:                 haranadh
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      AOI_Custom_FO2.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       AOI_Custom_FO2.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID
= NO
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
```

```
CheckText Mapping:          COMMENT TEXT + RULE FILE INFORMATION
Layers:                     MEMORY-BASED
Keep Empty Checks:          YES
--------------------------------------------------------------------
------------
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------
------------
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ...... TOTAL Original Geometry Count = 13
LAYER nwell ...... TOTAL Original Geometry Count = 13
LAYER active ..... TOTAL Original Geometry Count = 156
LAYER poly ....... TOTAL Original Geometry Count = 99
LAYER pimplant ... TOTAL Original Geometry Count = 12
LAYER nimplant ... TOTAL Original Geometry Count = 12
LAYER vth ........ TOTAL Original Geometry Count = 0
LAYER vtg ........ TOTAL Original Geometry Count = 0
LAYER metal1 ..... TOTAL Original Geometry Count = 104
LAYER metal2 ..... TOTAL Original Geometry Count = 3
LAYER metal3 ..... TOTAL Original Geometry Count = 0
LAYER metal4 ..... TOTAL Original Geometry Count = 0
LAYER metal5 ..... TOTAL Original Geometry Count = 0
LAYER metal6 ..... TOTAL Original Geometry Count = 0
LAYER metal7 ..... TOTAL Original Geometry Count = 0
LAYER metal8 ..... TOTAL Original Geometry Count = 0
LAYER metal9 ..... TOTAL Original Geometry Count = 0
LAYER metal10 .... TOTAL Original Geometry Count = 0
LAYER contact .... TOTAL Original Geometry Count = 117
LAYER via1 ....... TOTAL Original Geometry Count = 2
LAYER via2 ....... TOTAL Original Geometry Count = 0
LAYER via3 ....... TOTAL Original Geometry Count = 0
LAYER via4 ....... TOTAL Original Geometry Count = 0
LAYER via5 ....... TOTAL Original Geometry Count = 0
LAYER via6 ....... TOTAL Original Geometry Count = 0
LAYER via7 ....... TOTAL Original Geometry Count = 0
LAYER via8 ....... TOTAL Original Geometry Count = 0
LAYER via9 ....... TOTAL Original Geometry Count = 0
--------------------------------------------------------------------
------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK Well.1 ...... TOTAL Result Count = 0
RULECHECK Well.2 ...... TOTAL Result Count = 0
RULECHECK Well.4 ...... TOTAL Result Count = 0
RULECHECK Poly.1 ...... TOTAL Result Count = 0
RULECHECK Poly.2 ...... TOTAL Result Count = 0
RULECHECK Poly.3 ...... TOTAL Result Count = 0
RULECHECK Poly.4 ...... TOTAL Result Count = 0
RULECHECK Poly.5 ...... TOTAL Result Count = 0
RULECHECK Poly.6 ...... TOTAL Result Count = 0
```

```
RULECHECK Active.1 .... TOTAL Result Count = 0
RULECHECK Active.2 .... TOTAL Result Count = 0
RULECHECK Active.3 .... TOTAL Result Count = 0
RULECHECK Active.4 .... TOTAL Result Count = 0
RULECHECK Implant.1 ... TOTAL Result Count = 0
RULECHECK Implant.2 ... TOTAL Result Count = 0
RULECHECK Implant.3 ... TOTAL Result Count = 0
RULECHECK Implant.4 ... TOTAL Result Count = 0
RULECHECK Implant.6 ... TOTAL Result Count = 0
RULECHECK Contact.1 ... TOTAL Result Count = 0
RULECHECK Contact.2 ... TOTAL Result Count = 0
RULECHECK Contact.3 ... TOTAL Result Count = 0
RULECHECK Contact.4 ... TOTAL Result Count = 0
RULECHECK Contact.5 ... TOTAL Result Count = 0
RULECHECK Contact.6 ... TOTAL Result Count = 0
RULECHECK Metal1.1 .... TOTAL Result Count = 0
RULECHECK Metal1.2 .... TOTAL Result Count = 0
RULECHECK Metal1.3 .... TOTAL Result Count = 0
RULECHECK Metal1.4 .... TOTAL Result Count = 0
RULECHECK Via1.1 ...... TOTAL Result Count = 0
RULECHECK Via1.2 ...... TOTAL Result Count = 0
RULECHECK Via1.3 ...... TOTAL Result Count = 0
RULECHECK Via1.4 ...... TOTAL Result Count = 0
RULECHECK Metal2.1 .... TOTAL Result Count = 0
RULECHECK Metal2.2 .... TOTAL Result Count = 0
RULECHECK Metal2.3 .... TOTAL Result Count = 0
RULECHECK Metal2.4 .... TOTAL Result Count = 0
RULECHECK Via2.1 ...... TOTAL Result Count = 0
RULECHECK Via2.2 ...... TOTAL Result Count = 0
RULECHECK Via2.3 ...... TOTAL Result Count = 0
RULECHECK Via2.4 ...... TOTAL Result Count = 0
RULECHECK Metal3.1 .... TOTAL Result Count = 0
RULECHECK Metal3.2 .... TOTAL Result Count = 0
RULECHECK Metal3.3 .... TOTAL Result Count = 0
RULECHECK Metal3.4 .... TOTAL Result Count = 0
RULECHECK Via3.1 ...... TOTAL Result Count = 0
RULECHECK Via3.2 ...... TOTAL Result Count = 0
RULECHECK Via3.3 ...... TOTAL Result Count = 0
RULECHECK Via3.4 ...... TOTAL Result Count = 0
RULECHECK Metal4.1 .... TOTAL Result Count = 0
RULECHECK Metal4.2 .... TOTAL Result Count = 0
RULECHECK Metal4.3 .... TOTAL Result Count = 0
RULECHECK Via4.1 ...... TOTAL Result Count = 0
RULECHECK Via4.2 ...... TOTAL Result Count = 0
RULECHECK Via4.3 ...... TOTAL Result Count = 0
RULECHECK Via4.4 ...... TOTAL Result Count = 0
RULECHECK Metal5.1 .... TOTAL Result Count = 0
RULECHECK Metal5.2 .... TOTAL Result Count = 0
RULECHECK Metal5.3 .... TOTAL Result Count = 0
RULECHECK Via5.1 ...... TOTAL Result Count = 0
RULECHECK Via5.2 ...... TOTAL Result Count = 0
RULECHECK Via5.3 ...... TOTAL Result Count = 0
```

```
RULECHECK Via5.4 ..... TOTAL Result Count = 0
RULECHECK Metal6.1 .... TOTAL Result Count = 0
RULECHECK Metal6.2 .... TOTAL Result Count = 0
RULECHECK Metal6.3 .... TOTAL Result Count = 0
RULECHECK Via6.1 ..... TOTAL Result Count = 0
RULECHECK Via6.2 ..... TOTAL Result Count = 0
RULECHECK Via6.3 ..... TOTAL Result Count = 0
RULECHECK Via6.4 ..... TOTAL Result Count = 0
RULECHECK Metal7.1 .... TOTAL Result Count = 0
RULECHECK Metal7.2 .... TOTAL Result Count = 0
RULECHECK Metal7.3 .... TOTAL Result Count = 0
RULECHECK Via7.1 ..... TOTAL Result Count = 0
RULECHECK Via7.2 ..... TOTAL Result Count = 0
RULECHECK Via7.3 ..... TOTAL Result Count = 0
RULECHECK Via7.4 ..... TOTAL Result Count = 0
RULECHECK Metal8.1 .... TOTAL Result Count = 0
RULECHECK Metal8.2 .... TOTAL Result Count = 0
RULECHECK Metal8.3 .... TOTAL Result Count = 0
RULECHECK Via8.1 ..... TOTAL Result Count = 0
RULECHECK Via8.2 ..... TOTAL Result Count = 0
RULECHECK Via8.3 ..... TOTAL Result Count = 0
RULECHECK Via8.4 ..... TOTAL Result Count = 0
RULECHECK Metal9.1 .... TOTAL Result Count = 0
RULECHECK Metal9.2 .... TOTAL Result Count = 0
RULECHECK Metal9.3 .... TOTAL Result Count = 0
RULECHECK Via9.1 ..... TOTAL Result Count = 0
RULECHECK Via9.2 ..... TOTAL Result Count = 0
RULECHECK Via9.3 ..... TOTAL Result Count = 0
RULECHECK Via9.4 ..... TOTAL Result Count = 0
RULECHECK Metal10.1 ... TOTAL Result Count = 0
RULECHECK Metal10.2 ... TOTAL Result Count = 0
RULECHECK Metal10.3 ... TOTAL Result Count = 0
RULECHECK Metal1.5 .... TOTAL Result Count = 0
RULECHECK Metal1.6 .... TOTAL Result Count = 0
RULECHECK Metal1.7 .... TOTAL Result Count = 0
RULECHECK Metal1.8 .... TOTAL Result Count = 0
RULECHECK Metal1.9 .... TOTAL Result Count = 0
RULECHECK Metal2.5 .... TOTAL Result Count = 0
RULECHECK Metal2.6 .... TOTAL Result Count = 0
RULECHECK Metal2.7 .... TOTAL Result Count = 0
RULECHECK Metal2.8 .... TOTAL Result Count = 0
RULECHECK Metal2.9 .... TOTAL Result Count = 0
RULECHECK Metal3.5 .... TOTAL Result Count = 0
RULECHECK Metal3.6 .... TOTAL Result Count = 0
RULECHECK Metal3.7 .... TOTAL Result Count = 0
RULECHECK Metal3.8 .... TOTAL Result Count = 0
RULECHECK Metal3.9 .... TOTAL Result Count = 0
RULECHECK Metal4.5 .... TOTAL Result Count = 0
RULECHECK Metal4.6 .... TOTAL Result Count = 0
RULECHECK Metal4.7 .... TOTAL Result Count = 0
RULECHECK Metal4.8 .... TOTAL Result Count = 0
RULECHECK Metal5.5 .... TOTAL Result Count = 0
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RULECHECK Metal5.6 .... TOTAL Result Count = 0
RULECHECK Metal5.7 .... TOTAL Result Count = 0
RULECHECK Metal5.8 .... TOTAL Result Count = 0
RULECHECK Metal6.5 .... TOTAL Result Count = 0
RULECHECK Metal6.6 .... TOTAL Result Count = 0
RULECHECK Metal6.7 .... TOTAL Result Count = 0
RULECHECK Metal6.8 .... TOTAL Result Count = 0
RULECHECK Metal7.5 .... TOTAL Result Count = 0
RULECHECK Metal7.6 .... TOTAL Result Count = 0
RULECHECK Metal7.7 .... TOTAL Result Count = 0
RULECHECK Metal8.5 .... TOTAL Result Count = 0
RULECHECK Metal8.6 .... TOTAL Result Count = 0
RULECHECK Metal8.7 .... TOTAL Result Count = 0
RULECHECK Metal9.5 .... TOTAL Result Count = 0
RULECHECK Metal9.6 .... TOTAL Result Count = 0
RULECHECK Metal10.5 ... TOTAL Result Count = 0
RULECHECK Metal10.6 ... TOTAL Result Count = 0
RULECHECK Grid.1 ...... TOTAL Result Count = 0
RULECHECK Grid.2 ...... TOTAL Result Count = 0
RULECHECK Grid.3 ...... TOTAL Result Count = 0
RULECHECK Grid.4 ...... TOTAL Result Count = 0
RULECHECK Grid.5 ...... TOTAL Result Count = 0
RULECHECK Grid.6 ...... TOTAL Result Count = 0
RULECHECK Grid.7 ...... TOTAL Result Count = 0
RULECHECK Grid.8 ...... TOTAL Result Count = 0
RULECHECK Grid.9 ...... TOTAL Result Count = 0
RULECHECK Grid.10 ..... TOTAL Result Count = 0
RULECHECK Grid.11 ..... TOTAL Result Count = 0
RULECHECK Grid.12 ..... TOTAL Result Count = 0
RULECHECK Grid.13 ..... TOTAL Result Count = 0
RULECHECK Grid.14 ..... TOTAL Result Count = 0
RULECHECK Grid.15 ..... TOTAL Result Count = 0
RULECHECK Grid.16 ..... TOTAL Result Count = 0
RULECHECK Grid.17 ..... TOTAL Result Count = 0
RULECHECK Grid.18 ..... TOTAL Result Count = 0
RULECHECK Grid.19 ..... TOTAL Result Count = 0
RULECHECK Grid.20 ..... TOTAL Result Count = 0
RULECHECK Grid.21 ..... TOTAL Result Count = 0
RULECHECK Grid.22 ..... TOTAL Result Count = 0
RULECHECK Grid.23 ..... TOTAL Result Count = 0
RULECHECK Grid.24 ..... TOTAL Result Count = 0
RULECHECK Grid.25 ..... TOTAL Result Count = 0
RULECHECK Grid.26 ..... TOTAL Result Count = 0
--------------------------------------------------------------------------
------------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 531
TOTAL DRC RuleChecks Executed:   156
TOTAL DRC Results Generated:     0
```

FO4

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================================================================================
============
=== CALIBRE::DRC-F SUMMARY REPORT
===
Execution Date/Time:       Mon Mar 13 21:42:11 2017
Calibre Version:           v2013.2_35.25    Wed Jul 3 15:43:57 PDT
2013
Rule File Pathname:        /u/haranadh/cadence/DRC-
files/_calibreDRC.rul_
Rule File Title:
Layout System:             GDS
Layout Path(s):            AOI_Custom_FO4.calibre.db
Layout Primary Cell:       AOI_Custom_FO4
Current Directory:         /u/haranadh/cadence/DRC-files
User Name:                 haranadh
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      AOI_Custom_FO4.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       AOI_Custom_FO4.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID
= NO
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:         COMMENT TEXT + RULE FILE INFORMATION
Layers:                    MEMORY-BASED
Keep Empty Checks:         YES
--------------------------------------------------------------------------
------------
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------------
------------
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ...... TOTAL Original Geometry Count = 19
LAYER nwell ...... TOTAL Original Geometry Count = 19
LAYER active ..... TOTAL Original Geometry Count = 240
LAYER poly ....... TOTAL Original Geometry Count = 153
LAYER pimplant ... TOTAL Original Geometry Count = 18
LAYER nimplant ... TOTAL Original Geometry Count = 18
LAYER vth ........ TOTAL Original Geometry Count = 0
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LAYER vtg ........ TOTAL Original Geometry Count = 0
LAYER metal1 ..... TOTAL Original Geometry Count = 160
LAYER metal2 ..... TOTAL Original Geometry Count = 5
LAYER metal3 ..... TOTAL Original Geometry Count = 0
LAYER metal4 ..... TOTAL Original Geometry Count = 0
LAYER metal5 ..... TOTAL Original Geometry Count = 0
LAYER metal6 ..... TOTAL Original Geometry Count = 0
LAYER metal7 ..... TOTAL Original Geometry Count = 0
LAYER metal8 ..... TOTAL Original Geometry Count = 0
LAYER metal9 ..... TOTAL Original Geometry Count = 0
LAYER metal10 .... TOTAL Original Geometry Count = 0
LAYER contact .... TOTAL Original Geometry Count = 159
LAYER via1 ....... TOTAL Original Geometry Count = 4
LAYER via2 ....... TOTAL Original Geometry Count = 0
LAYER via3 ....... TOTAL Original Geometry Count = 0
LAYER via4 ....... TOTAL Original Geometry Count = 0
LAYER via5 ....... TOTAL Original Geometry Count = 0
LAYER via6 ....... TOTAL Original Geometry Count = 0
LAYER via7 ....... TOTAL Original Geometry Count = 0
LAYER via8 ....... TOTAL Original Geometry Count = 0
LAYER via9 ....... TOTAL Original Geometry Count = 0
--------------------------------------------------------------------------
------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK Well.1 ...... TOTAL Result Count = 0
RULECHECK Well.2 ...... TOTAL Result Count = 0
RULECHECK Well.4 ...... TOTAL Result Count = 0
RULECHECK Poly.1 ...... TOTAL Result Count = 0
RULECHECK Poly.2 ...... TOTAL Result Count = 0
RULECHECK Poly.3 ...... TOTAL Result Count = 0
RULECHECK Poly.4 ...... TOTAL Result Count = 0
RULECHECK Poly.5 ...... TOTAL Result Count = 0
RULECHECK Poly.6 ...... TOTAL Result Count = 0
RULECHECK Active.1 .... TOTAL Result Count = 0
RULECHECK Active.2 .... TOTAL Result Count = 0
RULECHECK Active.3 .... TOTAL Result Count = 0
RULECHECK Active.4 .... TOTAL Result Count = 0
RULECHECK Implant.1 ... TOTAL Result Count = 0
RULECHECK Implant.2 ... TOTAL Result Count = 0
RULECHECK Implant.3 ... TOTAL Result Count = 0
RULECHECK Implant.4 ... TOTAL Result Count = 0
RULECHECK Implant.6 ... TOTAL Result Count = 0
RULECHECK Contact.1 ... TOTAL Result Count = 0
RULECHECK Contact.2 ... TOTAL Result Count = 0
RULECHECK Contact.3 ... TOTAL Result Count = 0
RULECHECK Contact.4 ... TOTAL Result Count = 0
RULECHECK Contact.5 ... TOTAL Result Count = 0
RULECHECK Contact.6 ... TOTAL Result Count = 0
RULECHECK Metal1.1 .... TOTAL Result Count = 0
RULECHECK Metal1.2 .... TOTAL Result Count = 0
RULECHECK Metal1.3 .... TOTAL Result Count = 0
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RULECHECK Metal1.4 .... TOTAL Result Count = 0
RULECHECK Via1.1 ...... TOTAL Result Count = 0
RULECHECK Via1.2 ...... TOTAL Result Count = 0
RULECHECK Via1.3 ...... TOTAL Result Count = 0
RULECHECK Via1.4 ...... TOTAL Result Count = 0
RULECHECK Metal2.1 .... TOTAL Result Count = 0
RULECHECK Metal2.2 .... TOTAL Result Count = 0
RULECHECK Metal2.3 .... TOTAL Result Count = 0
RULECHECK Metal2.4 .... TOTAL Result Count = 0
RULECHECK Via2.1 ...... TOTAL Result Count = 0
RULECHECK Via2.2 ...... TOTAL Result Count = 0
RULECHECK Via2.3 ...... TOTAL Result Count = 0
RULECHECK Via2.4 ...... TOTAL Result Count = 0
RULECHECK Metal3.1 .... TOTAL Result Count = 0
RULECHECK Metal3.2 .... TOTAL Result Count = 0
RULECHECK Metal3.3 .... TOTAL Result Count = 0
RULECHECK Metal3.4 .... TOTAL Result Count = 0
RULECHECK Via3.1 ...... TOTAL Result Count = 0
RULECHECK Via3.2 ...... TOTAL Result Count = 0
RULECHECK Via3.3 ...... TOTAL Result Count = 0
RULECHECK Via3.4 ...... TOTAL Result Count = 0
RULECHECK Metal4.1 .... TOTAL Result Count = 0
RULECHECK Metal4.2 .... TOTAL Result Count = 0
RULECHECK Metal4.3 .... TOTAL Result Count = 0
RULECHECK Via4.1 ...... TOTAL Result Count = 0
RULECHECK Via4.2 ...... TOTAL Result Count = 0
RULECHECK Via4.3 ...... TOTAL Result Count = 0
RULECHECK Via4.4 ...... TOTAL Result Count = 0
RULECHECK Metal5.1 .... TOTAL Result Count = 0
RULECHECK Metal5.2 .... TOTAL Result Count = 0
RULECHECK Metal5.3 .... TOTAL Result Count = 0
RULECHECK Via5.1 ...... TOTAL Result Count = 0
RULECHECK Via5.2 ...... TOTAL Result Count = 0
RULECHECK Via5.3 ...... TOTAL Result Count = 0
RULECHECK Via5.4 ...... TOTAL Result Count = 0
RULECHECK Metal6.1 .... TOTAL Result Count = 0
RULECHECK Metal6.2 .... TOTAL Result Count = 0
RULECHECK Metal6.3 .... TOTAL Result Count = 0
RULECHECK Via6.1 ...... TOTAL Result Count = 0
RULECHECK Via6.2 ...... TOTAL Result Count = 0
RULECHECK Via6.3 ...... TOTAL Result Count = 0
RULECHECK Via6.4 ...... TOTAL Result Count = 0
RULECHECK Metal7.1 .... TOTAL Result Count = 0
RULECHECK Metal7.2 .... TOTAL Result Count = 0
RULECHECK Metal7.3 .... TOTAL Result Count = 0
RULECHECK Via7.1 ...... TOTAL Result Count = 0
RULECHECK Via7.2 ...... TOTAL Result Count = 0
RULECHECK Via7.3 ...... TOTAL Result Count = 0
RULECHECK Via7.4 ...... TOTAL Result Count = 0
RULECHECK Metal8.1 .... TOTAL Result Count = 0
RULECHECK Metal8.2 .... TOTAL Result Count = 0
RULECHECK Metal8.3 .... TOTAL Result Count = 0
```

```
RULECHECK Via8.1 ..... TOTAL Result Count = 0
RULECHECK Via8.2 ..... TOTAL Result Count = 0
RULECHECK Via8.3 ..... TOTAL Result Count = 0
RULECHECK Via8.4 ..... TOTAL Result Count = 0
RULECHECK Metal9.1 .... TOTAL Result Count = 0
RULECHECK Metal9.2 .... TOTAL Result Count = 0
RULECHECK Metal9.3 .... TOTAL Result Count = 0
RULECHECK Via9.1 ..... TOTAL Result Count = 0
RULECHECK Via9.2 ..... TOTAL Result Count = 0
RULECHECK Via9.3 ..... TOTAL Result Count = 0
RULECHECK Via9.4 ..... TOTAL Result Count = 0
RULECHECK Metal10.1 ... TOTAL Result Count = 0
RULECHECK Metal10.2 ... TOTAL Result Count = 0
RULECHECK Metal10.3 ... TOTAL Result Count = 0
RULECHECK Metal1.5 .... TOTAL Result Count = 0
RULECHECK Metal1.6 .... TOTAL Result Count = 0
RULECHECK Metal1.7 .... TOTAL Result Count = 0
RULECHECK Metal1.8 .... TOTAL Result Count = 0
RULECHECK Metal1.9 .... TOTAL Result Count = 0
RULECHECK Metal2.5 .... TOTAL Result Count = 0
RULECHECK Metal2.6 .... TOTAL Result Count = 0
RULECHECK Metal2.7 .... TOTAL Result Count = 0
RULECHECK Metal2.8 .... TOTAL Result Count = 0
RULECHECK Metal2.9 .... TOTAL Result Count = 0
RULECHECK Metal3.5 .... TOTAL Result Count = 0
RULECHECK Metal3.6 .... TOTAL Result Count = 0
RULECHECK Metal3.7 .... TOTAL Result Count = 0
RULECHECK Metal3.8 .... TOTAL Result Count = 0
RULECHECK Metal3.9 .... TOTAL Result Count = 0
RULECHECK Metal4.5 .... TOTAL Result Count = 0
RULECHECK Metal4.6 .... TOTAL Result Count = 0
RULECHECK Metal4.7 .... TOTAL Result Count = 0
RULECHECK Metal4.8 .... TOTAL Result Count = 0
RULECHECK Metal5.5 .... TOTAL Result Count = 0
RULECHECK Metal5.6 .... TOTAL Result Count = 0
RULECHECK Metal5.7 .... TOTAL Result Count = 0
RULECHECK Metal5.8 .... TOTAL Result Count = 0
RULECHECK Metal6.5 .... TOTAL Result Count = 0
RULECHECK Metal6.6 .... TOTAL Result Count = 0
RULECHECK Metal6.7 .... TOTAL Result Count = 0
RULECHECK Metal6.8 .... TOTAL Result Count = 0
RULECHECK Metal7.5 .... TOTAL Result Count = 0
RULECHECK Metal7.6 .... TOTAL Result Count = 0
RULECHECK Metal7.7 .... TOTAL Result Count = 0
RULECHECK Metal8.5 .... TOTAL Result Count = 0
RULECHECK Metal8.6 .... TOTAL Result Count = 0
RULECHECK Metal8.7 .... TOTAL Result Count = 0
RULECHECK Metal9.5 .... TOTAL Result Count = 0
RULECHECK Metal9.6 .... TOTAL Result Count = 0
RULECHECK Metal10.5 ... TOTAL Result Count = 0
RULECHECK Metal10.6 ... TOTAL Result Count = 0
RULECHECK Grid.1 ...... TOTAL Result Count = 0
```

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RULECHECK Grid.2 ..... TOTAL Result Count = 0
RULECHECK Grid.3 ..... TOTAL Result Count = 0
RULECHECK Grid.4 ..... TOTAL Result Count = 0
RULECHECK Grid.5 ..... TOTAL Result Count = 0
RULECHECK Grid.6 ..... TOTAL Result Count = 0
RULECHECK Grid.7 ..... TOTAL Result Count = 0
RULECHECK Grid.8 ..... TOTAL Result Count = 0
RULECHECK Grid.9 ..... TOTAL Result Count = 0
RULECHECK Grid.10 ..... TOTAL Result Count = 0
RULECHECK Grid.11 ..... TOTAL Result Count = 0
RULECHECK Grid.12 ..... TOTAL Result Count = 0
RULECHECK Grid.13 ..... TOTAL Result Count = 0
RULECHECK Grid.14 ..... TOTAL Result Count = 0
RULECHECK Grid.15 ..... TOTAL Result Count = 0
RULECHECK Grid.16 ..... TOTAL Result Count = 0
RULECHECK Grid.17 ..... TOTAL Result Count = 0
RULECHECK Grid.18 ..... TOTAL Result Count = 0
RULECHECK Grid.19 ..... TOTAL Result Count = 0
RULECHECK Grid.20 ..... TOTAL Result Count = 0
RULECHECK Grid.21 ..... TOTAL Result Count = 0
RULECHECK Grid.22 ..... TOTAL Result Count = 0
RULECHECK Grid.23 ..... TOTAL Result Count = 0
RULECHECK Grid.24 ..... TOTAL Result Count = 0
RULECHECK Grid.25 ..... TOTAL Result Count = 0
RULECHECK Grid.26 ..... TOTAL Result Count = 0
---------------------------------------------------------------------
------------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 795
TOTAL DRC RuleChecks Executed:   156
TOTAL DRC Results Generated:     0
```

FO8

```
=====================================================================
============
=== CALIBRE::DRC-F SUMMARY REPORT
===
Execution Date/Time:       Mon Mar 13 21:46:12 2017
Calibre Version:           v2013.2_35.25    Wed Jul 3 15:43:57 PDT
2013
Rule File Pathname:        /u/haranadh/cadence/DRC-
files/_calibreDRC.rul_
Rule File Title:
```

```
Layout System:              GDS
Layout Path(s):             AOI_Custom_FO8.calibre.db
Layout Primary Cell:        AOI_Custom_FO8
Current Directory:          /u/haranadh/cadence/DRC-files
User Name:                  haranadh
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:    4096
DRC Results Database:       AOI_Custom_FO8.drc.results (ASCII)
Layout Depth:               ALL
Text Depth:                 PRIMARY
Summary Report File:        AOI_Custom_FO8.drc.summary (REPLACE)
Geometry Flagging:          ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID
= NO
                            NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:          COMMENT TEXT + RULE FILE INFORMATION
Layers:                     MEMORY-BASED
Keep Empty Checks:          YES
--------------------------------------------------------------------------
------------
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------------
------------
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ...... TOTAL Original Geometry Count = 31
LAYER nwell ...... TOTAL Original Geometry Count = 31
LAYER active ..... TOTAL Original Geometry Count = 408
LAYER poly ....... TOTAL Original Geometry Count = 261
LAYER pimplant ... TOTAL Original Geometry Count = 30
LAYER nimplant ... TOTAL Original Geometry Count = 30
LAYER vth ........ TOTAL Original Geometry Count = 0
LAYER vtg ........ TOTAL Original Geometry Count = 0
LAYER metal1 ..... TOTAL Original Geometry Count = 275
LAYER metal2 ..... TOTAL Original Geometry Count = 15
LAYER metal3 ..... TOTAL Original Geometry Count = 0
LAYER metal4 ..... TOTAL Original Geometry Count = 0
LAYER metal5 ..... TOTAL Original Geometry Count = 0
LAYER metal6 ..... TOTAL Original Geometry Count = 0
LAYER metal7 ..... TOTAL Original Geometry Count = 0
LAYER metal8 ..... TOTAL Original Geometry Count = 0
LAYER metal9 ..... TOTAL Original Geometry Count = 0
LAYER metal10 .... TOTAL Original Geometry Count = 0
LAYER contact .... TOTAL Original Geometry Count = 243
LAYER via1 ....... TOTAL Original Geometry Count = 8
LAYER via2 ....... TOTAL Original Geometry Count = 0
LAYER via3 ....... TOTAL Original Geometry Count = 0
LAYER via4 ....... TOTAL Original Geometry Count = 0
LAYER via5 ....... TOTAL Original Geometry Count = 0
LAYER via6 ....... TOTAL Original Geometry Count = 0
LAYER via7 ....... TOTAL Original Geometry Count = 0
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LAYER via8 ....... TOTAL Original Geometry Count = 0
LAYER via9 ....... TOTAL Original Geometry Count = 0
---------------------------------------------------------------------
------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK Well.1 ...... TOTAL Result Count = 0
RULECHECK Well.2 ...... TOTAL Result Count = 0
RULECHECK Well.4 ...... TOTAL Result Count = 0
RULECHECK Poly.1 ...... TOTAL Result Count = 0
RULECHECK Poly.2 ...... TOTAL Result Count = 0
RULECHECK Poly.3 ...... TOTAL Result Count = 0
RULECHECK Poly.4 ...... TOTAL Result Count = 0
RULECHECK Poly.5 ...... TOTAL Result Count = 0
RULECHECK Poly.6 ...... TOTAL Result Count = 0
RULECHECK Active.1 .... TOTAL Result Count = 0
RULECHECK Active.2 .... TOTAL Result Count = 0
RULECHECK Active.3 .... TOTAL Result Count = 0
RULECHECK Active.4 .... TOTAL Result Count = 0
RULECHECK Implant.1 ... TOTAL Result Count = 0
RULECHECK Implant.2 ... TOTAL Result Count = 0
RULECHECK Implant.3 ... TOTAL Result Count = 0
RULECHECK Implant.4 ... TOTAL Result Count = 0
RULECHECK Implant.6 ... TOTAL Result Count = 0
RULECHECK Contact.1 ... TOTAL Result Count = 0
RULECHECK Contact.2 ... TOTAL Result Count = 0
RULECHECK Contact.3 ... TOTAL Result Count = 0
RULECHECK Contact.4 ... TOTAL Result Count = 0
RULECHECK Contact.5 ... TOTAL Result Count = 0
RULECHECK Contact.6 ... TOTAL Result Count = 0
RULECHECK Metal1.1 .... TOTAL Result Count = 0
RULECHECK Metal1.2 .... TOTAL Result Count = 0
RULECHECK Metal1.3 .... TOTAL Result Count = 0
RULECHECK Metal1.4 .... TOTAL Result Count = 0
RULECHECK Via1.1 ...... TOTAL Result Count = 0
RULECHECK Via1.2 ...... TOTAL Result Count = 0
RULECHECK Via1.3 ...... TOTAL Result Count = 0
RULECHECK Via1.4 ...... TOTAL Result Count = 0
RULECHECK Metal2.1 .... TOTAL Result Count = 0
RULECHECK Metal2.2 .... TOTAL Result Count = 0
RULECHECK Metal2.3 .... TOTAL Result Count = 0
RULECHECK Metal2.4 .... TOTAL Result Count = 0
RULECHECK Via2.1 ...... TOTAL Result Count = 0
RULECHECK Via2.2 ...... TOTAL Result Count = 0
RULECHECK Via2.3 ...... TOTAL Result Count = 0
RULECHECK Via2.4 ...... TOTAL Result Count = 0
RULECHECK Metal3.1 .... TOTAL Result Count = 0
RULECHECK Metal3.2 .... TOTAL Result Count = 0
RULECHECK Metal3.3 .... TOTAL Result Count = 0
RULECHECK Metal3.4 .... TOTAL Result Count = 0
RULECHECK Via3.1 ...... TOTAL Result Count = 0
RULECHECK Via3.2 ...... TOTAL Result Count = 0
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RULECHECK Via3.3 ..... TOTAL Result Count = 0
RULECHECK Via3.4 ..... TOTAL Result Count = 0
RULECHECK Metal4.1 .... TOTAL Result Count = 0
RULECHECK Metal4.2 .... TOTAL Result Count = 0
RULECHECK Metal4.3 .... TOTAL Result Count = 0
RULECHECK Via4.1 ..... TOTAL Result Count = 0
RULECHECK Via4.2 ..... TOTAL Result Count = 0
RULECHECK Via4.3 ..... TOTAL Result Count = 0
RULECHECK Via4.4 ..... TOTAL Result Count = 0
RULECHECK Metal5.1 .... TOTAL Result Count = 0
RULECHECK Metal5.2 .... TOTAL Result Count = 0
RULECHECK Metal5.3 .... TOTAL Result Count = 0
RULECHECK Via5.1 ..... TOTAL Result Count = 0
RULECHECK Via5.2 ..... TOTAL Result Count = 0
RULECHECK Via5.3 ..... TOTAL Result Count = 0
RULECHECK Via5.4 ..... TOTAL Result Count = 0
RULECHECK Metal6.1 .... TOTAL Result Count = 0
RULECHECK Metal6.2 .... TOTAL Result Count = 0
RULECHECK Metal6.3 .... TOTAL Result Count = 0
RULECHECK Via6.1 ..... TOTAL Result Count = 0
RULECHECK Via6.2 ..... TOTAL Result Count = 0
RULECHECK Via6.3 ..... TOTAL Result Count = 0
RULECHECK Via6.4 ..... TOTAL Result Count = 0
RULECHECK Metal7.1 .... TOTAL Result Count = 0
RULECHECK Metal7.2 .... TOTAL Result Count = 0
RULECHECK Metal7.3 .... TOTAL Result Count = 0
RULECHECK Via7.1 ..... TOTAL Result Count = 0
RULECHECK Via7.2 ..... TOTAL Result Count = 0
RULECHECK Via7.3 ..... TOTAL Result Count = 0
RULECHECK Via7.4 ..... TOTAL Result Count = 0
RULECHECK Metal8.1 .... TOTAL Result Count = 0
RULECHECK Metal8.2 .... TOTAL Result Count = 0
RULECHECK Metal8.3 .... TOTAL Result Count = 0
RULECHECK Via8.1 ..... TOTAL Result Count = 0
RULECHECK Via8.2 ..... TOTAL Result Count = 0
RULECHECK Via8.3 ..... TOTAL Result Count = 0
RULECHECK Via8.4 ..... TOTAL Result Count = 0
RULECHECK Metal9.1 .... TOTAL Result Count = 0
RULECHECK Metal9.2 .... TOTAL Result Count = 0
RULECHECK Metal9.3 .... TOTAL Result Count = 0
RULECHECK Via9.1 ..... TOTAL Result Count = 0
RULECHECK Via9.2 ..... TOTAL Result Count = 0
RULECHECK Via9.3 ..... TOTAL Result Count = 0
RULECHECK Via9.4 ..... TOTAL Result Count = 0
RULECHECK Metal10.1 ... TOTAL Result Count = 0
RULECHECK Metal10.2 ... TOTAL Result Count = 0
RULECHECK Metal10.3 ... TOTAL Result Count = 0
RULECHECK Metal1.5 .... TOTAL Result Count = 0
RULECHECK Metal1.6 .... TOTAL Result Count = 0
RULECHECK Metal1.7 .... TOTAL Result Count = 0
RULECHECK Metal1.8 .... TOTAL Result Count = 0
RULECHECK Metal1.9 .... TOTAL Result Count = 0
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RULECHECK Metal2.5 .... TOTAL Result Count = 0
RULECHECK Metal2.6 .... TOTAL Result Count = 0
RULECHECK Metal2.7 .... TOTAL Result Count = 0
RULECHECK Metal2.8 .... TOTAL Result Count = 0
RULECHECK Metal2.9 .... TOTAL Result Count = 0
RULECHECK Metal3.5 .... TOTAL Result Count = 0
RULECHECK Metal3.6 .... TOTAL Result Count = 0
RULECHECK Metal3.7 .... TOTAL Result Count = 0
RULECHECK Metal3.8 .... TOTAL Result Count = 0
RULECHECK Metal3.9 .... TOTAL Result Count = 0
RULECHECK Metal4.5 .... TOTAL Result Count = 0
RULECHECK Metal4.6 .... TOTAL Result Count = 0
RULECHECK Metal4.7 .... TOTAL Result Count = 0
RULECHECK Metal4.8 .... TOTAL Result Count = 0
RULECHECK Metal5.5 .... TOTAL Result Count = 0
RULECHECK Metal5.6 .... TOTAL Result Count = 0
RULECHECK Metal5.7 .... TOTAL Result Count = 0
RULECHECK Metal5.8 .... TOTAL Result Count = 0
RULECHECK Metal6.5 .... TOTAL Result Count = 0
RULECHECK Metal6.6 .... TOTAL Result Count = 0
RULECHECK Metal6.7 .... TOTAL Result Count = 0
RULECHECK Metal6.8 .... TOTAL Result Count = 0
RULECHECK Metal7.5 .... TOTAL Result Count = 0
RULECHECK Metal7.6 .... TOTAL Result Count = 0
RULECHECK Metal7.7 .... TOTAL Result Count = 0
RULECHECK Metal8.5 .... TOTAL Result Count = 0
RULECHECK Metal8.6 .... TOTAL Result Count = 0
RULECHECK Metal8.7 .... TOTAL Result Count = 0
RULECHECK Metal9.5 .... TOTAL Result Count = 0
RULECHECK Metal9.6 .... TOTAL Result Count = 0
RULECHECK Metal10.5 ... TOTAL Result Count = 0
RULECHECK Metal10.6 ... TOTAL Result Count = 0
RULECHECK Grid.1 ...... TOTAL Result Count = 0
RULECHECK Grid.2 ...... TOTAL Result Count = 0
RULECHECK Grid.3 ...... TOTAL Result Count = 0
RULECHECK Grid.4 ...... TOTAL Result Count = 0
RULECHECK Grid.5 ...... TOTAL Result Count = 0
RULECHECK Grid.6 ...... TOTAL Result Count = 0
RULECHECK Grid.7 ...... TOTAL Result Count = 0
RULECHECK Grid.8 ...... TOTAL Result Count = 0
RULECHECK Grid.9 ...... TOTAL Result Count = 0
RULECHECK Grid.10 ..... TOTAL Result Count = 0
RULECHECK Grid.11 ..... TOTAL Result Count = 0
RULECHECK Grid.12 ..... TOTAL Result Count = 0
RULECHECK Grid.13 ..... TOTAL Result Count = 0
RULECHECK Grid.14 ..... TOTAL Result Count = 0
RULECHECK Grid.15 ..... TOTAL Result Count = 0
RULECHECK Grid.16 ..... TOTAL Result Count = 0
RULECHECK Grid.17 ..... TOTAL Result Count = 0
RULECHECK Grid.18 ..... TOTAL Result Count = 0
RULECHECK Grid.19 ..... TOTAL Result Count = 0
RULECHECK Grid.20 ..... TOTAL Result Count = 0
```

```
RULECHECK Grid.21 ..... TOTAL Result Count = 0
RULECHECK Grid.22 ..... TOTAL Result Count = 0
RULECHECK Grid.23 ..... TOTAL Result Count = 0
RULECHECK Grid.24 ..... TOTAL Result Count = 0
RULECHECK Grid.25 ..... TOTAL Result Count = 0
RULECHECK Grid.26 ..... TOTAL Result Count = 0
---------------------------------------------------------------------
------------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 1332
TOTAL DRC RuleChecks Executed:   156
TOTAL DRC Results Generated:     0
```

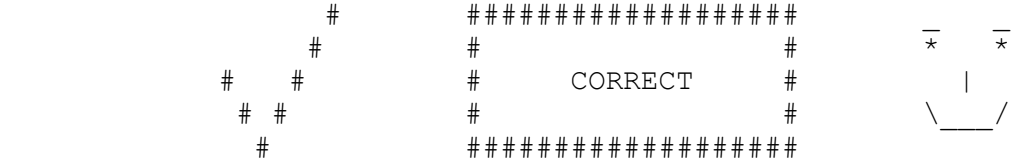
LVS Reports for Full Custom :

FO0

```
                  ################################################
                  ##                                            ##
                  ##         C A L I B R E    S Y S T E M       ##
                  ##                                            ##
                  ##             L V S   R E P O R T            ##
                  ##                                            ##
                  ################################################


REPORT FILE NAME:         AOI_Custom_FO0.lvs.report
LAYOUT NAME:              AOI_Custom_FO0.calibre.db
SOURCE NAME:              /u/haranadh/cadence/LVS-
files/AOI_Custom_FO0.src.net ('AOI_Custom_FO0')
RULE FILE:                /u/haranadh/cadence/LVS-
files/_calibreLVS.rul_
RULE FILE TITLE:          LVS Rule File for FreePDK45
LVS MODE:                 Mask
RULE FILE NAME:           /u/haranadh/cadence/LVS-
files/_calibreLVS.rul_
CREATION TIME:            Mon Mar 13 21:10:53 2017
CURRENT DIRECTORY:        /u/haranadh/cadence/LVS-files
USER NAME:                haranadh
CALIBRE VERSION:          v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013
```

```
*************************************************************************
*************************************
                                OVERALL COMPARISON RESULTS
*************************************************************************
*************************************
```




```
-------------------------------------------------------------------------
----------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------
```

	Layout	Source	Component Type
Nets:	8	8	
Instances:	5	5	mn (4 pins)
	5	5	mp (4 pins)
Total Inst:	10	10	

```
NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------
```

	Layout	Source	Component Type
Nets:	6	6	
Instances:	3	3	mn (4 pins)
	2	2	mp (4 pins)
	1	1	SMN2 (4 pins)
	1	1	SPMP_2_1 (5 pins)
Total Inst:	7	7	

```
*************************************************************************
*************************************
                                    LVS PARAMETERS
```

```
*************************************************************************
**************************************
```

o LVS Setup:

```
   LVS COMPONENT TYPE PROPERTY            element
   LVS COMPONENT SUBTYPE PROPERTY         model
   // LVS PIN NAME PROPERTY
   LVS POWER NAME                         "VDD"
   LVS GROUND NAME                        "VSS" "GROUND"
   LVS CELL SUPPLY                        NO
   LVS RECOGNIZE GATES                    ALL
   LVS IGNORE PORTS                       YES
   LVS CHECK PORT NAMES                   NO
   LVS IGNORE TRIVIAL NAMED PORTS         NO
   LVS BUILTIN DEVICE PIN SWAP            YES
   LVS ALL CAPACITOR PINS SWAPPABLE       NO
   LVS DISCARD PINS BY DEVICE             NO
   LVS SOFT SUBSTRATE PINS                NO
   LVS INJECT LOGIC                       YES
   LVS EXPAND UNBALANCED CELLS            YES
   LVS FLATTEN INSIDE CELL                NO
   LVS EXPAND SEED PROMOTIONS             NO
   LVS PRESERVE PARAMETERIZED CELLS       NO
   LVS GLOBALS ARE PORTS                  YES
   LVS REVERSE WL                         NO
   LVS SPICE PREFER PINS                  NO
   LVS SPICE SLASH IS SPACE               YES
   LVS SPICE ALLOW FLOATING PINS          YES
   // LVS SPICE ALLOW INLINE PARAMETERS
   LVS SPICE ALLOW UNQUOTED STRINGS       NO
   LVS SPICE CONDITIONAL LDD              NO
   LVS SPICE CULL PRIMITIVE SUBCIRCUITS   NO
   LVS SPICE IMPLIED MOS AREA             NO
   // LVS SPICE MULTIPLIER NAME
   LVS SPICE OVERRIDE GLOBALS             NO
   LVS SPICE REDEFINE PARAM               NO
   LVS SPICE REPLICATE DEVICES            NO
   LVS SPICE SCALE X PARAMETERS           NO
   LVS SPICE STRICT WL                    NO
   // LVS SPICE OPTION
   LVS STRICT SUBTYPES                    NO
   LVS EXACT SUBTYPES                     NO
   LAYOUT CASE                            NO
   SOURCE CASE                            NO
   LVS COMPARE CASE                       NO
   LVS DOWNCASE DEVICE                    NO
   LVS REPORT MAXIMUM                     50
   LVS PROPERTY RESOLUTION MAXIMUM        32
   // LVS SIGNATURE MAXIMUM
   // LVS FILTER UNUSED OPTION
```

```
   // LVS REPORT OPTION
   LVS REPORT UNITS                        YES
   // LVS NON USER NAME PORT
   // LVS NON USER NAME NET
   // LVS NON USER NAME INSTANCE

   // Reduction

   LVS REDUCE SERIES MOS                   YES
   LVS REDUCE PARALLEL MOS                 YES
   LVS REDUCE SEMI SERIES MOS              YES
   LVS REDUCE SPLIT GATES                  YES
   LVS REDUCE PARALLEL BIPOLAR             YES
   LVS REDUCE SERIES CAPACITORS            YES
   LVS REDUCE PARALLEL CAPACITORS          YES
   LVS REDUCE SERIES RESISTORS             YES
   LVS REDUCE PARALLEL RESISTORS           YES
   LVS REDUCE PARALLEL DIODES              YES
   LVS REDUCTION PRIORITY                  PARALLEL

   LVS SHORT EQUIVALENT NODES              NO

   // Trace Property

   TRACE PROPERTY  mn(nmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  w w 4e-09 ABSOLUTE



**************************************************************************
**************************************
                                INFORMATION AND WARNINGS
**************************************************************************
**************************************


                  Matched    Matched    Unmatched    Unmatched
Component
```

```
                  Layout     Source       Layout       Source    Type
                 -------    -------    ---------    ---------    ----
-----
   Nets:              6          6            0            0
   Instances:         3          3            0            0
mn(NMOS_VTL)
                      2          2            0            0
mp(PMOS_VTL)
                      1          1            0            0    SMN2
                      1          1            0            0
SPMP_2_1
                 -------    -------    ---------    ---------
   Total Inst:        7          7            0            0


****************************************************************************
**************************************
                                    SUMMARY
****************************************************************************
**************************************

Total CPU Time:      0 sec
Total Elapsed Time:  0 sec
```

FO1

```
                  ################################################
                  ##                                            ##
                  ##         C A L I B R E    S Y S T E M       ##
                  ##                                            ##
                  ##             L V S   R E P O R T            ##
                  ##                                            ##
                  ################################################


REPORT FILE NAME:         AOI_Custom_FO1.lvs.report
LAYOUT NAME:              AOI_Custom_FO1.calibre.db
SOURCE NAME:              /u/haranadh/cadence/LVS-
files/AOI_Custom_FO1.src.net ('AOI_Custom_FO1')
RULE FILE:                /u/haranadh/cadence/LVS-
files/_calibreLVS.rul_
RULE FILE TITLE:          LVS Rule File for FreePDK45
LVS MODE:                 Mask
```

```
RULE FILE NAME:           /u/haranadh/cadence/LVS-
files/_calibreLVS.rul_
CREATION TIME:            Mon Mar 13 21:19:27 2017
CURRENT DIRECTORY:        /u/haranadh/cadence/LVS-files
USER NAME:                haranadh
CALIBRE VERSION:          v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013


**************************************************************************
**************************************
                              OVERALL COMPARISON RESULTS
**************************************************************************
**************************************


                        #       ###################       _   _
                      #         #                 #       *   *
                   #   #        #     CORRECT     #         |
                    # #         #                 #       \___/
                     #          ###################


------------------------------------------------------------------------
----------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Nets:              11        11

 Instances:          8         8         mn (4 pins)
                     8         8         mp (4 pins)
                ------    ------
 Total Inst:        16        16


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Nets:               7         7

 Instances:          4         4         mn (4 pins)
                     2         2         mp (4 pins)
                     2         2         SMN2 (4 pins)
                     2         2         SPMP_2_1 (5 pins)
                ------    ------
 Total Inst:        10        10
```

```
*************************************************************************
**************************************
                                      LVS PARAMETERS
*************************************************************************
**************************************
```

o LVS Setup:

LVS COMPONENT TYPE PROPERTY	element
LVS COMPONENT SUBTYPE PROPERTY	model
// LVS PIN NAME PROPERTY	
LVS POWER NAME	"VDD"
LVS GROUND NAME	"VSS" "GROUND"
LVS CELL SUPPLY	NO
LVS RECOGNIZE GATES	ALL
LVS IGNORE PORTS	YES
LVS CHECK PORT NAMES	NO
LVS IGNORE TRIVIAL NAMED PORTS	NO
LVS BUILTIN DEVICE PIN SWAP	YES
LVS ALL CAPACITOR PINS SWAPPABLE	NO
LVS DISCARD PINS BY DEVICE	NO
LVS SOFT SUBSTRATE PINS	NO
LVS INJECT LOGIC	YES
LVS EXPAND UNBALANCED CELLS	YES
LVS FLATTEN INSIDE CELL	NO
LVS EXPAND SEED PROMOTIONS	NO
LVS PRESERVE PARAMETERIZED CELLS	NO
LVS GLOBALS ARE PORTS	YES
LVS REVERSE WL	NO
LVS SPICE PREFER PINS	NO
LVS SPICE SLASH IS SPACE	YES
LVS SPICE ALLOW FLOATING PINS	YES
// LVS SPICE ALLOW INLINE PARAMETERS	
LVS SPICE ALLOW UNQUOTED STRINGS	NO
LVS SPICE CONDITIONAL LDD	NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS	NO
LVS SPICE IMPLIED MOS AREA	NO
// LVS SPICE MULTIPLIER NAME	
LVS SPICE OVERRIDE GLOBALS	NO
LVS SPICE REDEFINE PARAM	NO
LVS SPICE REPLICATE DEVICES	NO
LVS SPICE SCALE X PARAMETERS	NO
LVS SPICE STRICT WL	NO
// LVS SPICE OPTION	
LVS STRICT SUBTYPES	NO
LVS EXACT SUBTYPES	NO
LAYOUT CASE	NO
SOURCE CASE	NO

```
   LVS COMPARE CASE                        NO
   LVS DOWNCASE DEVICE                     NO
   LVS REPORT MAXIMUM                      50
   LVS PROPERTY RESOLUTION MAXIMUM         32
   // LVS SIGNATURE MAXIMUM
   // LVS FILTER UNUSED OPTION
   // LVS REPORT OPTION
   LVS REPORT UNITS                        YES
   // LVS NON USER NAME PORT
   // LVS NON USER NAME NET
   // LVS NON USER NAME INSTANCE

   // Reduction

   LVS REDUCE SERIES MOS                   YES
   LVS REDUCE PARALLEL MOS                 YES
   LVS REDUCE SEMI SERIES MOS              YES
   LVS REDUCE SPLIT GATES                  YES
   LVS REDUCE PARALLEL BIPOLAR             YES
   LVS REDUCE SERIES CAPACITORS            YES
   LVS REDUCE PARALLEL CAPACITORS          YES
   LVS REDUCE SERIES RESISTORS             YES
   LVS REDUCE PARALLEL RESISTORS           YES
   LVS REDUCE PARALLEL DIODES              YES
   LVS REDUCTION PRIORITY                  PARALLEL

   LVS SHORT EQUIVALENT NODES              NO

   // Trace Property

   TRACE PROPERTY  mn(nmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  w w 4e-09 ABSOLUTE


********************************************************************************
****************************************
                                INFORMATION AND WARNINGS
```

```
********************************************************************************
****************************************

                  Matched    Matched    Unmatched    Unmatched
Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    ----
-----
   Nets:               7          7            0            0
   Instances:          4          4            0            0
mn(NMOS_VTL)
                       2          2            0            0
mp(PMOS_VTL)
                       2          2            0            0    SMN2
                       2          2            0            0
SPMP_2_1
                  -------    -------    ---------    ---------
   Total Inst:        10         10            0            0

********************************************************************************
****************************************
                                      SUMMARY
********************************************************************************
****************************************

Total CPU Time:      0 sec
Total Elapsed Time:  0 sec
```

FO2

```
                  ##################################################
                  ##                                              ##
                  ##         C A L I B R E    S Y S T E M         ##
                  ##                                              ##
                  ##             L V S   R E P O R T              ##
                  ##                                              ##
                  ##################################################


REPORT FILE NAME:         AOI_Custom_FO2.lvs.report
LAYOUT NAME:              AOI_Custom_FO2.calibre.db
```

```
SOURCE NAME:              /u/haranadh/cadence/LVS-
files/AOI_Custom_FO2.src.net ('AOI_Custom_FO2')
RULE FILE:                /u/haranadh/cadence/LVS-
files/_calibreLVS.rul_
RULE FILE TITLE:          LVS Rule File for FreePDK45
LVS MODE:                 Mask
RULE FILE NAME:           /u/haranadh/cadence/LVS-
files/_calibreLVS.rul_
CREATION TIME:            Mon Mar 13 21:32:26 2017
CURRENT DIRECTORY:        /u/haranadh/cadence/LVS-files
USER NAME:                haranadh
CALIBRE VERSION:          v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013


****************************************************************************
**************************************
                              OVERALL COMPARISON RESULTS
****************************************************************************
**************************************


                        #       ###################       _   _
                       #        #                 #       *   *
                    #   #       #     CORRECT     #         |
                     # #        #                 #       \___/
                      #         ###################


  Warning:  Ambiguity points were found and resolved arbitrarily.

----------------------------------------------------------------------------
----------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                 Layout    Source         Component Type
                 ------    ------         --------------
 Nets:               14        14

 Instances:          11        11         mn (4 pins)
                     11        11         mp (4 pins)
                 ------    ------
 Total Inst:         22        22


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                 Layout    Source         Component Type
                 ------    ------         --------------
 Nets:                8         8
```

```
 Instances:          5         5         mn (4 pins)
                     2         2         mp (4 pins)
                     3         3         SMN2 (4 pins)
                     3         3         SPMP_2_1 (5 pins)
                  ------    ------
 Total Inst:        13        13


********************************************************************************
****************************************
                                        LVS PARAMETERS
********************************************************************************
****************************************


o LVS Setup:

   LVS COMPONENT TYPE PROPERTY            element
   LVS COMPONENT SUBTYPE PROPERTY         model
   // LVS PIN NAME PROPERTY
   LVS POWER NAME                         "VDD"
   LVS GROUND NAME                        "VSS" "GROUND"
   LVS CELL SUPPLY                        NO
   LVS RECOGNIZE GATES                    ALL
   LVS IGNORE PORTS                       YES
   LVS CHECK PORT NAMES                   NO
   LVS IGNORE TRIVIAL NAMED PORTS         NO
   LVS BUILTIN DEVICE PIN SWAP            YES
   LVS ALL CAPACITOR PINS SWAPPABLE       NO
   LVS DISCARD PINS BY DEVICE             NO
   LVS SOFT SUBSTRATE PINS                NO
   LVS INJECT LOGIC                       YES
   LVS EXPAND UNBALANCED CELLS            YES
   LVS FLATTEN INSIDE CELL                NO
   LVS EXPAND SEED PROMOTIONS             NO
   LVS PRESERVE PARAMETERIZED CELLS       NO
   LVS GLOBALS ARE PORTS                  YES
   LVS REVERSE WL                         NO
   LVS SPICE PREFER PINS                  NO
   LVS SPICE SLASH IS SPACE               YES
   LVS SPICE ALLOW FLOATING PINS          YES
   // LVS SPICE ALLOW INLINE PARAMETERS
   LVS SPICE ALLOW UNQUOTED STRINGS       NO
   LVS SPICE CONDITIONAL LDD              NO
   LVS SPICE CULL PRIMITIVE SUBCIRCUITS   NO
   LVS SPICE IMPLIED MOS AREA             NO
   // LVS SPICE MULTIPLIER NAME
   LVS SPICE OVERRIDE GLOBALS             NO
   LVS SPICE REDEFINE PARAM               NO
   LVS SPICE REPLICATE DEVICES            NO
```

```
LVS SPICE SCALE X PARAMETERS           NO
LVS SPICE STRICT WL                    NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                    NO
LVS EXACT SUBTYPES                     NO
LAYOUT CASE                            NO
SOURCE CASE                            NO
LVS COMPARE CASE                       NO
LVS DOWNCASE DEVICE                    NO
LVS REPORT MAXIMUM                     50
LVS PROPERTY RESOLUTION MAXIMUM        32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                       YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction

LVS REDUCE SERIES MOS                  YES
LVS REDUCE PARALLEL MOS                YES
LVS REDUCE SEMI SERIES MOS             YES
LVS REDUCE SPLIT GATES                 YES
LVS REDUCE PARALLEL BIPOLAR            YES
LVS REDUCE SERIES CAPACITORS           YES
LVS REDUCE PARALLEL CAPACITORS         YES
LVS REDUCE SERIES RESISTORS            YES
LVS REDUCE PARALLEL RESISTORS          YES
LVS REDUCE PARALLEL DIODES             YES
LVS REDUCTION PRIORITY                 PARALLEL

LVS SHORT EQUIVALENT NODES             NO

// Trace Property

TRACE PROPERTY  mn(nmos_vtl)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtl)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtl)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtl)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vth)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vth)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vth)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vth)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtg)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtg)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtg)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtg)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_thkox)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_thkox)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_thkox)  l l 4e-09 ABSOLUTE
```

```
   TRACE PROPERTY  mp(pmos_thkox)  w w 4e-09 ABSOLUTE


****************************************************************************
************************************
                                INFORMATION AND WARNINGS
****************************************************************************
************************************


                  Matched    Matched    Unmatched    Unmatched
Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    ----
-----
   Nets:               8          8            0            0
   Instances:          5          5            0            0
mn(NMOS_VTL)
                       2          2            0            0
mp(PMOS_VTL)
                       3          3            0            0    SMN2
                       3          3            0            0
SPMP_2_1
                  -------    -------    ---------    ---------
   Total Inst:        13         13            0            0


o Statistics:

   1 net was matched arbitrarily.


o Ambiguity Resolution Points:

      (Each one of the following objects belongs to a group of
indistinguishable objects.
       The listed objects were matched arbitrarily by the Ambiguity
Resolution feature of LVS.
       Arbitrary matching may be prevented by assigning names to these
objects or to adjacent nets).

       Layout
Source
       ------                                                      -----
-

                                     Nets
                                     ----
```

```
       9(6.345,0.720)
net010



********************************************************************************
****************************************
                                        SUMMARY
********************************************************************************
****************************************

Total CPU Time:      0 sec
Total Elapsed Time:  0 sec
```

FO4

```
                  ##################################################
                  ##                                              ##
                  ##         C A L I B R E    S Y S T E M         ##
                  ##                                              ##
                  ##             L V S   R E P O R T              ##
                  ##                                              ##
                  ##################################################



REPORT FILE NAME:         aoi_F04_lab4.lvs.report
LAYOUT NAME:              aoi_F04_lab4.calibre.db
SOURCE NAME:              /u/sanjana2/cadence/LVS-
files/aoi_F04_lab4.src.net ('aoi_F04_lab4')
RULE FILE:                /u/sanjana2/cadence/LVS-files/_calibreLVS.rul_
RULE FILE TITLE:          LVS Rule File for FreePDK45
LVS MODE:                 Mask
RULE FILE NAME:           /u/sanjana2/cadence/LVS-files/_calibreLVS.rul_
CREATION TIME:            Tue Dec  6 16:03:24 2016
CURRENT DIRECTORY:        /u/sanjana2/cadence/LVS-files
USER NAME:                sanjana2
CALIBRE VERSION:          v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013


********************************************************************************
**********************************
                                OVERALL COMPARISON RESULTS
********************************************************************************
**********************************
```

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Nets:	20	20	
Instances:	17	17	mn (4 pins)
	17	17	mp (4 pins)
Total Inst:	34	34	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Nets:	10	10	
Instances:	7	7	mn (4 pins)
	2	2	mp (4 pins)
	5	5	SMN2 (4 pins)
	5	5	SPMP_2_1 (5 pins)
Total Inst:	19	19	

****

LVS PARAMETERS

****

o LVS Setup:

```
LVS COMPONENT TYPE PROPERTY          element
LVS COMPONENT SUBTYPE PROPERTY       model
// LVS PIN NAME PROPERTY
LVS POWER NAME                       "VDD"
LVS GROUND NAME                      "VSS" "GROUND"
```

```
LVS CELL SUPPLY                         NO
LVS RECOGNIZE GATES                     ALL
LVS IGNORE PORTS                        YES
LVS CHECK PORT NAMES                    NO
LVS IGNORE TRIVIAL NAMED PORTS          NO
LVS BUILTIN DEVICE PIN SWAP             YES
LVS ALL CAPACITOR PINS SWAPPABLE        NO
LVS DISCARD PINS BY DEVICE              NO
LVS SOFT SUBSTRATE PINS                 NO
LVS INJECT LOGIC                        YES
LVS EXPAND UNBALANCED CELLS             YES
LVS FLATTEN INSIDE CELL                 NO
LVS EXPAND SEED PROMOTIONS              NO
LVS PRESERVE PARAMETERIZED CELLS        NO
LVS GLOBALS ARE PORTS                   YES
LVS REVERSE WL                          NO
LVS SPICE PREFER PINS                   NO
LVS SPICE SLASH IS SPACE                YES
LVS SPICE ALLOW FLOATING PINS           YES
// LVS SPICE ALLOW INLINE PARAMETERS
LVS SPICE ALLOW UNQUOTED STRINGS        NO
LVS SPICE CONDITIONAL LDD               NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS    NO
LVS SPICE IMPLIED MOS AREA              NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS              NO
LVS SPICE REDEFINE PARAM                NO
LVS SPICE REPLICATE DEVICES             NO
LVS SPICE SCALE X PARAMETERS            NO
LVS SPICE STRICT WL                     NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                     NO
LVS EXACT SUBTYPES                      NO
LAYOUT CASE                             NO
SOURCE CASE                             NO
LVS COMPARE CASE                        NO
LVS DOWNCASE DEVICE                     NO
LVS REPORT MAXIMUM                      50
LVS PROPERTY RESOLUTION MAXIMUM         32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                        YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction

LVS REDUCE SERIES MOS                   YES
LVS REDUCE PARALLEL MOS                 YES
LVS REDUCE SEMI SERIES MOS              YES
LVS REDUCE SPLIT GATES                  YES
LVS REDUCE PARALLEL BIPOLAR             YES
```

```
   LVS REDUCE SERIES CAPACITORS           YES
   LVS REDUCE PARALLEL CAPACITORS         YES
   LVS REDUCE SERIES RESISTORS            YES
   LVS REDUCE PARALLEL RESISTORS          YES
   LVS REDUCE PARALLEL DIODES             YES
   LVS REDUCTION PRIORITY                 PARALLEL

   LVS SHORT EQUIVALENT NODES             NO

   // Trace Property

   TRACE PROPERTY  mn(nmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  w w 4e-09 ABSOLUTE


********************************************************************************
**********************************
                                INFORMATION AND WARNINGS
********************************************************************************
**********************************


                  Matched    Matched    Unmatched    Unmatched
Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    --------
-
   Nets:               10         10            0            0

   Instances:           7          7            0            0
mn(NMOS_VTL)
                        2          2            0            0
mp(PMOS_VTL)
                        5          5            0            0    SMN2
                        5          5            0            0    SPMP_2_1
                  -------    -------    ---------    ---------
   Total Inst:         19         19            0            0
```

```
o Initial Correspondence Points:

   Nets:         o4 o3 o2 vdd! gnd! Y o1 x


**************************************************************************
**********************************
                                    SUMMARY
**************************************************************************
**********************************

Total CPU Time:      0 sec
Total Elapsed Time:  0 sec
```

FO8

```
                  ##################################################
                  ##                                              ##
                  ##         C A L I B R E    S Y S T E M         ##
                  ##                                              ##
                  ##             L V S   R E P O R T              ##
                  ##                                              ##
                  ##################################################



REPORT FILE NAME:         AOI_Custom_FO8.lvs.report
LAYOUT NAME:              AOI_Custom_FO8.calibre.db
SOURCE NAME:              /u/haranadh/cadence/LVS-
files/AOI_Custom_FO8.src.net ('AOI_Custom_FO8')
RULE FILE:                /u/haranadh/cadence/LVS-
files/_calibreLVS.rul_
RULE FILE TITLE:          LVS Rule File for FreePDK45
LVS MODE:                 Mask
RULE FILE NAME:           /u/haranadh/cadence/LVS-
files/_calibreLVS.rul_
CREATION TIME:            Mon Mar 13 21:46:54 2017
CURRENT DIRECTORY:        /u/haranadh/cadence/LVS-files
USER NAME:                haranadh
CALIBRE VERSION:          v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013


**************************************************************************
**************************************
                                  OVERALL COMPARISON RESULTS
**************************************************************************
**************************************
```

Warning: Ambiguity points were found and resolved arbitrarily.

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Nets:	32	32	
Instances:	29	29	mn (4 pins)
	29	29	mp (4 pins)
Total Inst:	58	58	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Nets:	14	14	
Instances:	11	11	mn (4 pins)
	2	2	mp (4 pins)
	9	9	SMN2 (4 pins)
	9	9	SPMP_2_1 (5 pins)
Total Inst:	31	31	

****

LVS PARAMETERS

****

o LVS Setup:

LVS COMPONENT TYPE PROPERTY element

```
LVS COMPONENT SUBTYPE PROPERTY         model
// LVS PIN NAME PROPERTY
LVS POWER NAME                         "VDD"
LVS GROUND NAME                        "VSS" "GROUND"
LVS CELL SUPPLY                        NO
LVS RECOGNIZE GATES                    ALL
LVS IGNORE PORTS                       YES
LVS CHECK PORT NAMES                   NO
LVS IGNORE TRIVIAL NAMED PORTS         NO
LVS BUILTIN DEVICE PIN SWAP            YES
LVS ALL CAPACITOR PINS SWAPPABLE       NO
LVS DISCARD PINS BY DEVICE             NO
LVS SOFT SUBSTRATE PINS                NO
LVS INJECT LOGIC                       YES
LVS EXPAND UNBALANCED CELLS            YES
LVS FLATTEN INSIDE CELL                NO
LVS EXPAND SEED PROMOTIONS             NO
LVS PRESERVE PARAMETERIZED CELLS       NO
LVS GLOBALS ARE PORTS                  YES
LVS REVERSE WL                         NO
LVS SPICE PREFER PINS                  NO
LVS SPICE SLASH IS SPACE               YES
LVS SPICE ALLOW FLOATING PINS          YES
// LVS SPICE ALLOW INLINE PARAMETERS
LVS SPICE ALLOW UNQUOTED STRINGS       NO
LVS SPICE CONDITIONAL LDD              NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS   NO
LVS SPICE IMPLIED MOS AREA             NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS             NO
LVS SPICE REDEFINE PARAM               NO
LVS SPICE REPLICATE DEVICES            NO
LVS SPICE SCALE X PARAMETERS           NO
LVS SPICE STRICT WL                    NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                    NO
LVS EXACT SUBTYPES                     NO
LAYOUT CASE                            NO
SOURCE CASE                            NO
LVS COMPARE CASE                       NO
LVS DOWNCASE DEVICE                    NO
LVS REPORT MAXIMUM                     50
LVS PROPERTY RESOLUTION MAXIMUM        32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                       YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction
```

```
   LVS REDUCE SERIES MOS                   YES
   LVS REDUCE PARALLEL MOS                 YES
   LVS REDUCE SEMI SERIES MOS              YES
   LVS REDUCE SPLIT GATES                  YES
   LVS REDUCE PARALLEL BIPOLAR             YES
   LVS REDUCE SERIES CAPACITORS            YES
   LVS REDUCE PARALLEL CAPACITORS          YES
   LVS REDUCE SERIES RESISTORS             YES
   LVS REDUCE PARALLEL RESISTORS           YES
   LVS REDUCE PARALLEL DIODES              YES
   LVS REDUCTION PRIORITY                  PARALLEL

   LVS SHORT EQUIVALENT NODES              NO

   // Trace Property

   TRACE PROPERTY  mn(nmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  w w 4e-09 ABSOLUTE


********************************************************************************
**************************************
                                INFORMATION AND WARNINGS
********************************************************************************
**************************************


                  Matched    Matched    Unmatched    Unmatched
Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    ----
-----
   Nets:               14         14            0            0

   Instances:          11         11            0            0
mn(NMOS_VTL)
```

```
                         2           2             0             0
mp(PMOS_VTL)
                         9           9             0             0    SMN2
                         9           9             0             0
SPMP_2_1
                  -------     -------     ---------     ---------
   Total Inst:         31          31             0             0


o Statistics:

   7 nets were matched arbitrarily.


o Ambiguity Resolution Points:

      (Each one of the following objects belongs to a group of
indistinguishable objects.
       The listed objects were matched arbitrarily by the Ambiguity
Resolution feature of LVS.
       Arbitrary matching may be prevented by assigning names to these
objects or to adjacent nets).

       Layout
Source
       ------                                                        -----
-

                                       Nets
                                       ----

       30(29.675,0.720)                                              net16
       27(26.265,0.720)                                              net11
       24(23.025,0.720)                                              net13
       21(19.870,0.720)                                              net14
       18(16.350,0.720)                                              net17
       15(12.770,0.720)                                              net18
       12(9.600,0.720)                                               net19



********************************************************************************
*************************************
                                          SUMMARY
********************************************************************************
*************************************

Total CPU Time:      0 sec
Total Elapsed Time:  0 sec
```

Standard Cell Template