Laboratory 3

Full Custom Inverter Layout

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Group Number - 5

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Introduction and Physical Properties

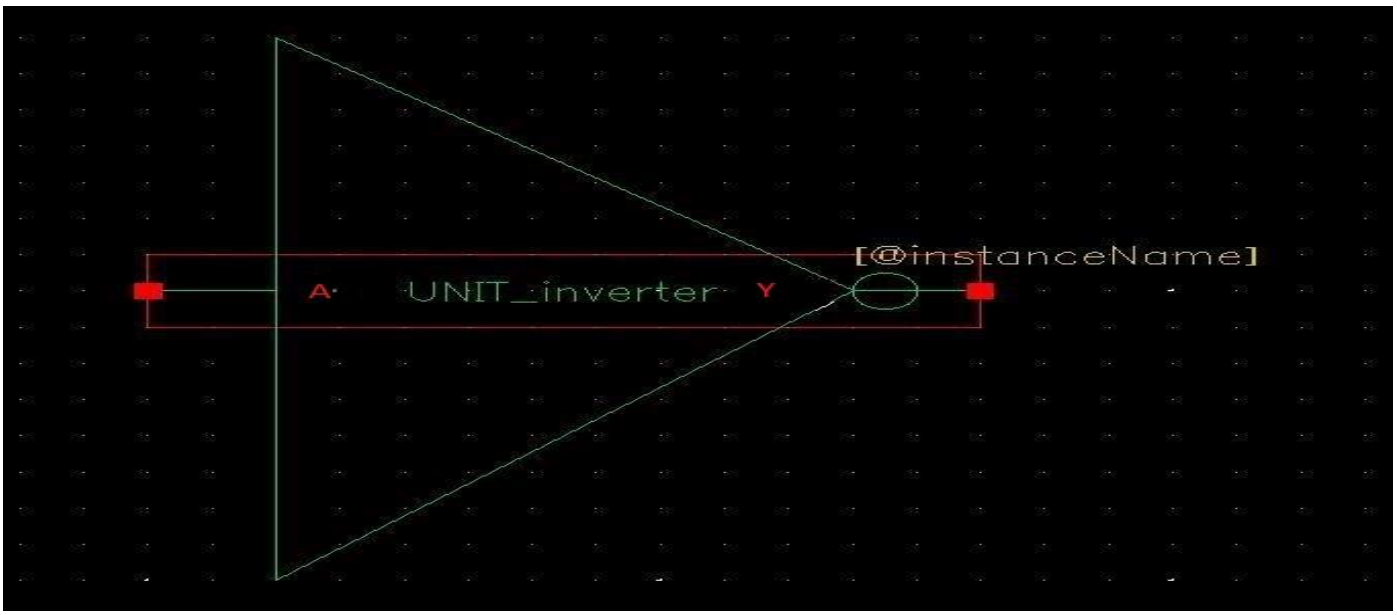
Cell Description

CMOS is referred as complementary-symmetry metal oxide semiconductor. The inverter is universally accepted as the most basic logic gate doing a Boolean function on a single input variable. The simple structure consists of a p-mos at the top and n-mos transistor at the bottom. A pair of complementary and symmetrical p-type and n-type metal oxide semiconductor field effect transistor is used for performing logic functions. CMOS devices are high noise immunity and low static power consumption. The Boolean equation is as shown below:

$$Q = \sim A$$

Where Q is output and A is input

CELL SYMBOL:



Cell Truth Table:

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Truth table of the inverter is as shown below. We can observe that the output of the inverter is reverse of those respective inputs.

Logic function is no different than that of Inverter, i.e.,

$$Q = \sim A$$

Where Q is output and A is input.

Input	Output
0	H
1	L

Table 1: Inverter full custom truth table.

Input and Output Parasitic Capacitance Table

From the schematic calculate each input's capacitance normalized to the nominal inverter (your inverter standard cell) by the width of the transistor or drain area as needed. This entry should be an integer fraction similar to Weste and Harris. [Note the normalization is to a standard inverter (the standard cell inverter INV1X). Repeat the rows as needed.]

Computed Cell Input Capacitance	
Input Name	**Capacitance (/Cinv)**
Output Name	**Capacitance (/Cinv)**

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Performance Analysis

Rise and Fall Times

[Note: It is highly desirable to split the simulation work load among the team members so that each team member learns how to use the tools.]

FOx denotes output loads. The loads are defined by the number of identical logic gates. Use 20%-80% swings for the output rise and fall entries. Use a 1.2V power supply.

For each output load in the table complete transient simulations. Remember to include a CMOS non-inverting buffer between the ideal voltage source and the logic gate driving the FOx load. Note rise t_r / fall t_f times are at the input to the logic gate driving the load, **not** the rise/fall times for the input ideal voltage source.

Complete the number needed copies (copies = No. input stacks x No. outputs) of the table below.

For multi-input gates, complete tables for each transistor stack (i.e. each branch connected to the output) using the stack's worst case single controlling input transition in the stack. Label the tables with worst case input in each stack and the output. Replace **X** below with the signal name.

Input X: Output Rise Time Data t_r (ns)					
Input rise/fall time (ns)	Output Load (FOx) 0	1	2	4	8
0.04					
0.06					

Stack Input Combination: ***Replace with Boolean Product***

Stack S, Input X: Output Fall Time Data t_f (ns)					
Input rise/fall time (ns)	Output Load (FOx) 0	1	2	4	8
0.04					
0.06					

Stack Input Combination: ***Replace with Boolean Product***

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Propagation Delays

For the range of output loads shown in the table simulate propagation delays (low to high t_{plh} and high to low t_{phl}) for the stack's worst case single controlling input transition. The input controlling the output is the same input reported in the rise and fall time section. Use a 1.2V power supply and timing measurements start when input to the logic gate driving the FOx load crosses the 50% of the rail and stop when the logic gate driving output crosses 50% of the rail. Negative values are entered as 0.

Label the tables with the Boolean product (e.g. AB) of the transistor stack and the output. Complete copies of the table below for each branch connected to the output.

Data Worst Case Low to High Propagation Delay Data t_{plh} (ns)					
Input rise/fall time (ns)	Output Load (FOx) 0	1	2	4	8
0.04					
0.06					

Worse Case Input Combination: ***Replace with Boolean Product***

Data Worst Case High to Low Propagation Delay Data t_{phl} (ns)					
Input rise/fall time (ns)	Output Load (FOx) 0	1	2	4	8
0.04					
0.06					

Worse Case Input Combination: ***Replace with Boolean Product***

From each row of the slew rate data compute the best fit linear propagation delay equation for low-to-high T_{plh} (h) and high-to-low T_{phl} (h). The model predicts a delay, in nanoseconds, as a function of the output load, *h*, *Cout/Cin =FOx*. The model line is parameterized by a slope, *m*, and an intercept, *b*. The units of *m* are (*ns/FOx*) and the units of *b* are *ns*.

Complete the table below by increasing the number of rows for multiple input gates. The row labeled **All data** is the computed slope and intercept after combining data from all slew rates.

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Complete the **Model** row for the gate using the assumptions and methods of the linear delay model from Weste and Harris. Only skewed standard cells will have different values propagation models for rising and falling inputs.

All data means combine the results for both slew rates into a single model.

Discuss in your own words the differences in the calibration and the Weste Harris linear delay model. Discuss the differences in high-to-low versus low-to-high models.

Data Model Propagation Delay Equation $T_{pd}(h) = b + m \cdot h$				
Input Slew Rate (ns) (b_r)	Rising Logical Effort (m_r)	Falling Logical Effort (m_f)	Parasitic Rising Delay (b_r)	Parasitic Falling Delay
0.04				
0.06				
All data				

In the table below normalize the model for the T_{pd} (h) results of the table above to give the logical effort model *D(h)* described in Weste and Harris. *D(h)* is a unitless value and predicts the delay as multiples of the standard inverter delay. Normalization is based on the observed CMOS inverter parasitic delay, b_{inv}. *Recall* ***all data*** $p_{inv} \approx 1$.

Inverter Normalized Data Model Propagation Delay Equation $D(h) = p + g \cdot h$				
Input Slew Rate (ns)	Rising Logical) Effort (g_r	Falling Logical Effort (g_f)	Parasitic Rising Delay (p_r)	Parasitic Falling Delay (p_r)
0.04				
0.06				
All data				
W&H Model				

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Power-Delay

Simulate the cell for a sequence of input combinations based on the Gray code and compute the time averaged power (mW), average delay (ns), and average powerdelay product (mW ns = pJ). The Gray code restricts the simulations to single input transitions and ignores the large number of multiple input change combinations. Use the same slew rate for all input transitions. Use equal output loads for multiple output gates. Use a period of 2X maximum output delay with FO=8.

Average Power Data (mW)					
Input Slew (ns)	Output Load (FOx) 0	1	2	4	8
0.04					
0.06					

verage Delay Data (ns)					
Input Slew (ns)	Output Load (FOx) 0	1	2	4	8
0.04					
0.06					

Average Power-Delay Data (pJ)					
Input Slew (ns)	Output Load (FOx) 0	1	2	4	8
0.04					
0.06					

Schematic Diagram

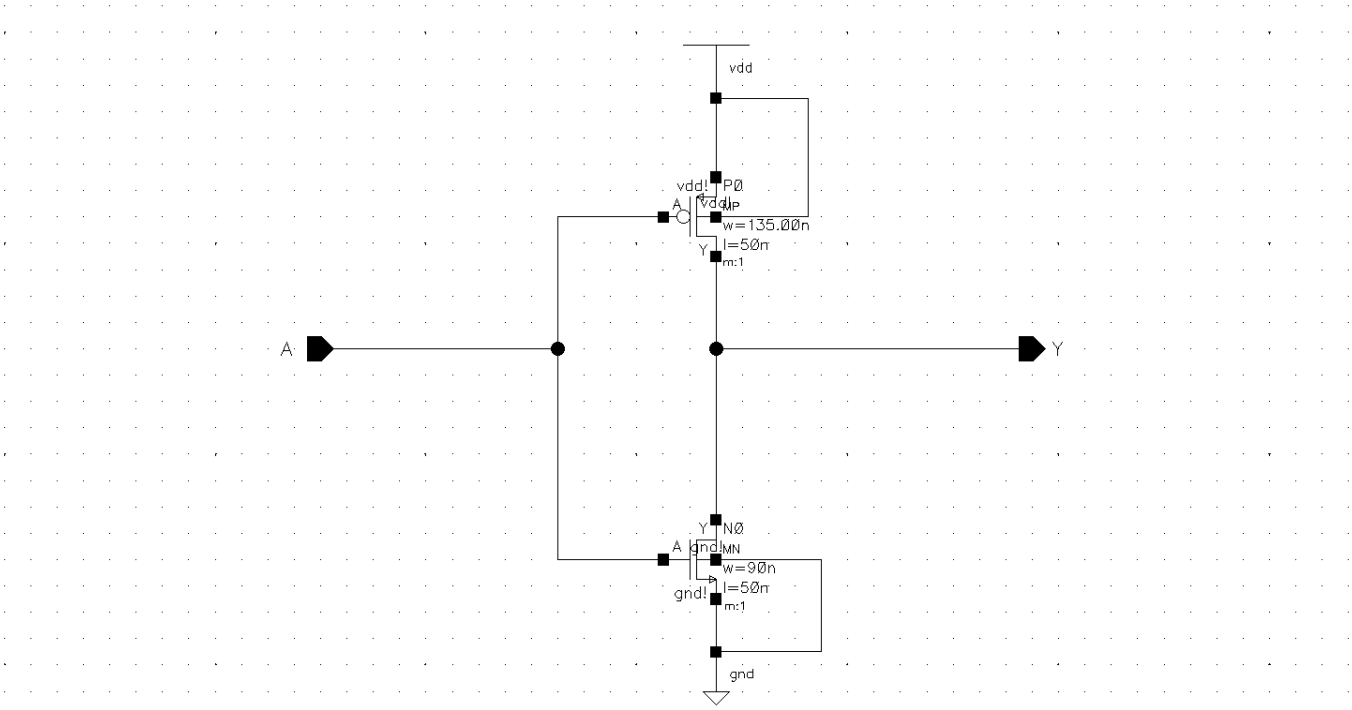

Figure 1: Schematic diagram of Full custom Inverter

Transistor Dimensions

Save a color or black and white layout of the cell in EPS (i.e. Encapsulated Postscript) format. The cell dimensions are saved in both lambda (□) and microns (□m). Record the transistor length and width dimensions (nm).
[Repeat the transistor row as needed.]

Cell Physical Dimensions		
	X	Y
Cell Dimension in □□		
Cell Dimension in □m		

Transistor Dimensions		
UNIT Name	Length (nm)	Width (nm)
NMOS N1	50	90
PMOS P0	50	135

Table 2 : Inverter Transistor Dimensions

Cell Layout

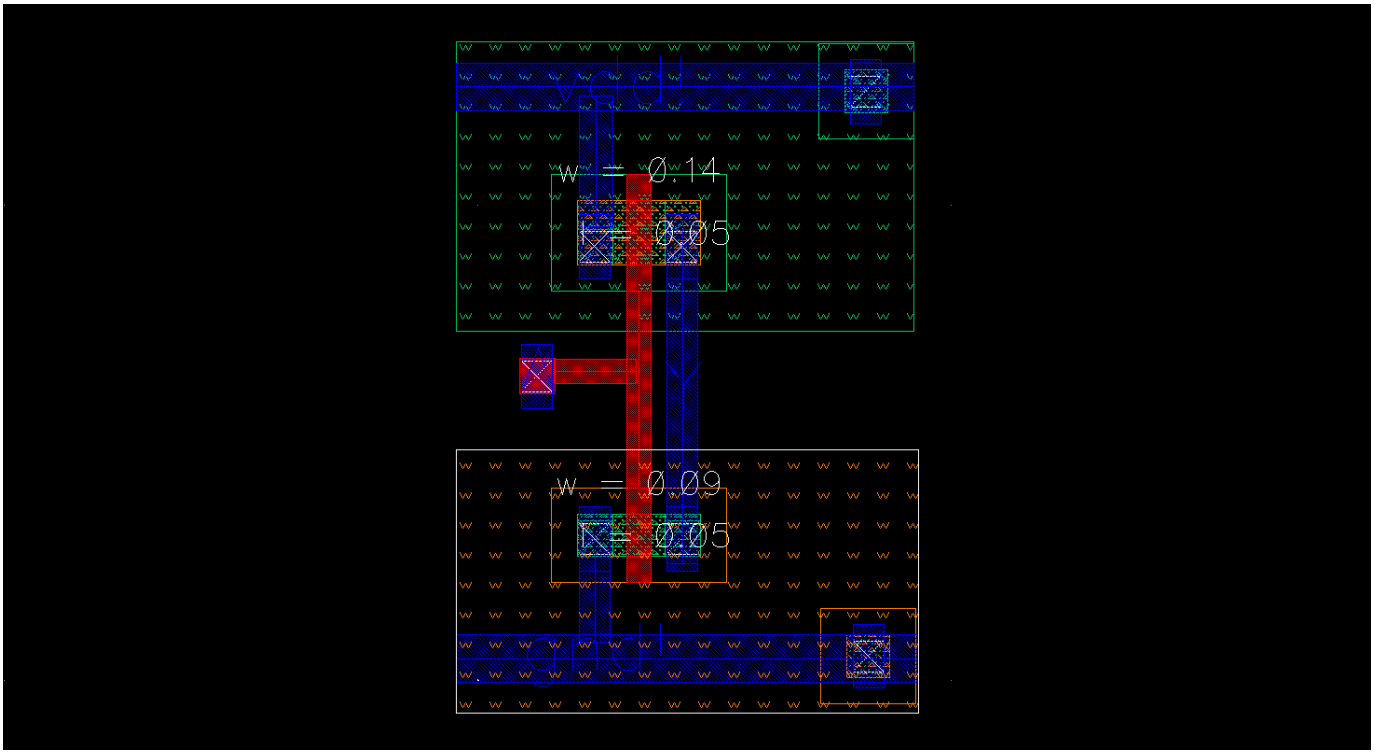

Figure 2: Layout diagram of Full custom Inverter

DRC Report

```
================================================================================
=
=== CALIBRE::DRC-F SUMMARY REPORT
===
Execution Date/Time:       Wed Feb 22 21:20:43 2017
Calibre Version:           v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013
Rule File Pathname:        /u/erpina/cadence/DRC-files/_calibreDRC.rul_
Rule File Title:
Layout System:             GDS
Layout Path(s):            Inverter.calibre.db
Layout Primary Cell:       Inverter
Current Directory:         /u/erpina/cadence/DRC-files
User Name:                 erpina
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      Inverter.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       Inverter.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID = NO
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:         COMMENT TEXT + RULE FILE INFORMATION
Layers:                    MEMORY-BASED
Keep Empty Checks:         YES
--------------------------------------------------------------------------------
-
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------------------
-
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ...... TOTAL Original Geometry Count = 3
LAYER nwell ...... TOTAL Original Geometry Count = 3
LAYER active ..... TOTAL Original Geometry Count = 16
LAYER poly ....... TOTAL Original Geometry Count = 9
LAYER pimplant ... TOTAL Original Geometry Count = 2
LAYER nimplant ... TOTAL Original Geometry Count = 2
LAYER vth ........ TOTAL Original Geometry Count = 0
LAYER vtg ........ TOTAL Original Geometry Count = 0
LAYER metal1 ..... TOTAL Original Geometry Count = 12
LAYER metal2 ..... TOTAL Original Geometry Count = 0
```

```
LAYER metal3 ..... TOTAL Original Geometry Count = 0
LAYER metal4 ..... TOTAL Original Geometry Count = 0
LAYER metal5 ..... TOTAL Original Geometry Count = 0
LAYER metal6 ..... TOTAL Original Geometry Count = 0
LAYER metal7 ..... TOTAL Original Geometry Count = 0
LAYER metal8 ..... TOTAL Original Geometry Count = 0
LAYER metal9 ..... TOTAL Original Geometry Count = 0
LAYER metal10 .... TOTAL Original Geometry Count = 0
LAYER contact .... TOTAL Original Geometry Count = 7
LAYER via1 ....... TOTAL Original Geometry Count = 0
LAYER via2 ....... TOTAL Original Geometry Count = 0
LAYER via3 ....... TOTAL Original Geometry Count = 0
LAYER via4 ....... TOTAL Original Geometry Count = 0
LAYER via5 ....... TOTAL Original Geometry Count = 0
LAYER via6 ....... TOTAL Original Geometry Count = 0
LAYER via7 ....... TOTAL Original Geometry Count = 0
LAYER via8 ....... TOTAL Original Geometry Count = 0
LAYER via9 ....... TOTAL Original Geometry Count = 0
--------------------------------------------------------------------------------
-
--- RULECHECK RESULTS STATISTICS
---
RULECHECK Well.1 ...... TOTAL Result Count = 0
RULECHECK Well.2 ...... TOTAL Result Count = 0
RULECHECK Well.4 ...... TOTAL Result Count = 0
RULECHECK Poly.1 ...... TOTAL Result Count = 0
RULECHECK Poly.2 ...... TOTAL Result Count = 0
RULECHECK Poly.3 ...... TOTAL Result Count = 0
RULECHECK Poly.4 ...... TOTAL Result Count = 0
RULECHECK Poly.5 ...... TOTAL Result Count = 0
RULECHECK Poly.6 ...... TOTAL Result Count = 0
RULECHECK Active.1 .... TOTAL Result Count = 0
RULECHECK Active.2 .... TOTAL Result Count = 0
RULECHECK Active.3 .... TOTAL Result Count = 0
RULECHECK Active.4 .... TOTAL Result Count = 0
RULECHECK Implant.1 ... TOTAL Result Count = 0
RULECHECK Implant.2 ... TOTAL Result Count = 0
RULECHECK Implant.3 ... TOTAL Result Count = 0
RULECHECK Implant.4 ... TOTAL Result Count = 0
RULECHECK Implant.6 ... TOTAL Result Count = 0
RULECHECK Contact.1 ... TOTAL Result Count = 0
RULECHECK Contact.2 ... TOTAL Result Count = 0
RULECHECK Contact.3 ... TOTAL Result Count = 0
RULECHECK Contact.4 ... TOTAL Result Count = 0
RULECHECK Contact.5 ... TOTAL Result Count = 0
RULECHECK Contact.6 ... TOTAL Result Count = 0
RULECHECK Metal1.1 .... TOTAL Result Count = 0
RULECHECK Metal1.2 .... TOTAL Result Count = 0
RULECHECK Metal1.3 .... TOTAL Result Count = 0
RULECHECK Metal1.4 .... TOTAL Result Count = 0
RULECHECK Via1.1 ...... TOTAL Result Count = 0
RULECHECK Via1.2 ...... TOTAL Result Count = 0
RULECHECK Via1.3 ...... TOTAL Result Count = 0
RULECHECK Via1.4 ...... TOTAL Result Count = 0
```

```
RULECHECK Metal2.1 .... TOTAL Result Count = 0
RULECHECK Metal2.2 .... TOTAL Result Count = 0
RULECHECK Metal2.3 .... TOTAL Result Count = 0
RULECHECK Metal2.4 .... TOTAL Result Count = 0
RULECHECK Via2.1 ...... TOTAL Result Count = 0
RULECHECK Via2.2 ...... TOTAL Result Count = 0
RULECHECK Via2.3 ...... TOTAL Result Count = 0
RULECHECK Via2.4 ...... TOTAL Result Count = 0
RULECHECK Metal3.1 .... TOTAL Result Count = 0
RULECHECK Metal3.2 .... TOTAL Result Count = 0
RULECHECK Metal3.3 .... TOTAL Result Count = 0
RULECHECK Metal3.4 .... TOTAL Result Count = 0
RULECHECK Via3.1 ...... TOTAL Result Count = 0
RULECHECK Via3.2 ...... TOTAL Result Count = 0
RULECHECK Via3.3 ...... TOTAL Result Count = 0
RULECHECK Via3.4 ...... TOTAL Result Count = 0
RULECHECK Metal4.1 .... TOTAL Result Count = 0
RULECHECK Metal4.2 .... TOTAL Result Count = 0
RULECHECK Metal4.3 .... TOTAL Result Count = 0
RULECHECK Via4.1 ...... TOTAL Result Count = 0
RULECHECK Via4.2 ...... TOTAL Result Count = 0
RULECHECK Via4.3 ...... TOTAL Result Count = 0
RULECHECK Via4.4 ...... TOTAL Result Count = 0
RULECHECK Metal5.1 .... TOTAL Result Count = 0
RULECHECK Metal5.2 .... TOTAL Result Count = 0
RULECHECK Metal5.3 .... TOTAL Result Count = 0
RULECHECK Via5.1 ...... TOTAL Result Count = 0
RULECHECK Via5.2 ...... TOTAL Result Count = 0
RULECHECK Via5.3 ...... TOTAL Result Count = 0
RULECHECK Via5.4 ...... TOTAL Result Count = 0
RULECHECK Metal6.1 .... TOTAL Result Count = 0
RULECHECK Metal6.2 .... TOTAL Result Count = 0
RULECHECK Metal6.3 .... TOTAL Result Count = 0
RULECHECK Via6.1 ...... TOTAL Result Count = 0
RULECHECK Via6.2 ...... TOTAL Result Count = 0
RULECHECK Via6.3 ...... TOTAL Result Count = 0
RULECHECK Via6.4 ...... TOTAL Result Count = 0
RULECHECK Metal7.1 .... TOTAL Result Count = 0
RULECHECK Metal7.2 .... TOTAL Result Count = 0
RULECHECK Metal7.3 .... TOTAL Result Count = 0
RULECHECK Via7.1 ...... TOTAL Result Count = 0
RULECHECK Via7.2 ...... TOTAL Result Count = 0
RULECHECK Via7.3 ...... TOTAL Result Count = 0
RULECHECK Via7.4 ...... TOTAL Result Count = 0
RULECHECK Metal8.1 .... TOTAL Result Count = 0
RULECHECK Metal8.2 .... TOTAL Result Count = 0
RULECHECK Metal8.3 .... TOTAL Result Count = 0
RULECHECK Via8.1 ...... TOTAL Result Count = 0
RULECHECK Via8.2 ...... TOTAL Result Count = 0
RULECHECK Via8.3 ...... TOTAL Result Count = 0
RULECHECK Via8.4 ...... TOTAL Result Count = 0
RULECHECK Metal9.1 .... TOTAL Result Count = 0
RULECHECK Metal9.2 .... TOTAL Result Count = 0
RULECHECK Metal9.3 .... TOTAL Result Count = 0
```

```
RULECHECK Via9.1 ..... TOTAL Result Count = 0
RULECHECK Via9.2 ..... TOTAL Result Count = 0
RULECHECK Via9.3 ..... TOTAL Result Count = 0
RULECHECK Via9.4 ..... TOTAL Result Count = 0
RULECHECK Metal10.1 ... TOTAL Result Count = 0
RULECHECK Metal10.2 ... TOTAL Result Count = 0
RULECHECK Metal10.3 ... TOTAL Result Count = 0
RULECHECK Metal1.5 .... TOTAL Result Count = 0
RULECHECK Metal1.6 .... TOTAL Result Count = 0
RULECHECK Metal1.7 .... TOTAL Result Count = 0
RULECHECK Metal1.8 .... TOTAL Result Count = 0
RULECHECK Metal1.9 .... TOTAL Result Count = 0
RULECHECK Metal2.5 .... TOTAL Result Count = 0
RULECHECK Metal2.6 .... TOTAL Result Count = 0
RULECHECK Metal2.7 .... TOTAL Result Count = 0
RULECHECK Metal2.8 .... TOTAL Result Count = 0
RULECHECK Metal2.9 .... TOTAL Result Count = 0
RULECHECK Metal3.5 .... TOTAL Result Count = 0
RULECHECK Metal3.6 .... TOTAL Result Count = 0
RULECHECK Metal3.7 .... TOTAL Result Count = 0
RULECHECK Metal3.8 .... TOTAL Result Count = 0
RULECHECK Metal3.9 .... TOTAL Result Count = 0
RULECHECK Metal4.5 .... TOTAL Result Count = 0
RULECHECK Metal4.6 .... TOTAL Result Count = 0
RULECHECK Metal4.7 .... TOTAL Result Count = 0
RULECHECK Metal4.8 .... TOTAL Result Count = 0
RULECHECK Metal5.5 .... TOTAL Result Count = 0
RULECHECK Metal5.6 .... TOTAL Result Count = 0
RULECHECK Metal5.7 .... TOTAL Result Count = 0
RULECHECK Metal5.8 .... TOTAL Result Count = 0
RULECHECK Metal6.5 .... TOTAL Result Count = 0
RULECHECK Metal6.6 .... TOTAL Result Count = 0
RULECHECK Metal6.7 .... TOTAL Result Count = 0
RULECHECK Metal6.8 .... TOTAL Result Count = 0
RULECHECK Metal7.5 .... TOTAL Result Count = 0
RULECHECK Metal7.6 .... TOTAL Result Count = 0
RULECHECK Metal7.7 .... TOTAL Result Count = 0
RULECHECK Metal8.5 .... TOTAL Result Count = 0
RULECHECK Metal8.6 .... TOTAL Result Count = 0
RULECHECK Metal8.7 .... TOTAL Result Count = 0
RULECHECK Metal9.5 .... TOTAL Result Count = 0
RULECHECK Metal9.6 .... TOTAL Result Count = 0
RULECHECK Metal10.5 ... TOTAL Result Count = 0
RULECHECK Metal10.6 ... TOTAL Result Count = 0
RULECHECK Grid.1 ...... TOTAL Result Count = 0
RULECHECK Grid.2 ...... TOTAL Result Count = 0
RULECHECK Grid.3 ...... TOTAL Result Count = 0
RULECHECK Grid.4 ...... TOTAL Result Count = 0
RULECHECK Grid.5 ...... TOTAL Result Count = 0
RULECHECK Grid.6 ...... TOTAL Result Count = 0
RULECHECK Grid.7 ...... TOTAL Result Count = 0
RULECHECK Grid.8 ...... TOTAL Result Count = 0
RULECHECK Grid.9 ...... TOTAL Result Count = 0
RULECHECK Grid.10 ..... TOTAL Result Count = 0
```

```
RULECHECK Grid.11 ..... TOTAL Result Count = 0
RULECHECK Grid.12 ..... TOTAL Result Count = 0
RULECHECK Grid.13 ..... TOTAL Result Count = 0
RULECHECK Grid.14 ..... TOTAL Result Count = 0
RULECHECK Grid.15 ..... TOTAL Result Count = 0
RULECHECK Grid.16 ..... TOTAL Result Count = 0
RULECHECK Grid.17 ..... TOTAL Result Count = 0
RULECHECK Grid.18 ..... TOTAL Result Count = 0
RULECHECK Grid.19 ..... TOTAL Result Count = 0
RULECHECK Grid.20 ..... TOTAL Result Count = 0
RULECHECK Grid.21 ..... TOTAL Result Count = 0
RULECHECK Grid.22 ..... TOTAL Result Count = 0
RULECHECK Grid.23 ..... TOTAL Result Count = 0
RULECHECK Grid.24 ..... TOTAL Result Count = 0
RULECHECK Grid.25 ..... TOTAL Result Count = 0
RULECHECK Grid.26 ..... TOTAL Result Count = 0
--------------------------------------------------------------------------------
-
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 54
TOTAL DRC RuleChecks Executed:   156
TOTAL DRC Results Generated:     0
```

LVS Report

```
                ################################################
                ##                                            ##
                ##        C A L I B R E   S Y S T E M         ##
                ##                                            ##
                ##            L V S   R E P O R T             ##
                ##                                            ##
                ################################################



REPORT FILE NAME:         Inverter.lvs.report
LAYOUT NAME:              Inverter.calibre.db
SOURCE NAME:              /u/erpina/cadence/LVS-files/Inverter.src.net
('Inverter')
RULE FILE:                /u/erpina/cadence/LVS-files/_calibreLVS.rul_
RULE FILE TITLE:          LVS Rule File for FreePDK45
LVS MODE:                 Mask
RULE FILE NAME:           /u/erpina/cadence/LVS-files/_calibreLVS.rul_
CREATION TIME:            Wed Feb 22 21:21:43 2017
CURRENT DIRECTORY:        /u/erpina/cadence/LVS-files
USER NAME:                erpina
CALIBRE VERSION:          v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013
```

```
********************************************************************************
*****************************
                                OVERALL COMPARISON RESULTS
********************************************************************************
*****************************

                          #       ###################       _   _
                        #         #                 #       *   *
                    #   #         #     CORRECT     #         |
                     # #          #                 #       \___/
                       #          ###################


--------------------------------------------------------------------------------
-----------------------------

NUMBERS OF OBJECTS
------------------

                 Layout    Source         Component Type
                 ------    ------         --------------
 Nets:                4         4

 Instances:           1         1         mn (4 pins)
                      1         1         mp (4 pins)
                 ------    ------
 Total Inst:          2         2



********************************************************************************
*****************************
                                       LVS PARAMETERS
********************************************************************************
*****************************


o LVS Setup:

   LVS COMPONENT TYPE PROPERTY            element
   LVS COMPONENT SUBTYPE PROPERTY         model
   // LVS PIN NAME PROPERTY
   LVS POWER NAME                         "VDD"
   LVS GROUND NAME                        "VSS" "GROUND"
   LVS CELL SUPPLY                        NO
   LVS RECOGNIZE GATES                    ALL
   LVS IGNORE PORTS                       YES
   LVS CHECK PORT NAMES                   NO
   LVS IGNORE TRIVIAL NAMED PORTS         NO
   LVS BUILTIN DEVICE PIN SWAP            YES
```

```
LVS ALL CAPACITOR PINS SWAPPABLE       NO
LVS DISCARD PINS BY DEVICE             NO
LVS SOFT SUBSTRATE PINS                NO
LVS INJECT LOGIC                       YES
LVS EXPAND UNBALANCED CELLS            YES
LVS FLATTEN INSIDE CELL                NO
LVS EXPAND SEED PROMOTIONS             NO
LVS PRESERVE PARAMETERIZED CELLS       NO
LVS GLOBALS ARE PORTS                  YES
LVS REVERSE WL                         NO
LVS SPICE PREFER PINS                  NO
LVS SPICE SLASH IS SPACE               YES
LVS SPICE ALLOW FLOATING PINS          YES
// LVS SPICE ALLOW INLINE PARAMETERS
LVS SPICE ALLOW UNQUOTED STRINGS       NO
LVS SPICE CONDITIONAL LDD              NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS   NO
LVS SPICE IMPLIED MOS AREA             NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS             NO
LVS SPICE REDEFINE PARAM               NO
LVS SPICE REPLICATE DEVICES            NO
LVS SPICE SCALE X PARAMETERS           NO
LVS SPICE STRICT WL                    NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                    NO
LVS EXACT SUBTYPES                     NO
LAYOUT CASE                            NO
SOURCE CASE                            NO
LVS COMPARE CASE                       NO
LVS DOWNCASE DEVICE                    NO
LVS REPORT MAXIMUM                     50
LVS PROPERTY RESOLUTION MAXIMUM        32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                       YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction

LVS REDUCE SERIES MOS                  YES
LVS REDUCE PARALLEL MOS                YES
LVS REDUCE SEMI SERIES MOS             YES
LVS REDUCE SPLIT GATES                 YES
LVS REDUCE PARALLEL BIPOLAR            YES
LVS REDUCE SERIES CAPACITORS           YES
LVS REDUCE PARALLEL CAPACITORS         YES
LVS REDUCE SERIES RESISTORS            YES
LVS REDUCE PARALLEL RESISTORS          YES
LVS REDUCE PARALLEL DIODES             YES
LVS REDUCTION PRIORITY                 PARALLEL
```

```
   LVS SHORT EQUIVALENT NODES              NO

   // Trace Property

   TRACE PROPERTY  mn(nmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  w w 4e-09 ABSOLUTE


********************************************************************************
*****************************
                              INFORMATION AND WARNINGS
********************************************************************************
*****************************


                  Matched    Matched    Unmatched    Unmatched    Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    ---------
   Nets:               4          4            0            0

   Instances:          1          1            0            0    mn(NMOS_VTL)
                       1          1            0            0    mp(PMOS_VTL)
                  -------    -------    ---------    ---------
   Total Inst:         2          2            0            0


o Initial Correspondence Points:

   Nets:         gnd! vdd! A Y


********************************************************************************
*****************************
                                        SUMMARY
********************************************************************************
*****************************

Total CPU Time:      0 sec
```

```
Total Elapsed Time:  0 sec
```