Standard Cell Template

RESISTOR LONG LOAD INVERTER

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Introduction and Physical Properties

Cell Description

In a Resistive load invertor, the p-mos transistor of a CMOS inverter is replaced by a resistive load. Here, the enhancement type, n-mos acts as the driver transistor. The load consists of linear resistor. When the input is low(vin<vth), the transistor is in off condition and current flows through the resistor from vdd to ground and the output voltage is high(vdd). When the input is high(vin>vth), the transistor starts to conduct that results in decrease of output voltage.

Cell Symbol

Where applicable use standard logic symbols (i.e. INVERTER, NAND, NOR, AOI has a standard symbol) for the assigned standard cells. This will require editing the symbol after Cadence NSCU CDK creates the boring square or rectangular default symbol. [Note: There are two "extra" pins inside the inverter symbol. These pins may be needed for a workaround when simulating the extracted view of the physical design later in the term and next quarter. The top symbolic pin is for the VDD and the lower for GND. If they are not needed they can be dropped in the schematic as well as in this picture.]

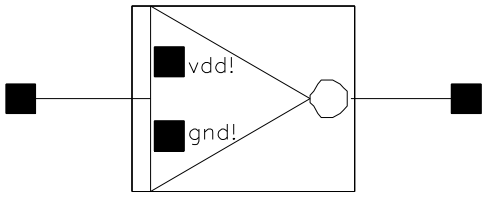

Figure 1: Example Logic Symbol from NCSU Digital Parts. All symbols are 1in tall.

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Cell Truth Table

Complete the truth table for all cell outputs using {0, 1} for the input low and high, respectively and {L, H} for the output low and high, respectively. Repeat rows and columns as needed.

INPUT	OUTPUT
1	L
0	H

Cell Schematic Diagram

Prepare Encapsulated Postscript of the schematic for publication (Cadence has this option in the Virtuoso schematic design). Do not use a screen shot or create Encapsulated Postscript of the raw schematic. For each "publication schematic" in NSCU CDK remove the transistor width and length, model name etc. but leave the instance names of the pins and transistor. This makes the schematic easier to read.

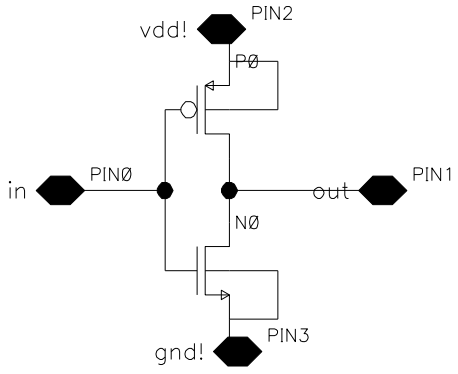

Figure 2: Example Schematic from NCSU CDK Publication Schematic. All schematic figure are 2in tall.

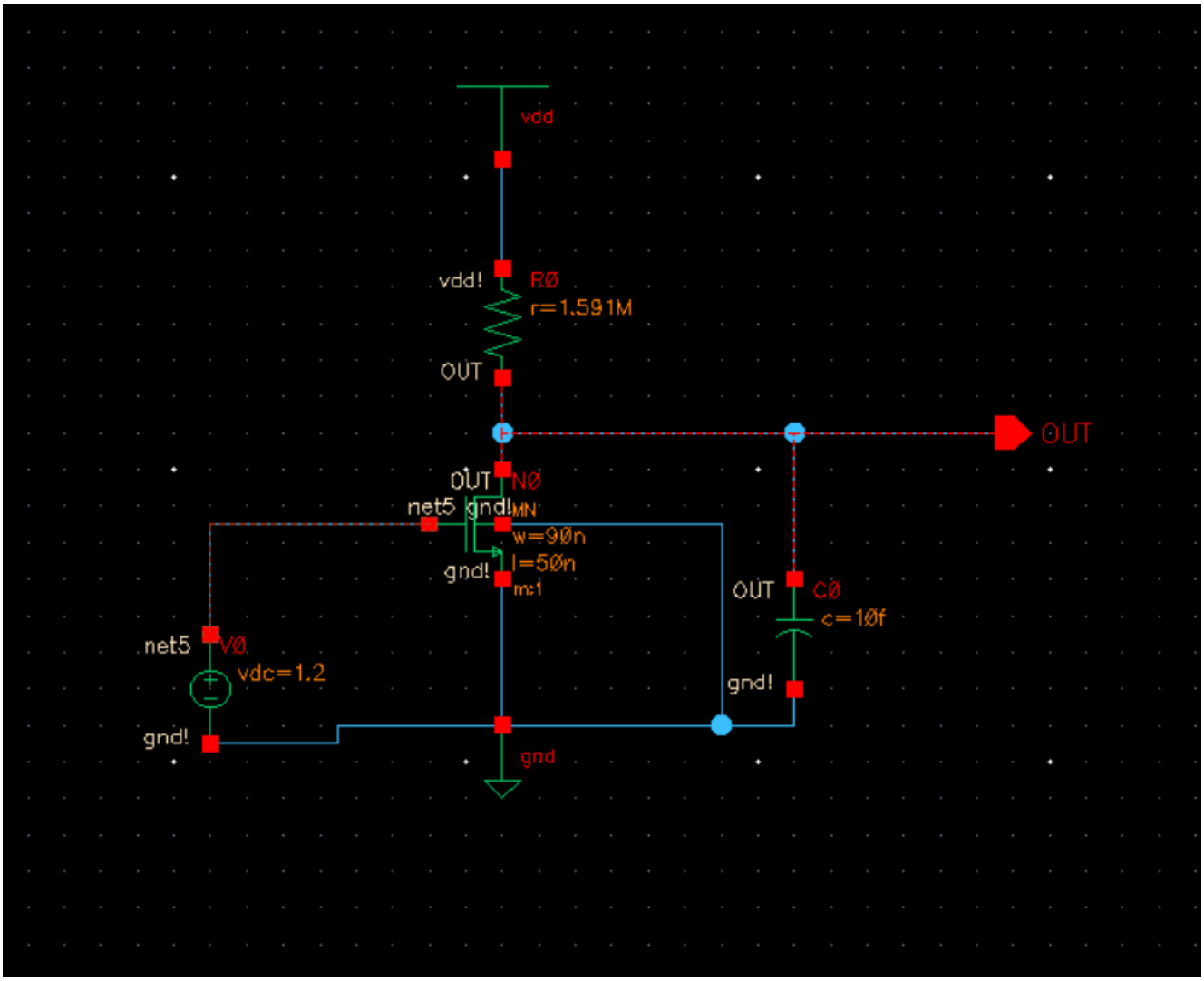

Figure 3: Schematic of CMOS resistive load inverter for dc analysis

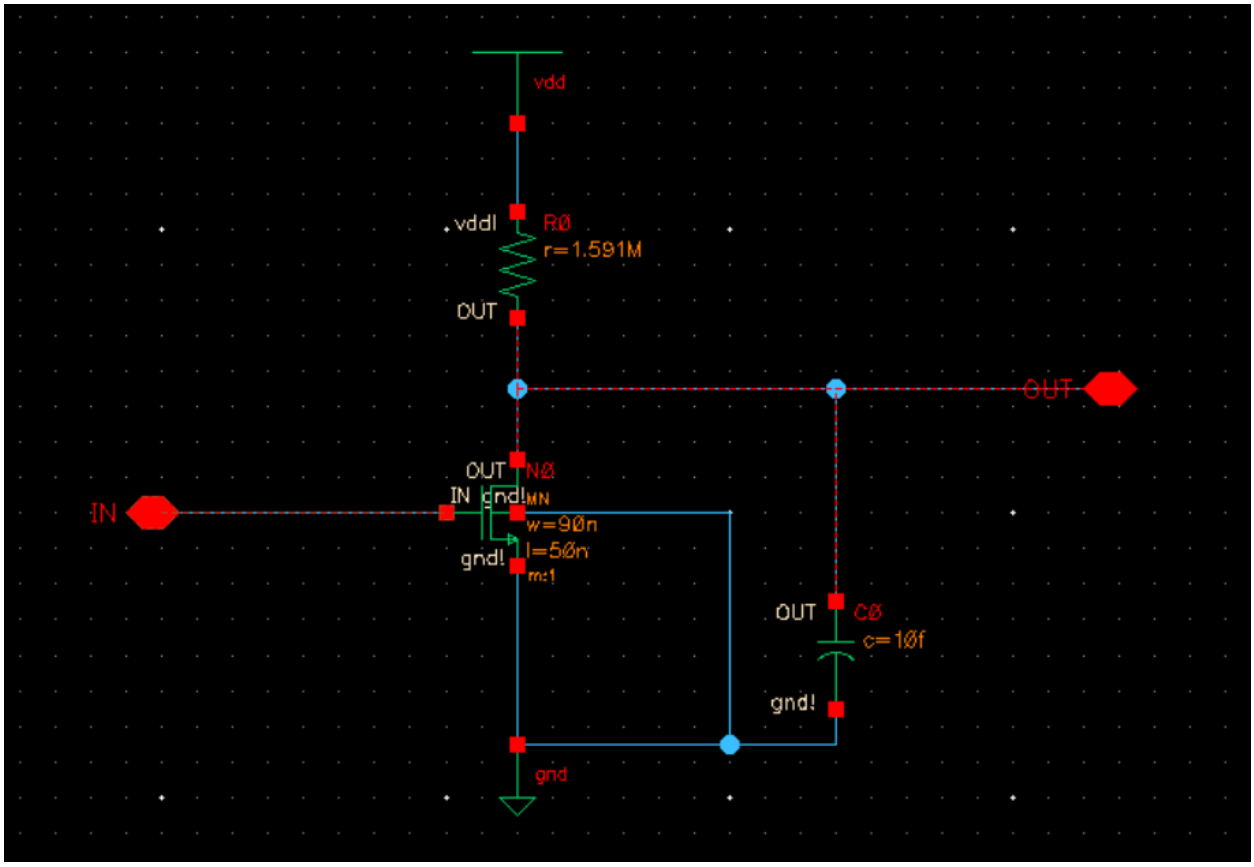

Figure 4: Schematic of CMOS resistive load inverter for transient analysis

Cell Layout Diagram and Dimensions

Save a color or black and white layout of the cell in EPS (i.e. Encapsulated Postscript) format. The cell dimensions are saved in both lambda (□) and microns (□m). Record the transistor length and width dimensions (nm).
[Repeat the transistor row as needed.]

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Cell Physical Dimensions		
	X	Y
Cell Dimension in □□		
Cell Dimension in □m		
Transistor Dimensions		
Transistor Instance Number	Length (nm)	Width (nm)
N1	50	90

Input and Output Parasitic Capacitance Table

From the schematic calculate each input's capacitance normalized to the nominal inverter (your inverter standard cell) by the width of the transistor or drain area as needed. This entry should be an integer fraction similar to Weste and Harris. [Note the normalization is to a standard inverter (the standard cell inverter INV1X). Repeat the rows as needed.]

Computed Cell Input Capacitance	
Input Name	**Capacitance (/Cinv)**
Output Name	**Capacitance (/Cinv)**

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Performance Analysis

Rise and Fall Times

[Note: It is highly desirable to split the simulation work load among the team members so that each team member learns how to use the tools.]

FOx denotes output loads. The loads are defined by the number of identical logic gates. Use 20%-80% swings for the output rise and fall entries. Use a 1.2V power supply.

For each output load in the table complete transient simulations. Remember to include a CMOS non-inverting buffer between the ideal voltage source and the logic gate driving the FOx load. Note rise t_r / fall t_f times are at the input to the logic gate driving the load, **not** the rise/fall times for the input ideal voltage source.

Complete the number needed copies (copies = No. input stacks x No. outputs) of the table below.

For multi-input gates, complete tables for each transistor stack (i.e. each branch connected to the output) using the stack's worst case single controlling input transition in the stack. Label the tables with worst case input in each stack and the output. Replace **X** below with the signal name.

Input X: Output Rise Time Data t_r (ns)					
Input rise/fall time (ns)	Output Load (FOx) 0	1	2	4	8
0.04				14.7879	
0.06					

Stack Input Combination: ***Replace with Boolean Product***

Stack S, Input X: Output Fall Time Data t_f (ns)					
Input rise/fall time (ns)	Output Load (FOx) 0	1	2	4	8
0.04				ND	
0.06					

Stack Input Combination: ***Replace with Boolean Product***

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Propagation Delays

For the range of output loads shown in the table simulate propagation delays (low to high t_{plh} and high to low t_{phl}) for the stack's worst case single controlling input transition. The input controlling the output is the same input reported in the rise and fall time section. Use a 1.2V power supply and timing measurements start when input to the logic gate driving the FOx load crosses the 50% of the rail and stop when the logic gate driving output crosses 50% of the rail. Negative values are entered as 0.

Label the tables with the Boolean product (e.g. AB) of the transistor stack and the output. Complete copies of the table below for each branch connected to the output.

Data Worst Case Low to High Propagation Delay Data t_{plh} (ns)					
Input rise/fall time (ns)	Output Load (FOx) 0	1	2	4	8
0.04				8.8354	
0.06					

Worse Case Input Combination: ***Replace with Boolean Product***

Data Worst Case High to Low Propagation Delay Data t_{phl} (ns)					
Input rise/fall time (ns)	Output Load (FOx) 0	1	2	4	8
0.04				ND	
0.06					

Worse Case Input Combination: ***Replace with Boolean Product***

From each row of the slew rate data compute the best fit linear propagation delay equation for low-to-high T_{plh} (h) and high-to-low T_{phl} (h). The model predicts a delay, in nanoseconds, as a function of the output load, *h*, *Cout/Cin =FOx*. The model line is parameterized by a slope, *m*, and an intercept, *b*. The units of *m* are (*ns/FOx*) and the units of *b* are *ns*.

Complete the table below by increasing the number of rows for multiple input gates. The row labeled **All data** is the computed slope and intercept after combining data from all slew rates.

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Complete the **Model** row for the gate using the assumptions and methods of the linear delay model from Weste and Harris. Only skewed standard cells will have different values propagation models for rising and falling inputs.

All data means combine the results for both slew rates into a single model.

Discuss in your own words the differences in the calibration and the Weste Harris linear delay model. Discuss the differences in high-to-low versus low-to-high models.

Data Model Propagation Delay Equation $T_{pd}(h) = b + m \cdot h$				
Input Slew Rate (ns) (b_r)	Rising Logical Effort (m_r)	Falling Logical Effort (m_f)	Parasitic Rising Delay (b_r)	Parasitic Falling Delay
0.04				
0.06				
All data				

In the table below normalize the model for the T_{pd} (h) results of the table above to give the logical effort model *D(h)* described in Weste and Harris. *D(h)* is a unitless value and predicts the delay as multiples of the standard inverter delay. Normalization is based on the observed CMOS inverter parasitic delay, b_{inv}. ***Recall all data*** $p_{inv} \approx 1$.

Inverter Normalized Data Model Propagation Delay Equation $D(h) = p + g \cdot h$				
Input Slew Rate (ns)	Rising Logical Effort (g_r)	Falling Logical Effort (g_f)	Parasitic Rising Delay (p_r)	Parasitic Falling Delay (p_r)
0.04				
0.06				
All data				
W&H Model				

Power-Delay

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Simulate the cell for a sequence of input combinations based on the Gray code and compute the time averaged power (mW), average delay (ns), and average powerdelay product (mW ns = pJ). The Gray code restricts the simulations to single input transitions and ignores the large number of multiple input change combinations. Use the same slew rate for all input transitions. Use equal output loads for multiple output gates. Use a period of 2X maximum output delay with FO=8.

Average Power Data (mW)					
Input Slew (ns)	Output Load (FOx) 0	1	2	4	8
0.04					
0.06					

verage Delay Data (ns)					
Input Slew (ns)	Output Load (FOx) 0	1	2	4	8
0.04					
0.06					

Average Power-Delay Data (pJ)					
Input Slew (ns)	Output Load (FOx) 0	1	2	4	8
0.04					
0.06					

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Tabulation for comparison of the transient and the dc values:

Type	V_{IH}	$V_{IL\_DC(mV)}$	$V_{OH\_DC(mV)}$	$V_{OL\_DC(mV)}$
CMOS	776.968	423.915	986.5602	28.4789
CMOS Wide	777.124	423.78	986.451	28.9607
Diode	692.016	223.881	720.316	91.83267
Diode Long	561.361	200.001	721.7334	47.52194
Resistor	692.015	245.192	991.444	38.4126
Resistor Long	**561.361**	**200.392**	**998.288**	**9.36811**

Type	$V_{OH\_TRAN\ (mV)}$	$V_{OL\_TRAN\ (mV)}$	t_{plh}	t_{phl}	t_r	t_f
CMOS	953.043	256.937	0.2295	0.1091	0.3332	0.14847
CMOS Wide	912.533	201.419	0.056	0.0291	0.0687	0.0315
Diode	712.0589	360.8567	0.63637	ND	2.3493	ND
Diode Long	719.7788	224.3859	2.48685	ND	0.6339	ND
Resistor	1078.4	314.256	1.8455	ND	3.7316	ND
Resistor Long	**993.737**	**112.357**	**8.8354**	**ND**	**14.7879**	**ND**

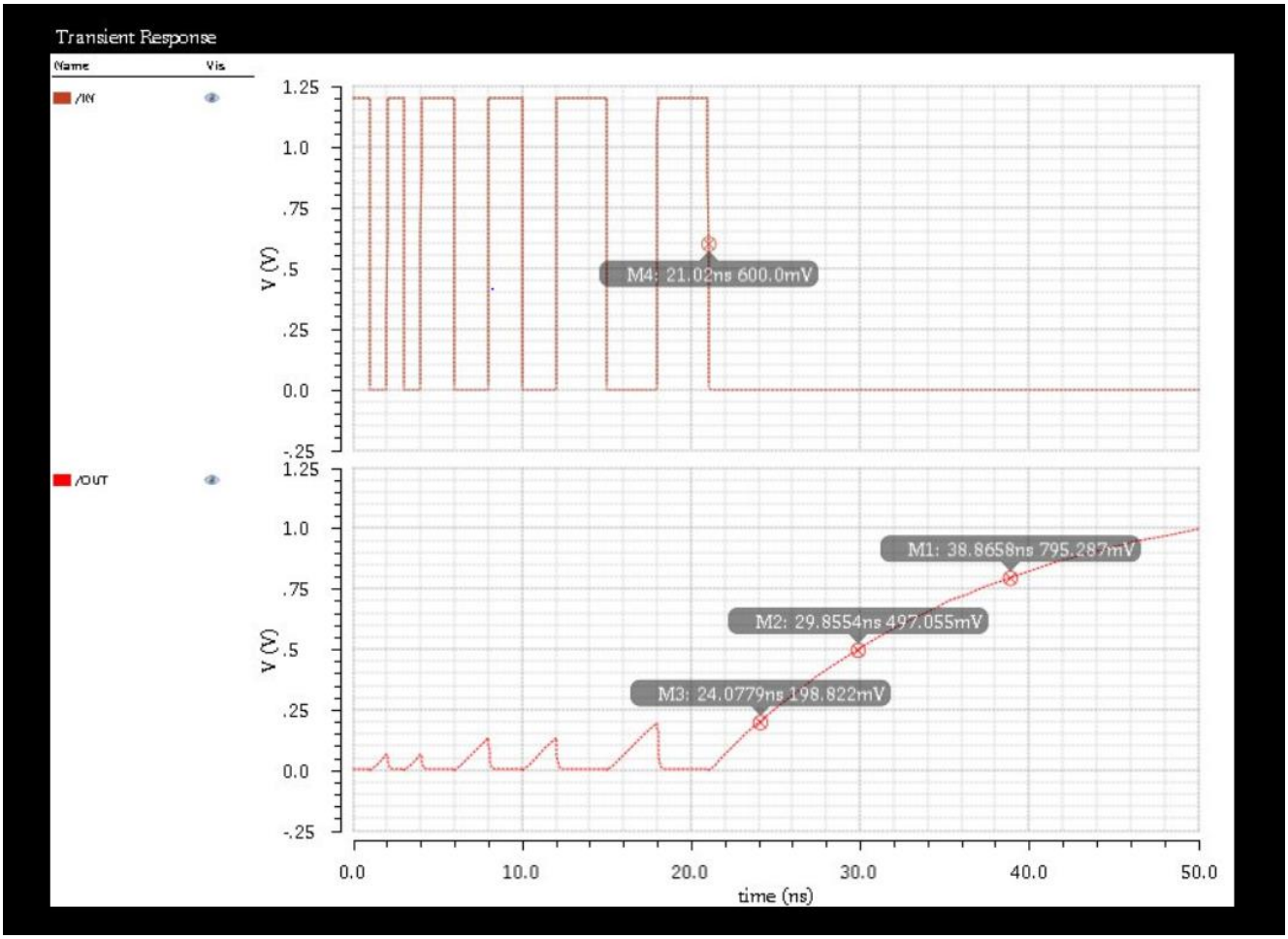

Figure 5: Transient analysis of the resistive long load inverter

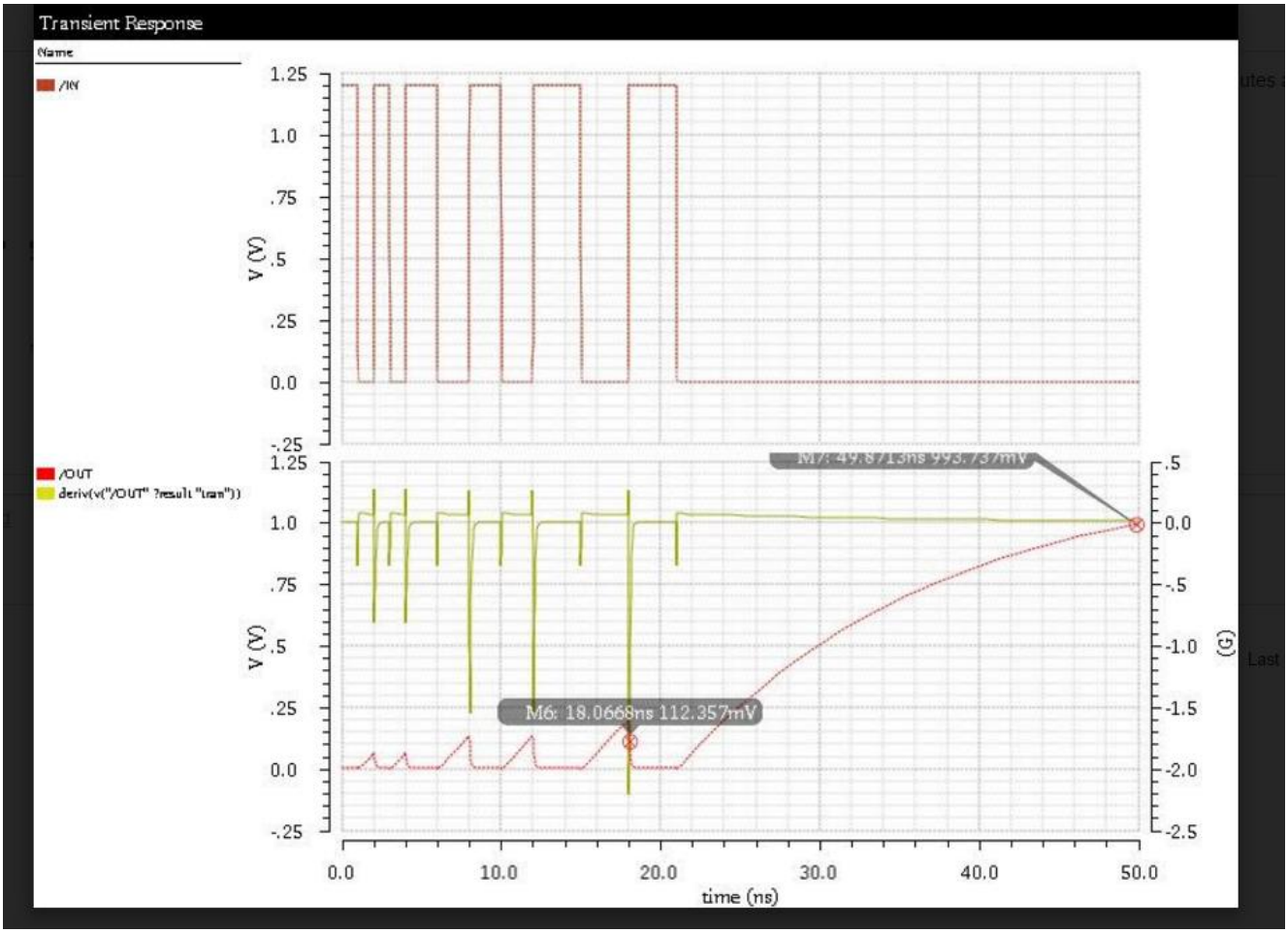

Figure 6: Transient analysis of the resistive long load inverter

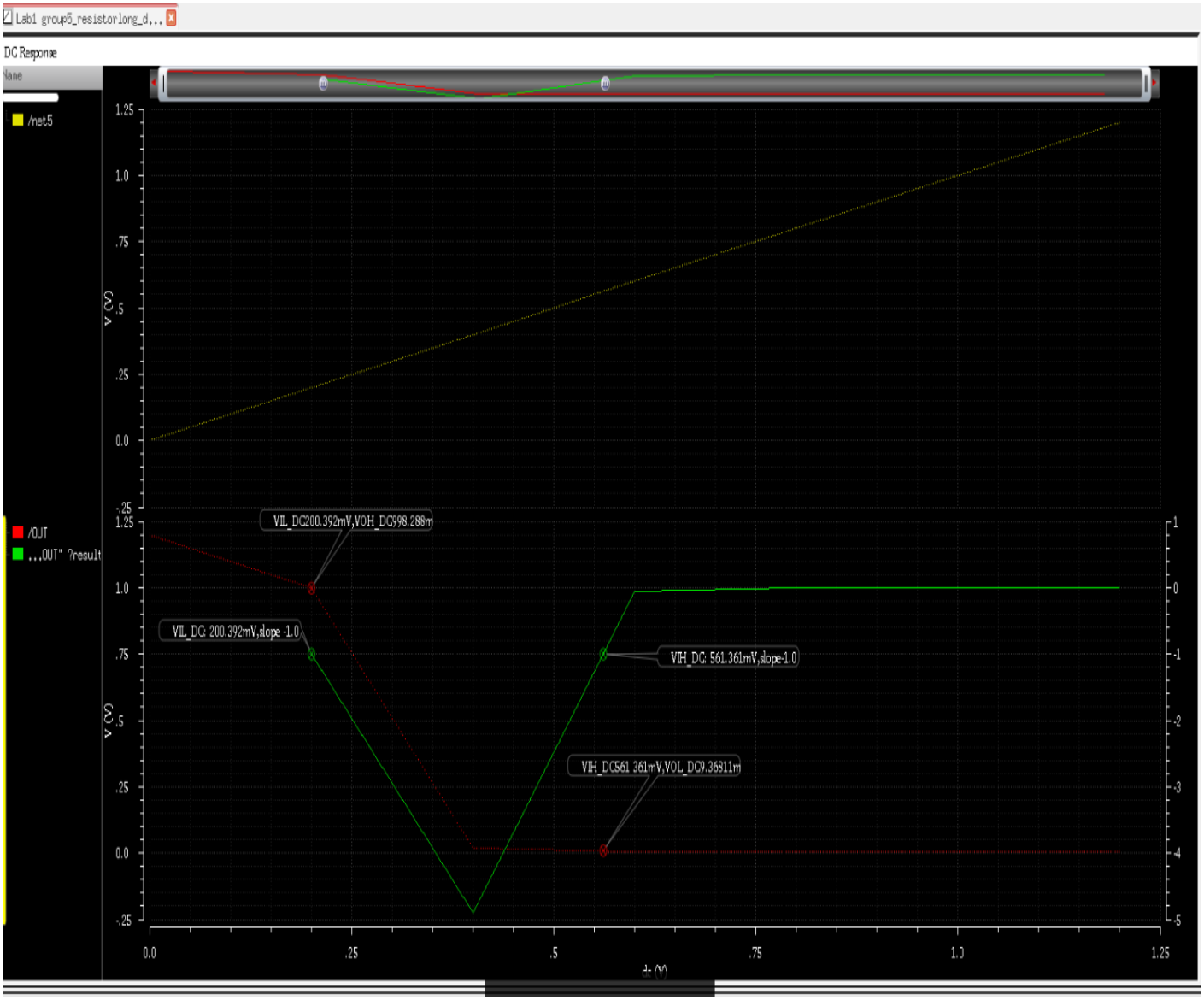

Figure 7: DC analysis of the resistive long load inverter

3. Explain in your own words the variation of the DC output voltages VOH and VOL for the four inverters? In particular focus on the differences noted earlier in the diode connected inverters.

Ans:

- The VOH_DC, VOL_DC values of CMOS and CMOS Wide inverter circuits do not have much variation. This means that variation in the width of the gate of the pull up transistor doesn't effect much with VOL_DC, VOH_DC.
- The Resistor invertor circuit is similar to MOS circuit but the Resistor also has internal capacitance, which again affects the V_OH and V_OL.
- As we observe the V_OH and V_OL values of the CMOS and diode, the V_OH values of diode are less when compared to CMOS and V_OL value is more than that of CMOS, because in CMOS the pull-up network (p-MOS) always offers resistance, which is less in case of diode. This indicates that even for low power input, the output is driven in case of diode load inverter.

4. Explain in your own words the variation of the propagation times tplh and tphl for the four inverters?

Ans:

The propagation delay for CMOS _Wide is less than that of CMOS, since there is more space for the electrons to drift through from source to drain. So, the current flow is high which results in high magnitude of charge reaching the source from drain in a short time , which decreases the propagation delay value ,rise and fall times at the output.

The Channel length of resistor long inverter is greater than that of resistor inverter. So the tphl and tphl for resistor inverter is low compared to that of resistor long inverter. As the length increases, it takes more time for the Electrons to drift from source to drain which results in lesser drain current. Therefore, t plh and t phl is low for resistor inverter compared to that of Resistor Long inverter. Same is with the diode and the diode long as the resistance increases the time taken for the output to reflect change in the input is more.

So this is the tradeoff for the lower Vol value i.e vol decreases at the cost of the increased propagation delay.

CMOS configuration serves all purposes i.e. it has high output voltage to drive cascaded loads at the same time ,the propagation delay and the rise time and the fall time and ultimately the noise margin- due to low Vol and high Voh all are optimized. So its more preferred than any other configuration.