Inverter

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Group Number: 5

Date: 3/13/2017

Introduction and Physical Properties

Cell Description

A pair of complementary and symmetrical p-type and n-type metal oxide semiconductor field effect transistor are used for performing logic functions. CMOS has a number of advantages, where it offers power saving and less cost. Improvement in CMOS has made CMOS Sensors more suitable for cameras. For digital cameras, CMOS Sensors are much cheaper to produce and also have desirable power saving.

In this project we are trying to drive different loads (CMOS Inverters with minimum dimensions) with a Cmos Inverter whose dimensions are known.
The Design Under Test(DUT) which is the CMOS inverter drives those fanouts.

Thus schematics with various fanouts are used to draw the layout. The DRC report checks for any error in the desgin i.e., layout. The LVS report compares the layout and the schematic and checks for any errors. The PEX report gives the parasitic extraction. The power is also calculated.

CellSymbol

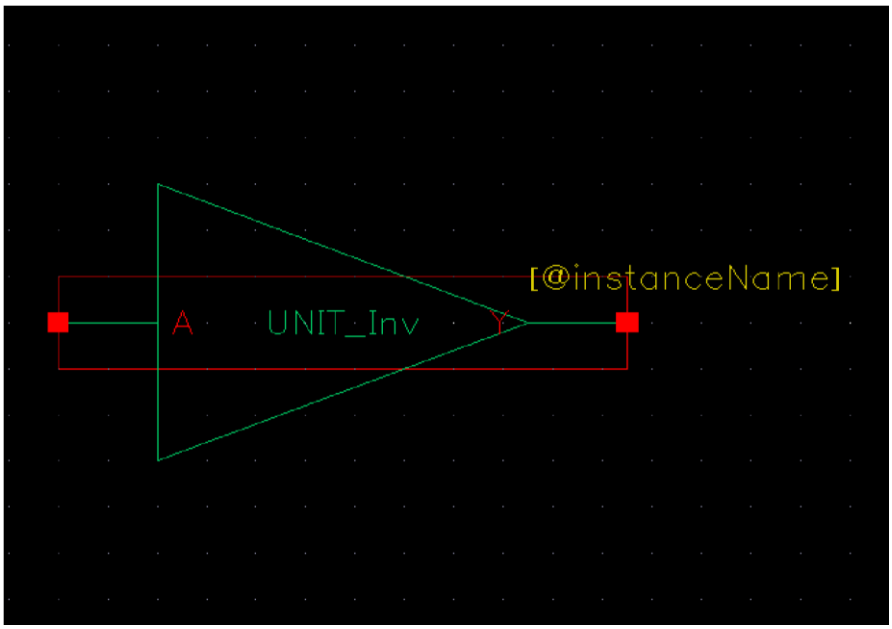


Figure 1: CMOS Unit Inverter circuit symbol.

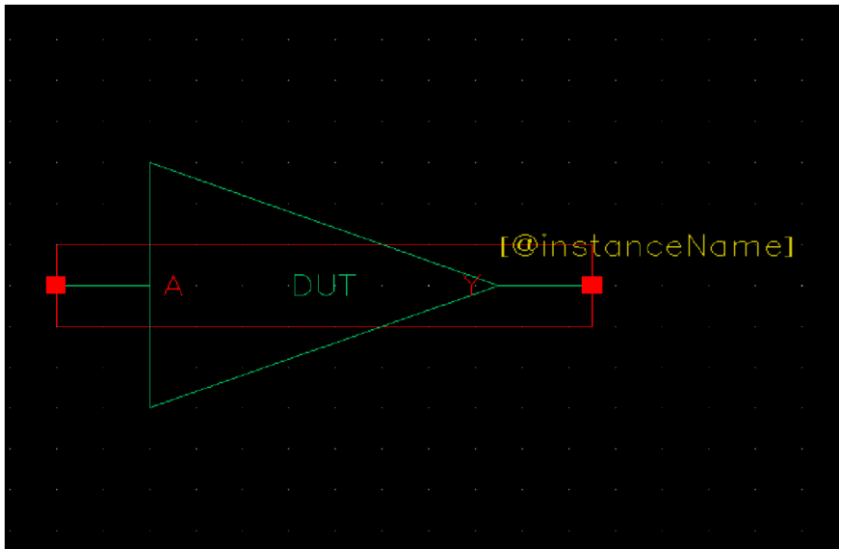


Figure 2: CMOS DUT Inverter circuit symbol.

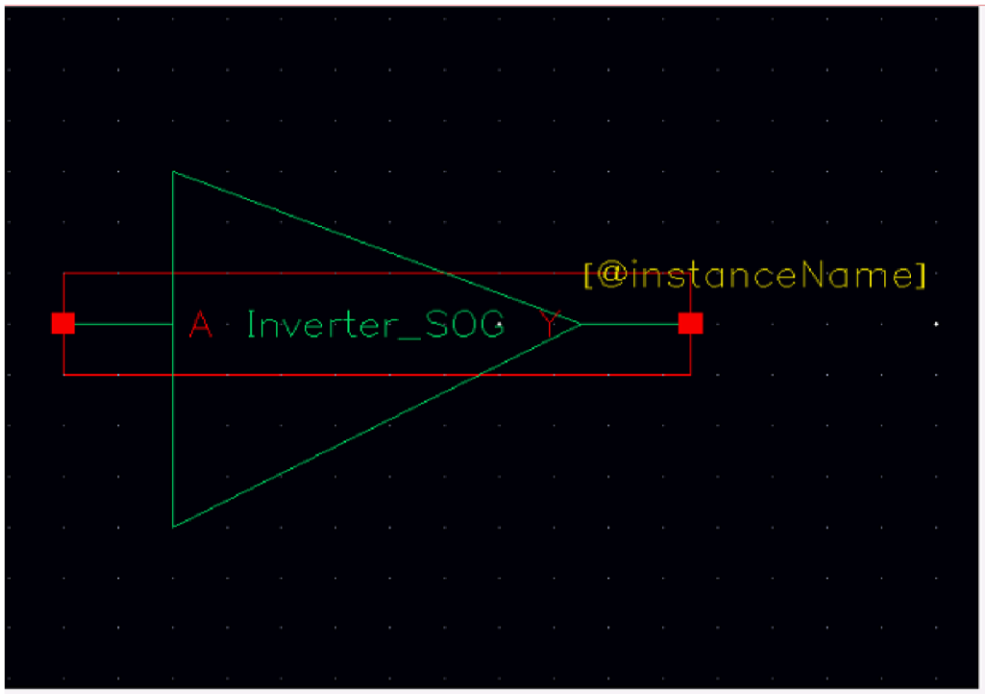


Figure 3: CMOS SOG Inverter circuit symbol

Cell Truth Table:

Truth table of the inverter is as shown below. We can observe that the output of the inverter is reverse of those respective inputs. Logic function is no different than that of Inverter, i.e.,

$$Q = \sim A$$

where Q is output and A is input.

Output	Input
H	0
L	1

Table 1: Inverter full custom truth table

Cell Schematic Diagram

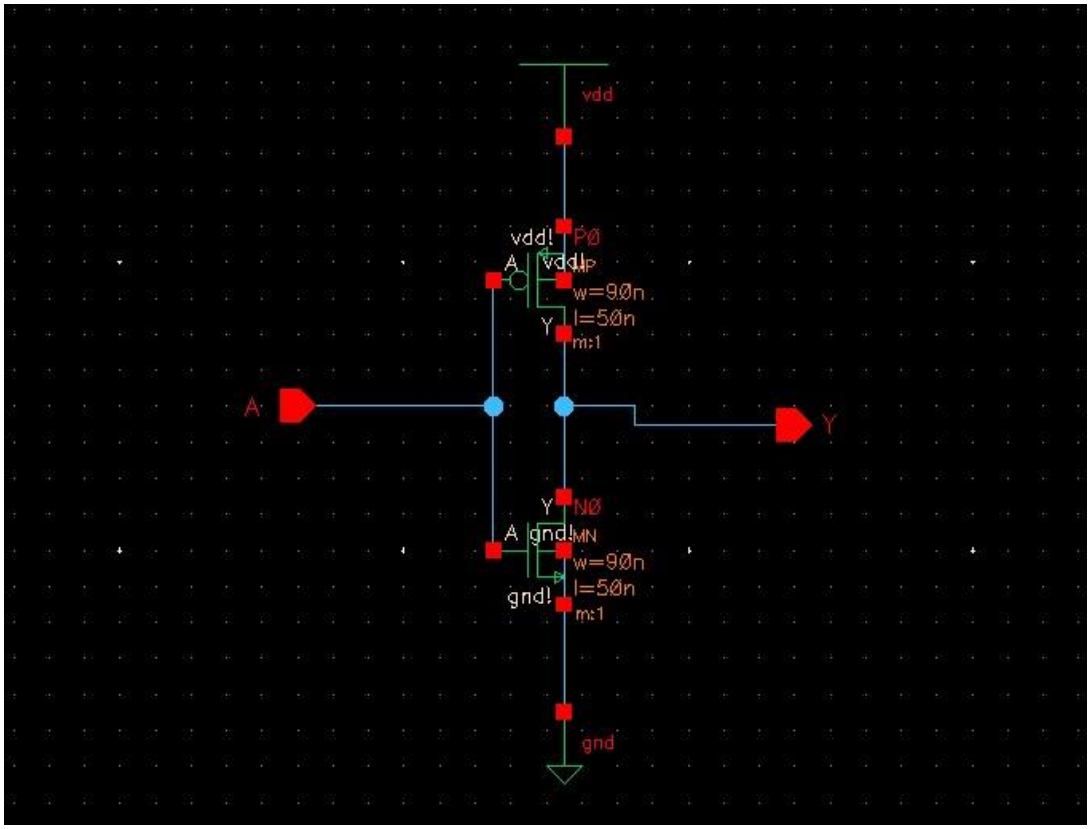


Figure 4: Schematic diagram of Unit Inverter

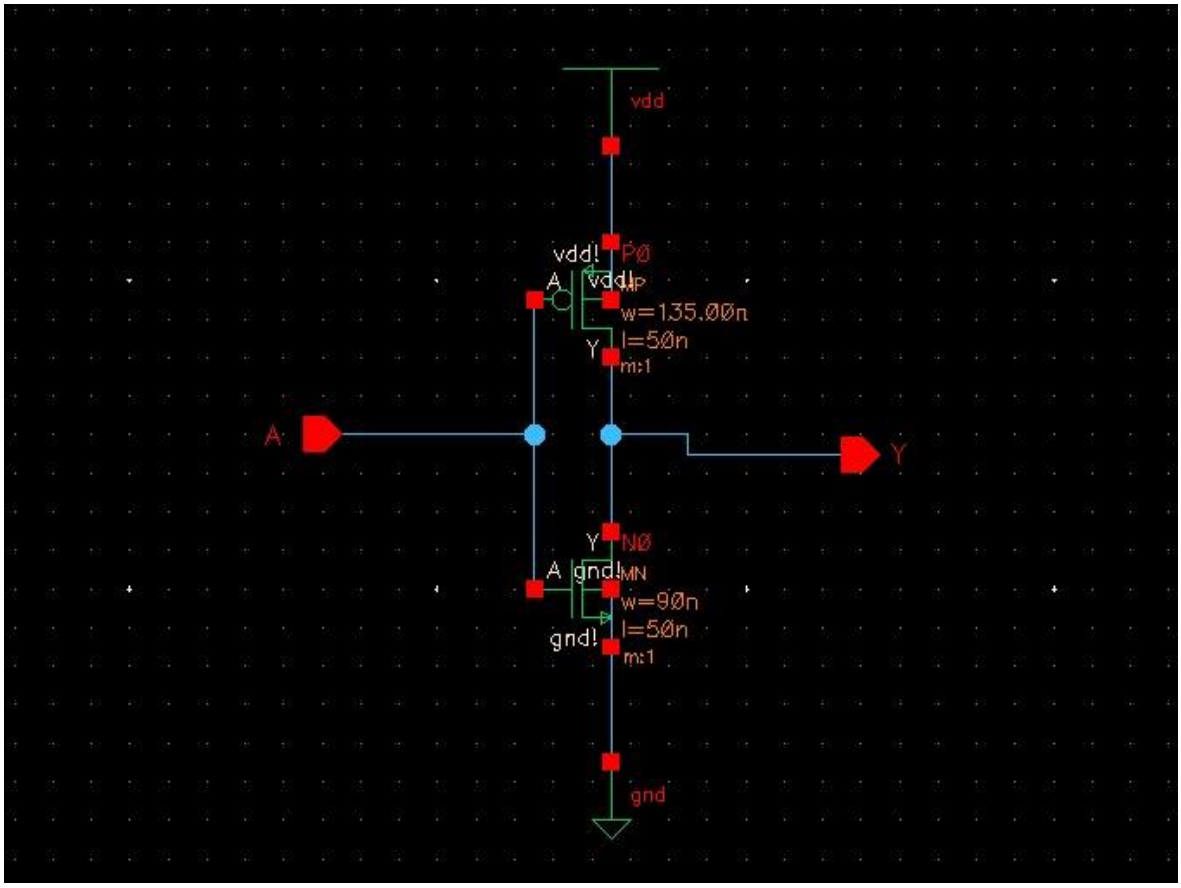


Figure 5: Schematic diagram of Full Custom Inverter

Transistor Dimensions

Save a color or black and white layout of the cell in EPS (i.e. Encapsulated Postscript) format. The cell dimensions are saved in both lambda (λ) and microns (μm). Record the transistor length and width dimensions (nm).

Cell Physical Dimensions		
Y	X	
		Cell Dimension in λ

		Cell Dimension in µm
Transistor Dimensions		
Width (nm)	Length (nm)	UNIT Name
135	50	PMOS P0
90	50	NMOS N1

Table 2: Custom Inverter Transistor Dimensions

Schematic diagrams of Custom Inverter :

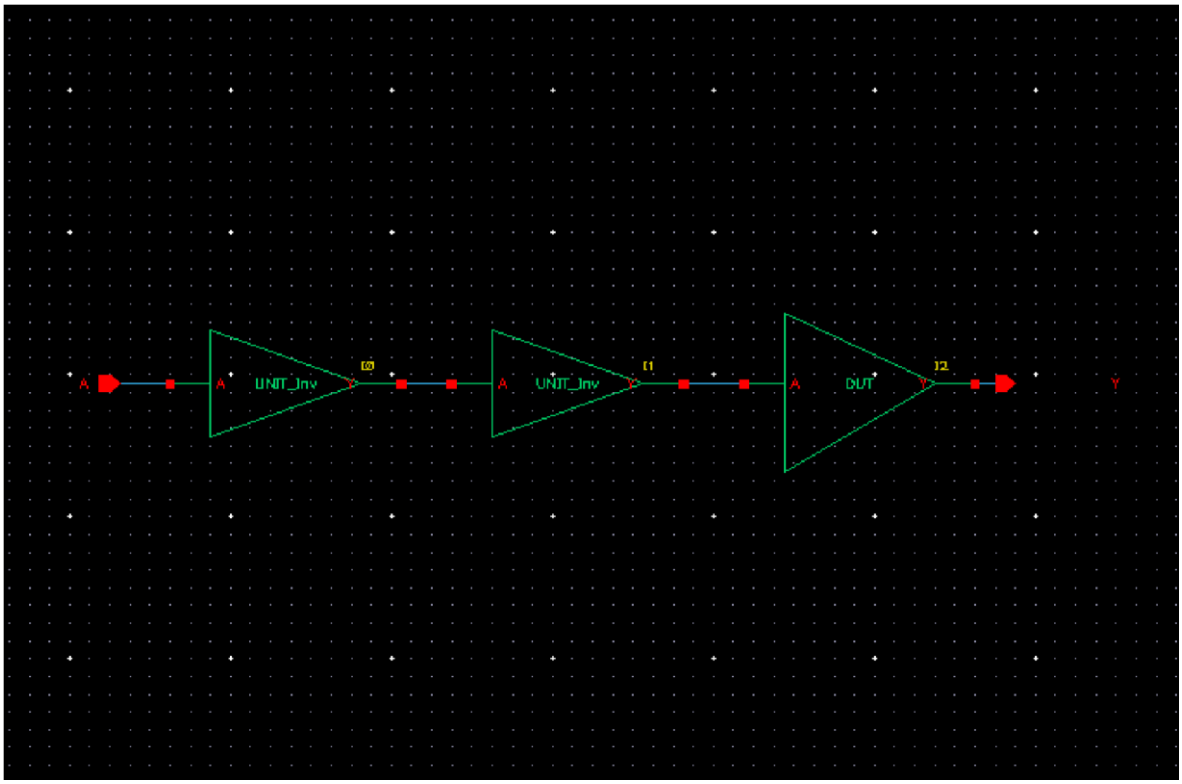


Figure 6: Schematic diagram of Custom Inverter with 0 fanout

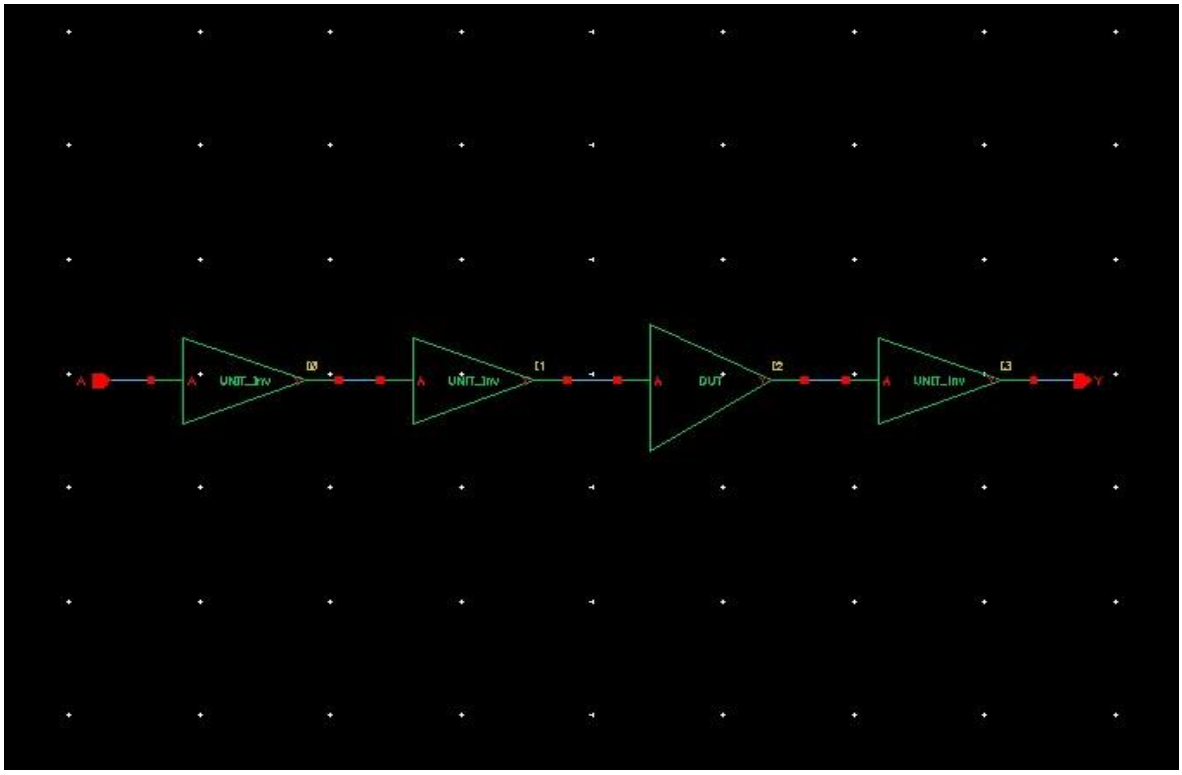


Figure 7: Schematic diagram of Custom Inverter with 1 fanout

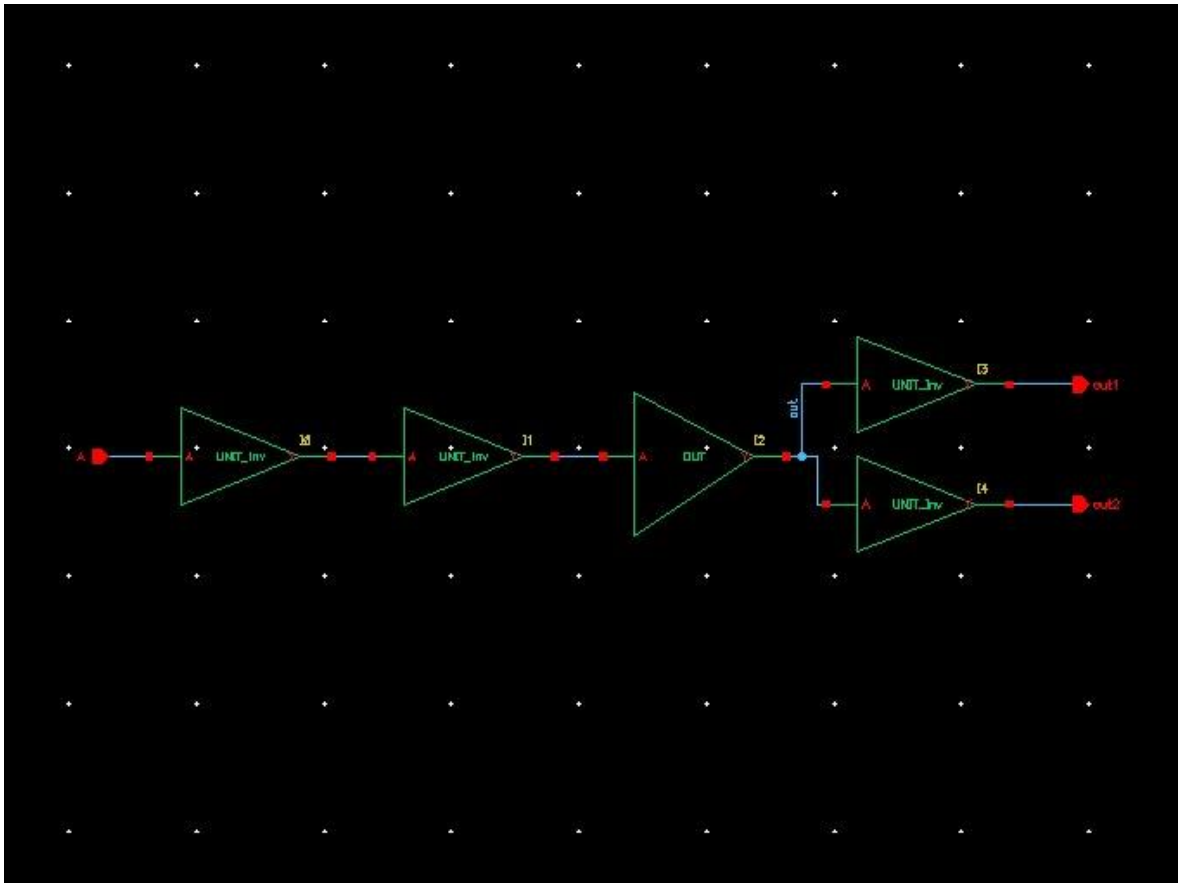


Figure 8: Schematic diagram of Custom Inverter with 2 fanouts

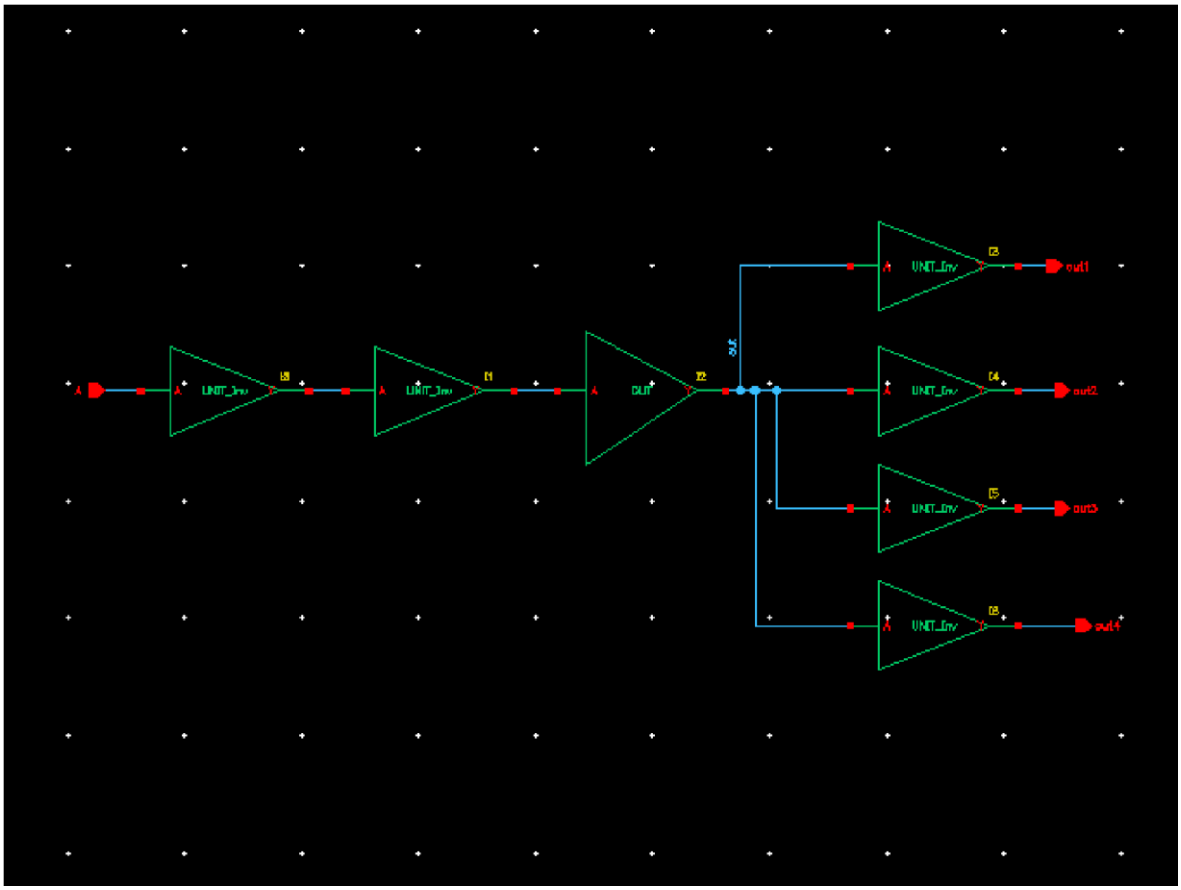


Figure 9: Schematic diagram of Custom Inverter with 4 fanouts

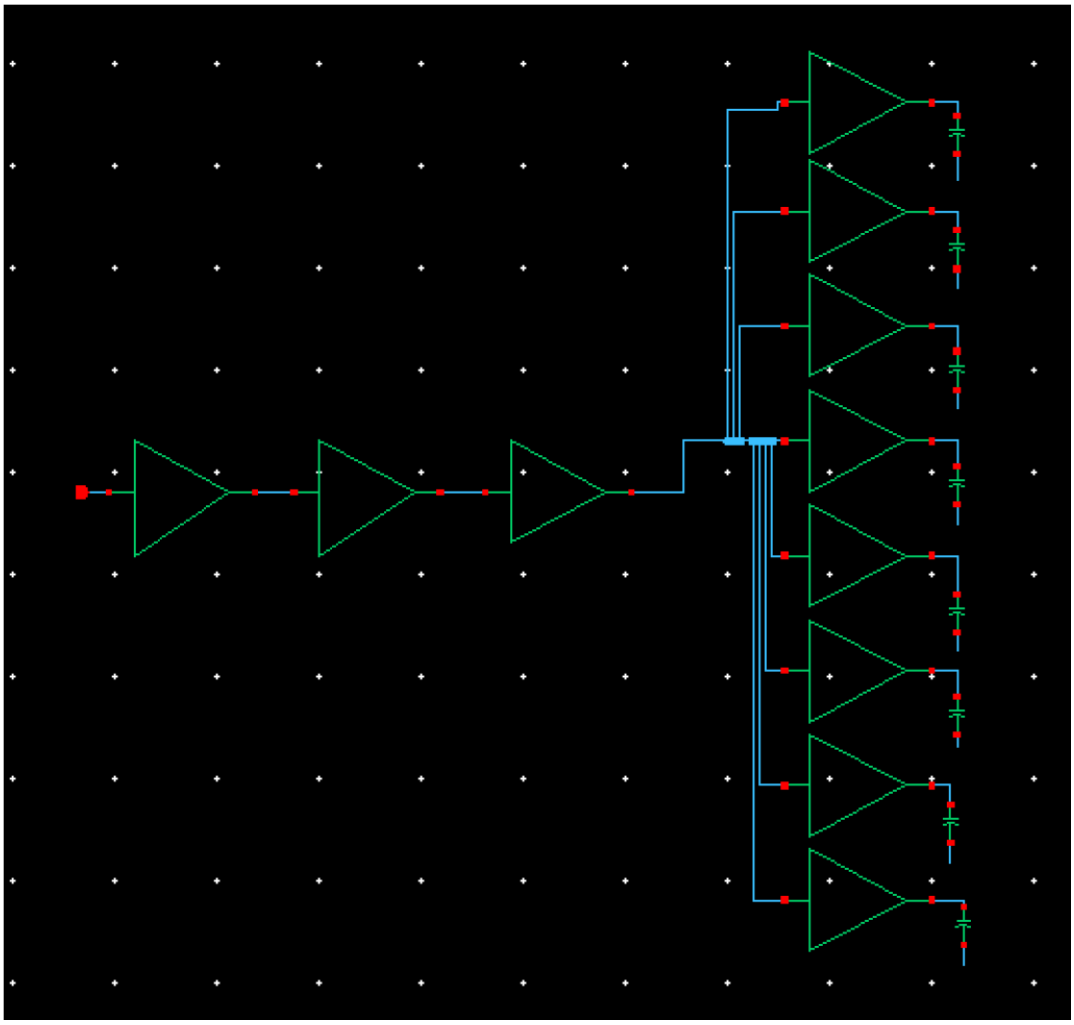


Figure 10: Schematic diagram of Custom Inverter with 8 fanouts

SOG INVERTER

Group 5 13th March, 2017

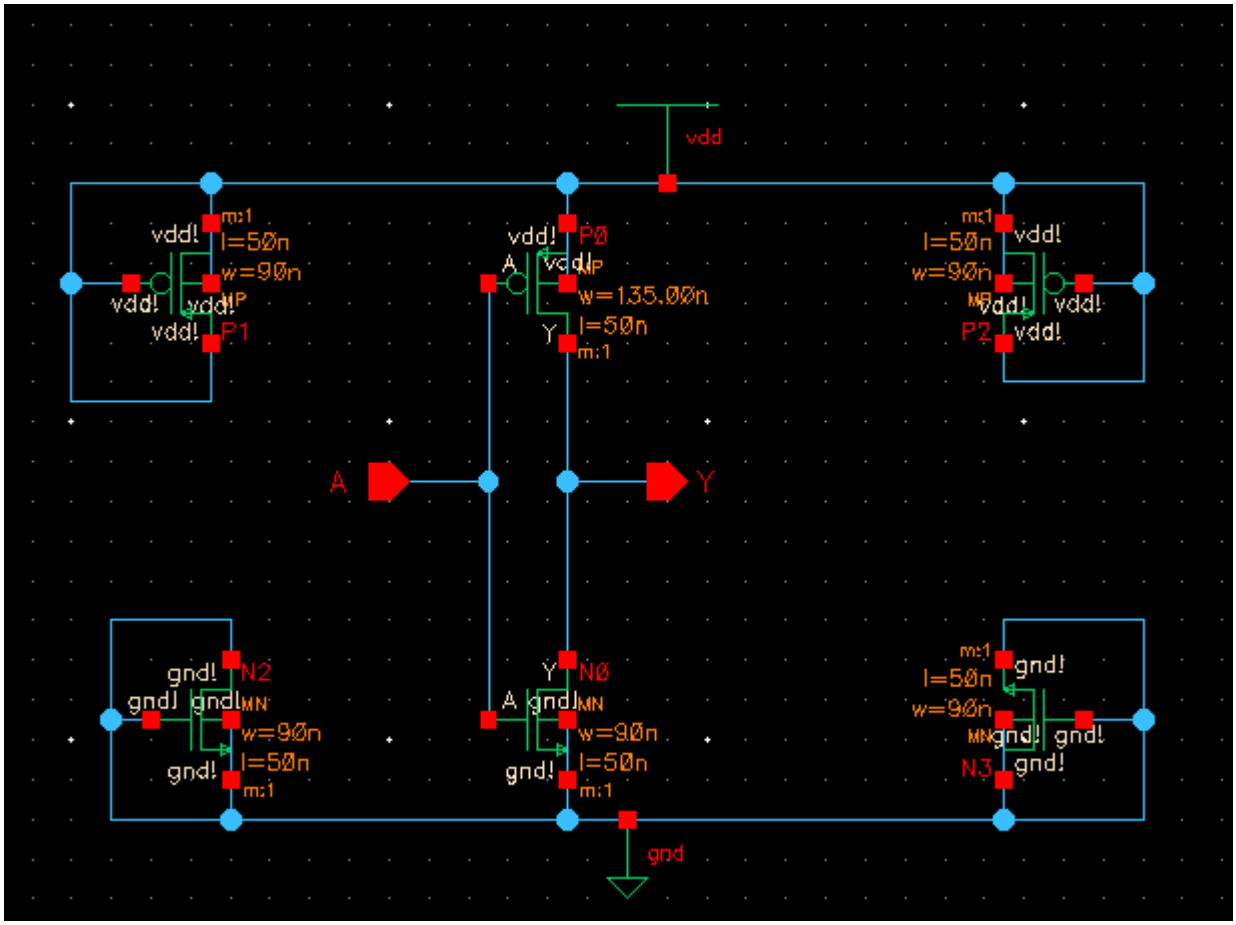


Figure 11: Schematic diagram of SOG Inverter

Transistor Dimensions

Save a color or black and white layout of the cell in EPS (i.e. Encapsulated Postscript) format. The cell dimensions are saved in both lambda (λ) and microns (μm). Record the transistor length and width dimensions (nm). [Repeat the transistor row as needed.]

Cell Physical Dimensions		
Y	X	
		Cell Dimension in λ
		Cell Dimension in μm
Transistor Dimensions		

Width (nm)	Length (nm)	UNIT Name
135	50	PMOS P0
90	50	PMOS P1, P2 NMOS N1, N2

Table 3: SOG Inverter Transistor Dimensions

Schematic diagrams of SOG Inverter :

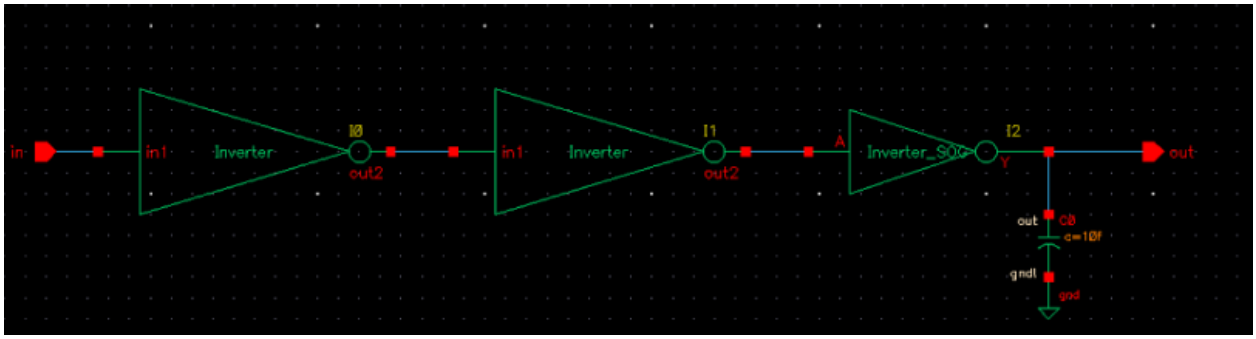


Figure 12: Schematic diagram of SOG Inverter with 0 fanout

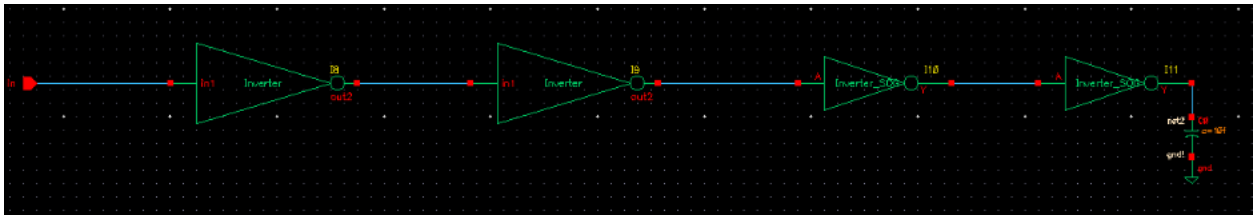


Figure 13: Schematic diagram of SOG Inverter with 1 fanout

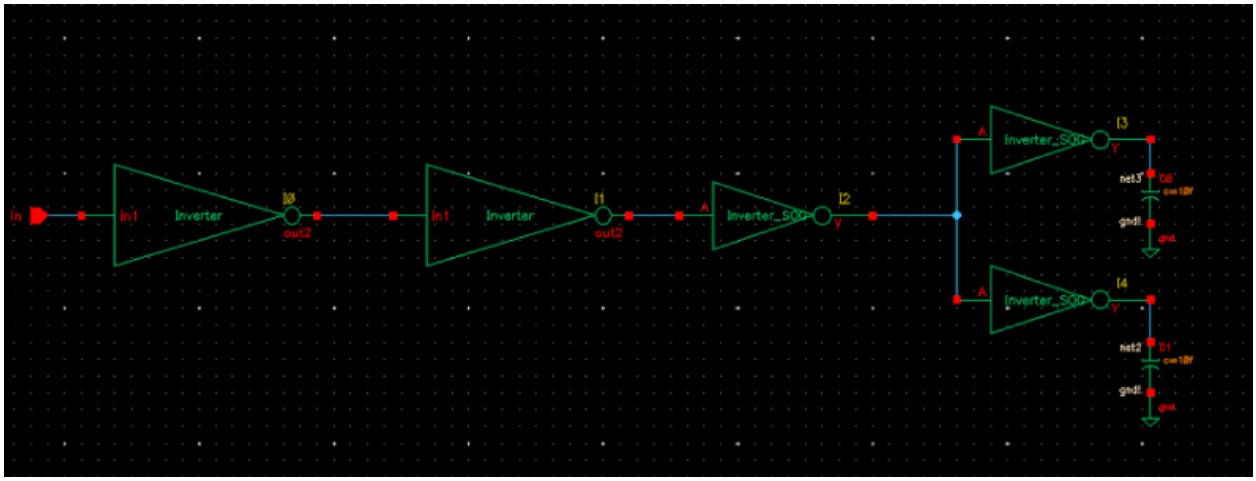


Figure 14: Schematic diagram of SOG Inverter with 2 fanouts

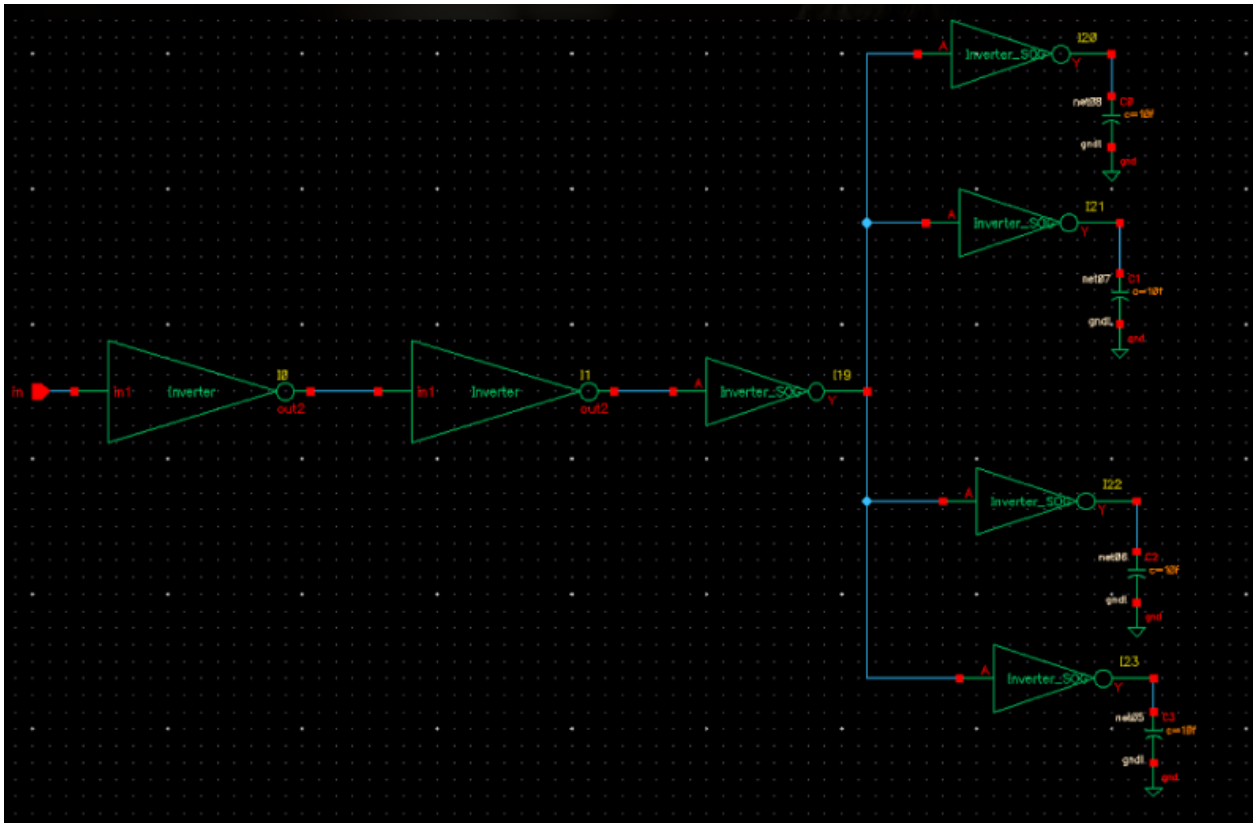


Figure 15: Schematic diagram of SOG Inverter with 4 fanouts

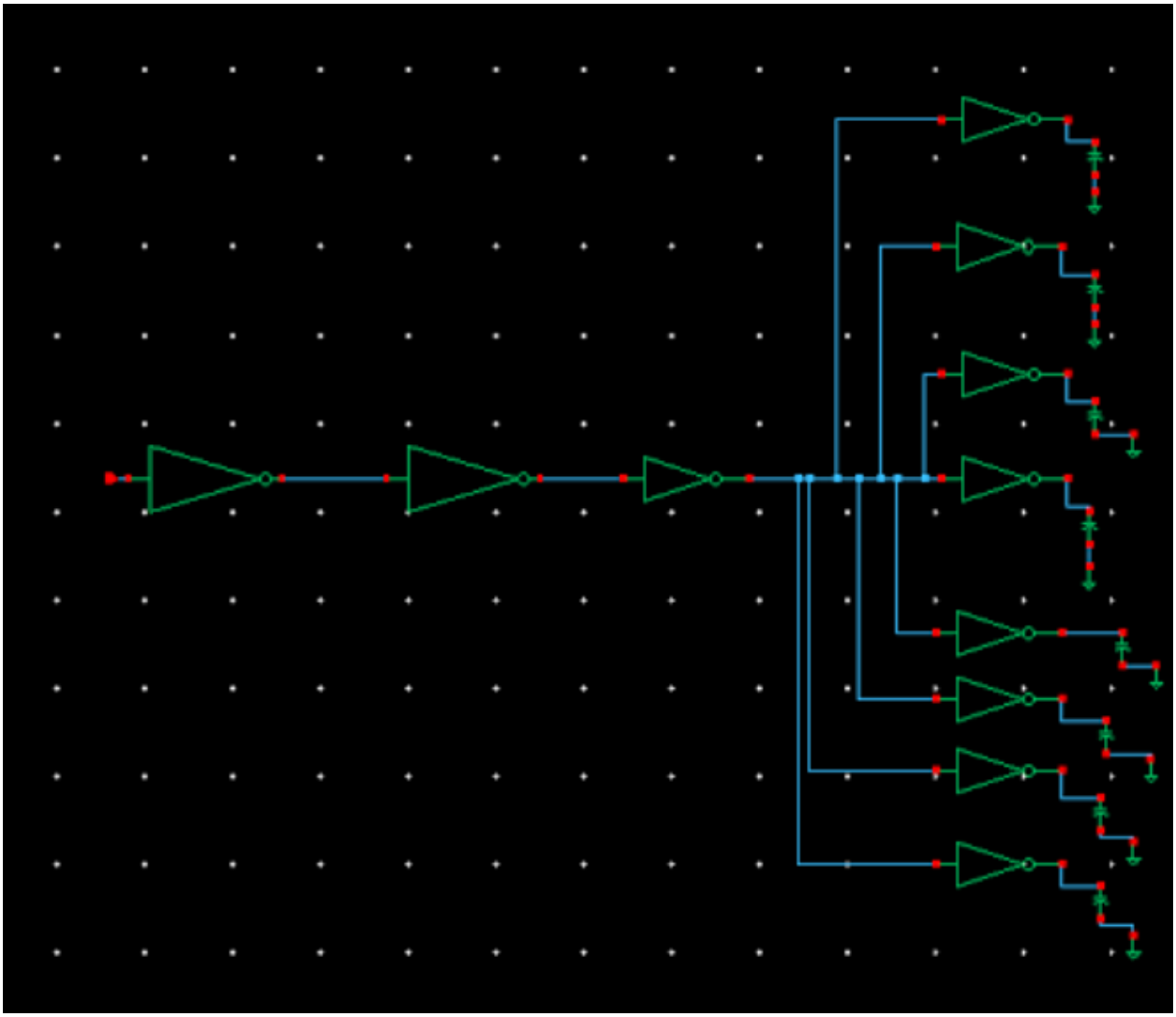


Figure 16: Schematic diagram of SOG Inverter with 8 fanouts

Input and Output Parasitic Capacitance Table

From the schematic calculate each input's capacitance normalized to the nominal inverter (your inverter standard cell) by the width of the transistor or drain area as needed. This entry should be an integer fraction similar to Weste and Harris. [Note the normalization is to a standard inverter (the standard cell inverter INV1X). Repeat the rows as needed.]

Computed Cell Input Capacitance	
Capacitance (/Cinv)	**Input Name**
Capacitance (/Cinv)	**Output Name**

Performance Analysis

Rise and Fall Times

[Note: It is highly desirable to split the simulation work load among the team members so that each team member learns how to use the tools.]

FOx denotes output loads. The loads are defined by the number of identical logic gates. Use 20%-80% swings for the output rise and fall entries. Use a 1.2V power supply.

For each output load in the table complete transient simulations. Remember to include a CMOS non-inverting buffer between the ideal voltage source and the logic gate driving the FOx load. Note rise t_r / fall t_f times are at the input to the logic gate driving the load, **not** the rise/fall times for the input ideal voltage source.

Complete the number needed copies (copies = No. input stacks x No. outputs) of the table below.

For multi-input gates, complete tables for each transistor stack (i.e. each branch connected to the output) using the stack's worst case single controlling input transition in the stack. Label the tables with worst case input in each stack and the output. Replace **X** below with the signal name.

Rise and Fall Times

SOG INVERTER

Input X: **Output Rise Time Data t_r** (ns)					
Output Load (FOx)					Input rise/fall time (ns)
0	1	2	4	8	
0.2175	0.0253	0.0307	0.0191	0.1074	0.04
					0.06

Stack S, Input X: **Output Fall Time Data t_f (ns)**					
Output Load (FOx)					Input rise/fall time (ns)
0	1	2	4	8	
0.1489	0.0236	0.036	0.033	0.0761	0.04
					0.06

Stack Input Combination: ***Replace with Boolean Product***

Propagation Delays

For the range of output loads shown in the table simulate propagation delays (low to high t_{plh} and high to low t_{phl}) for the stack's worst case single controlling input transition. The input controlling the output is the same input reported in

the rise and fall time section. Use a 1.2V power supply and timing measurements start when input to the logic gate driving the FOx load crosses the 50% of the rail and stop when the logic gate driving output crosses 50% of the rail. Negative values are entered as 0.

Label the tables with the Boolean product (e.g. AB) of the transistor stack and the output. Complete copies of the table below for each branch connected to the output.

Custom SOG:

Data Worst Case Low to High Propagation Delay Data t_{plh} (ns)					
Output Load (FOx)					Input rise/fall time (ns)
0	1	2	4	8	
0.1515	0.022	0.032	0.031	0.1404	0.04
					0.06

Data Worst Case High to Low Propagation Delay Data t_{phl} (ns)					
Output Load (FOx)					Input rise/fall time (ns)
0	1	2	4	8	
0.1179	0.0247	0.0284	0.0399	0.0609	0.04
					0.06

Custom Inverter:

Data Worst Case Low to High Propagation Delay Data t_{plh} (ns)					
Output Load (FOx)					Input rise/fall time (ns)
0	1	2	4	8	
0.0744	0.0461	0.032	0.0247	0.1515	0.04
					0.06

Data Worst Case High to Low Propagation Delay Data t_{phl} (ns)					
Output Load (FOx)					Input rise/fall time (ns)
0	1	2	4	8	
0.0609	0.0399	0.0284	0.022	0.1179	0.04
					0.06

Worse Case Input Combination: ***Replace with Boolean Product***

From each row of the slew rate data compute the best fit linear propagation delay equation for low-to-high T_{plh} (h) and high-to-low T_{phl} (h). The model predicts a delay, in nanoseconds, as a function of the output load, *h, Cout/Cin =FOx*. The model line is parameterized by a slope, *m*, and an intercept, *b*.
The units of *m* are (*ns/FOx*) and the units of *b* are *ns*.
Complete the table below by increasing the number of rows for multiple input gates. The row labeled **All data** is the computed slope and intercept after combining data from all slew rates.
Complete the **Model** row for the gate using the assumptions and methods of the linear delay model from Weste and Harris. Only skewed standard cells will

have different values propagation models for rising and falling inputs. All data means combine the results for both slew rates into a single model.

Discuss in your own words the differences in the calibration and the Weste Harris linear delay model. Discuss the differences in high-to-low versus lowto-high models.

Data Model Propagation Delay Equation $T_{pd}(h) = b + m \cdot h$				
Parasitic Falling Delay (b_r)	Parasitic Rising Delay (b_r)	Falling Logical Effort (m_f)	Rising Logical Effort (m_r)	Input Slew Rate (ns)
				0.04
				0.06
				All data

In the table below normalize the model for the T_{pd} (h) results of the table above to give the logical effort model *D(h)* described in Weste and Harris. *D(h)* is a unitless value and predicts the delay as multiples of the standard inverter delay. Normalization is based on the observed CMOS inverter parasitic delay, b_{inv}. *Recall* ***all data*** $p_{inv} \equiv 1$.

Inverter Normalized Data Model Propagation Delay Equation $D(h) = p + g \cdot h$				
Parasitic Falling Delay (p_r)	Parasitic Rising Delay (p_r)	Falling Logical Effort (g_f)	Rising Logical Effort (g_r)	Input Slew Rate (ns)
				0.04
				0.06
				All data
				W&H Model

Power-Delay

Simulate the cell for a sequence of input combinations based on the Gray code and compute the time averaged power (mW), average delay (ns), and average power-delay product (mW ns = pJ). The Gray code restricts the simulations to single input transitions and ignores the large number of multiple input change combinations. Use the same slew rate for all input transitions. Use equal output loads for multiple output gates. Use a period of 2X maximum output delay with FO=8.

INVERTER_CUSTOM

Average Power Data (u W)					
Output Load (FOx)					Input Slew (ns)
8	4	2	1	0	
	12.75				0.04
					0.06

Table 1.13 Average power data for full custom

Average Delay Data (n s)					
Output Load (FOx)					Input Slew (ns)
8	4	2	1	0	
	0.1536				0.04
					0.06

Table 1.14 Average delay data for full custom

Average Power-Delay Data (pJ)					
Output Load (FOx)					Input Slew (ns)
8	4	2	1	0	
	$1.9584e^{-3}$				0.04

					0.06

Table 1.15 Average power- delay data for full custom

INVERTER_SOG

Average Power Data (u W)					
Output Load (FOx)					Input Slew (ns)
8	4	2	1	0	
	18.09				0.04
					0.06

Table 1.16 Average power data for sea of gates

Average Delay Data (n s)					
Output Load (FOx)					Input Slew (ns)
8	4	2	1	0	
	0.043				0.04
					0.06

Table 1.17 Average delay data for sea of gates

Average Power-Delay Data (pJ)					
Output Load (FOx)					Input Slew (ns)
8	4	2	1	0	
	0.778 e $^{-3}$				0.04
					0.06

Table 1.18 Average power- delay data for sea of gates

Waveforms for CUSTOM INVERTER

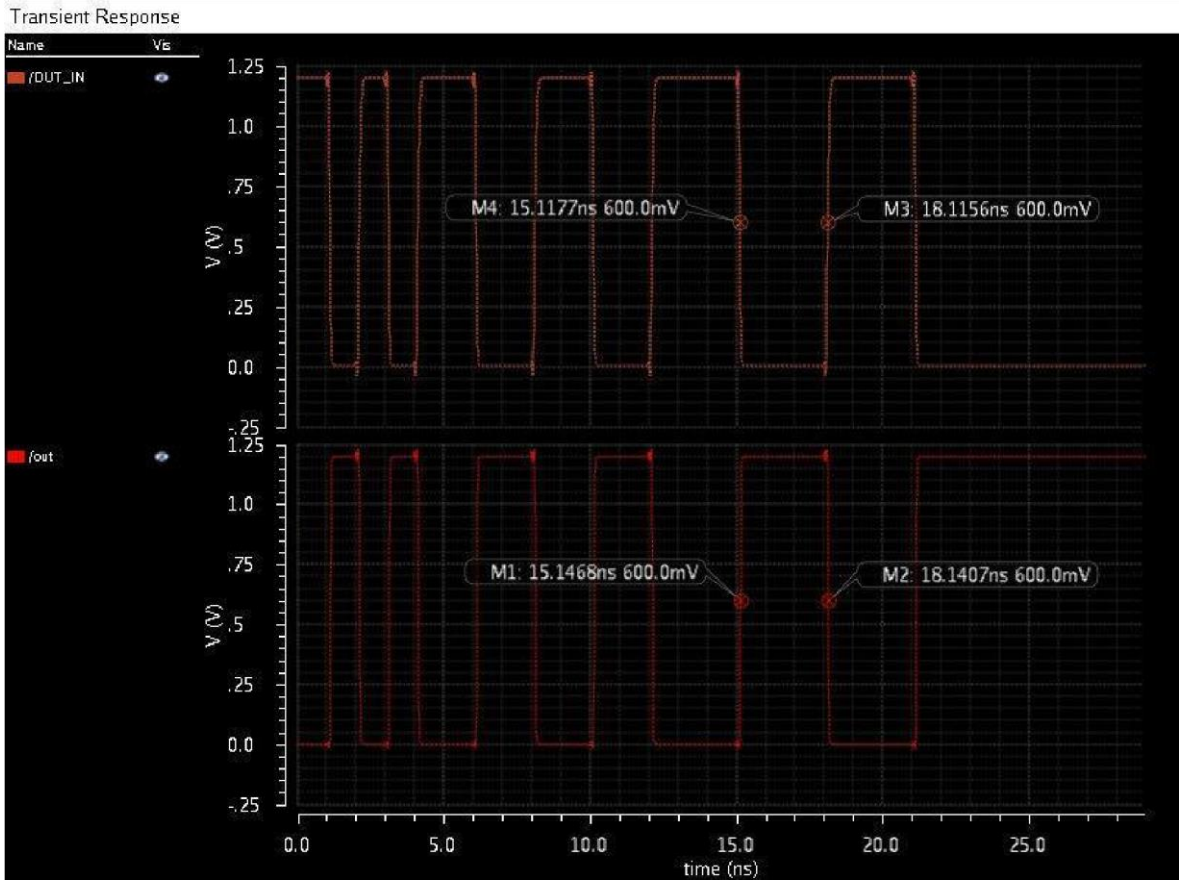


Figure 17: Waveform of Custom Inverter with 0 fanout

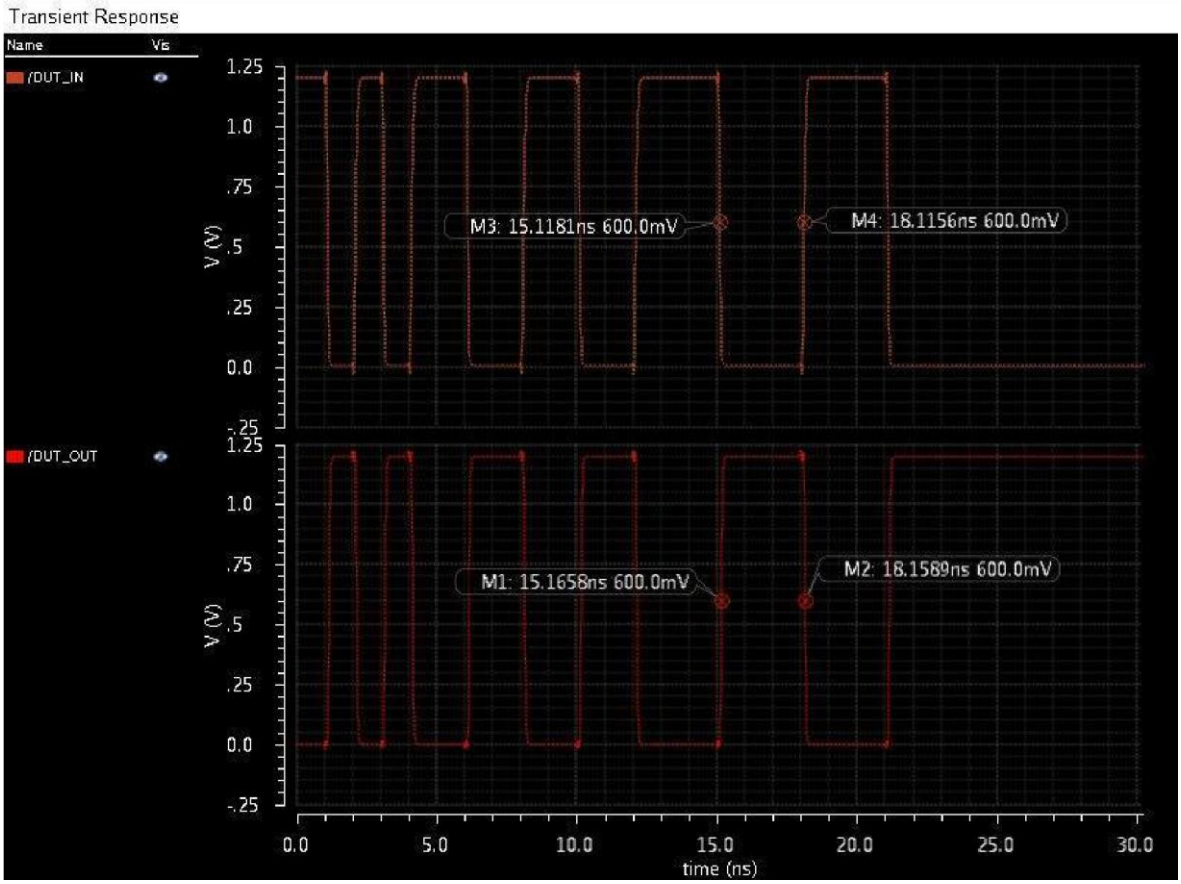


Figure 18 : Waveform of Custom Inverter with 1 fanout

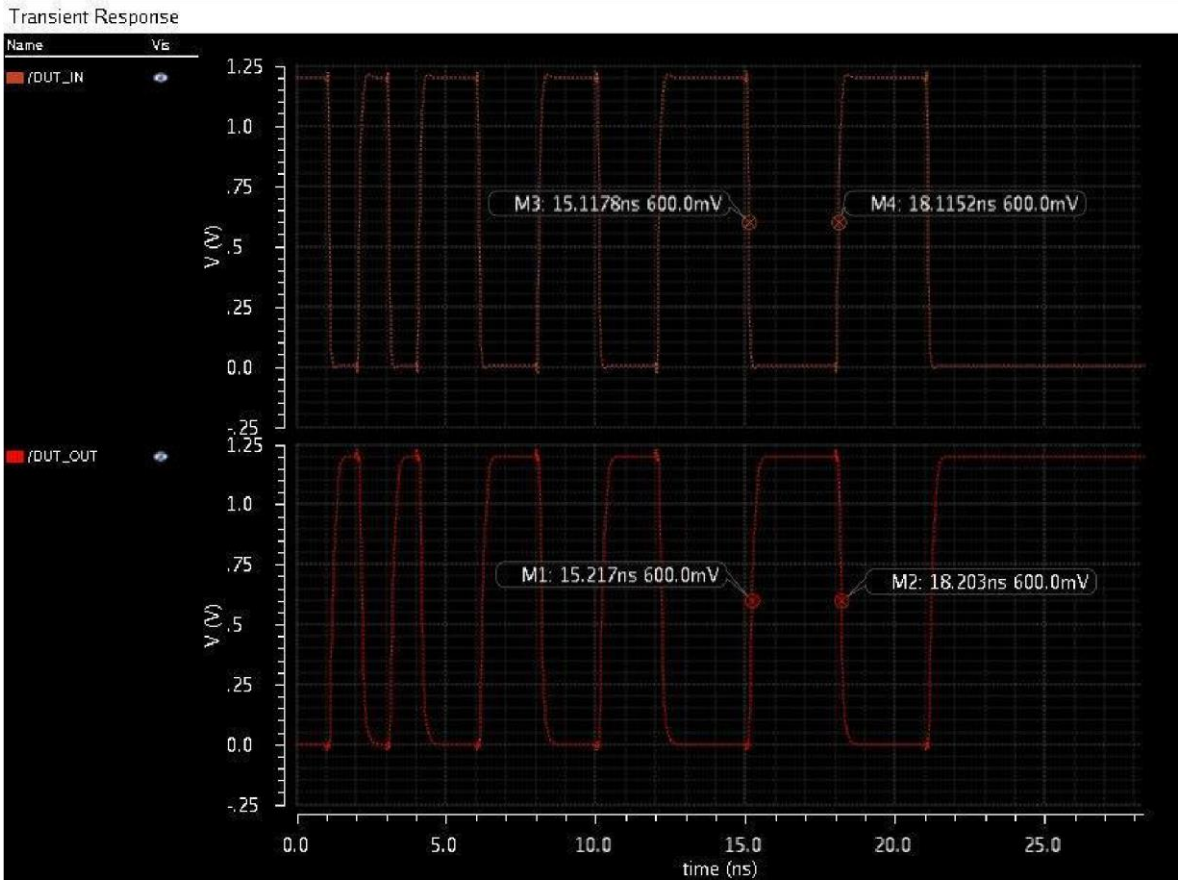


Figure 19: Waveform of Custom Inverter with 2 fanouts

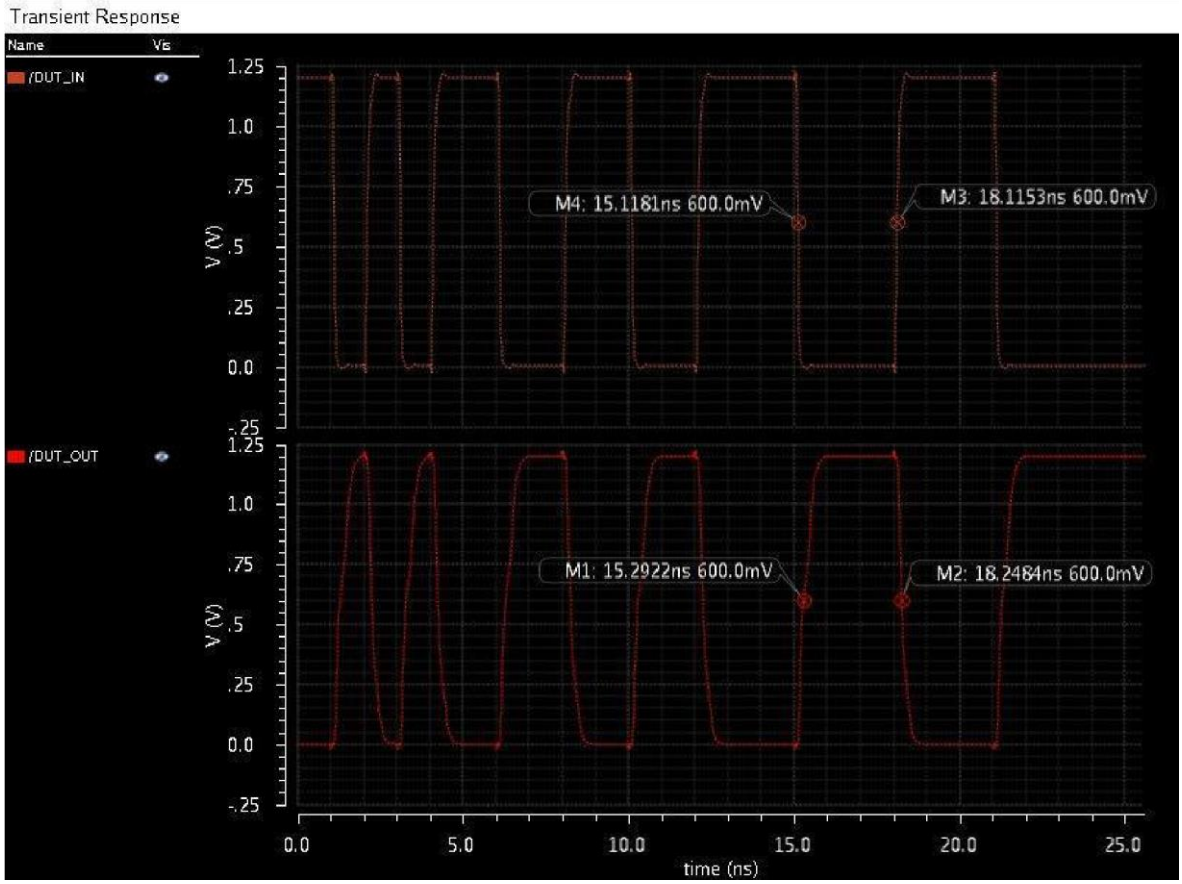
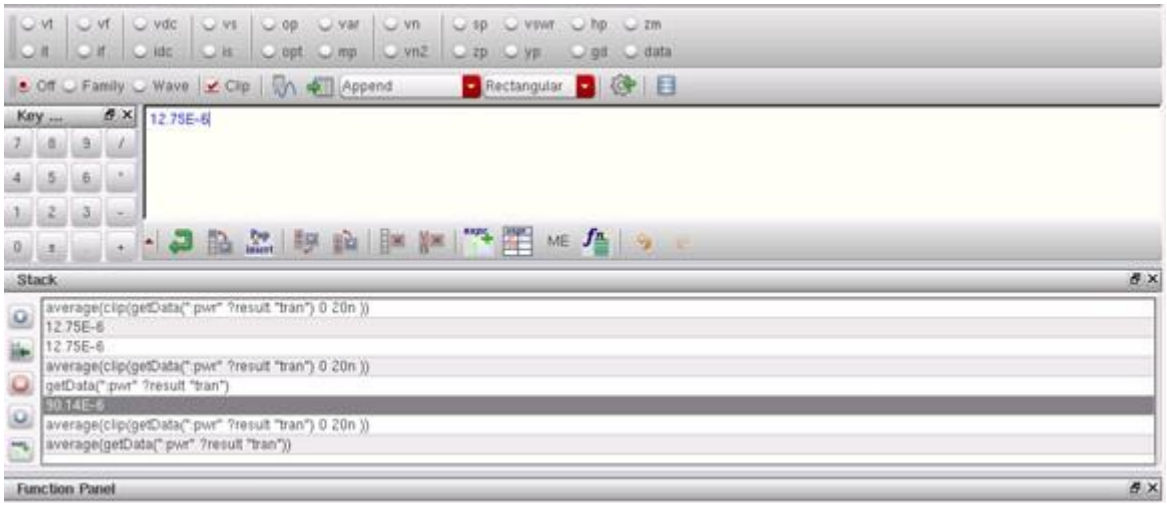


Figure 20: Waveform of Custom Inverter with 4 fanouts



Power Calculation for Custom Inverter with 4 fanouts

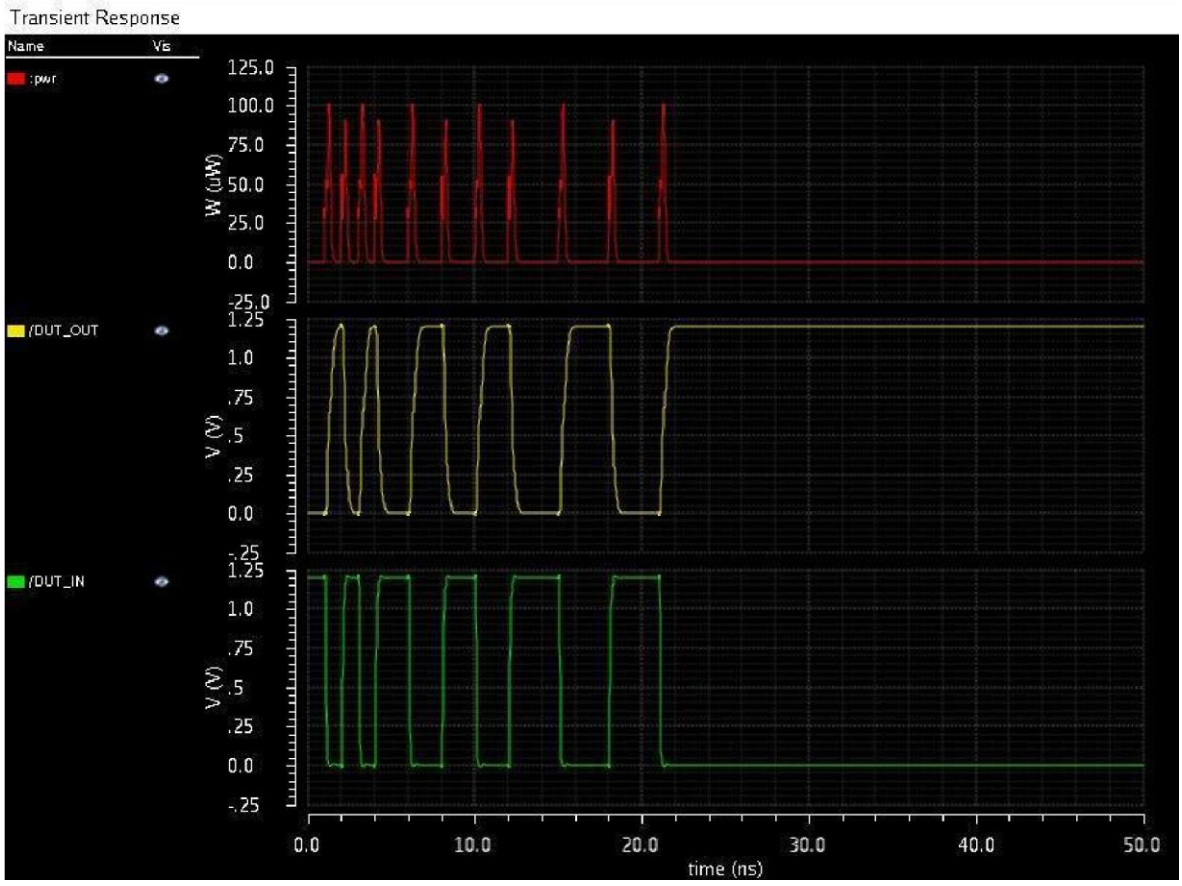


Figure 21 : Waveform of Custom Inverter displaying power with 4 fanouts

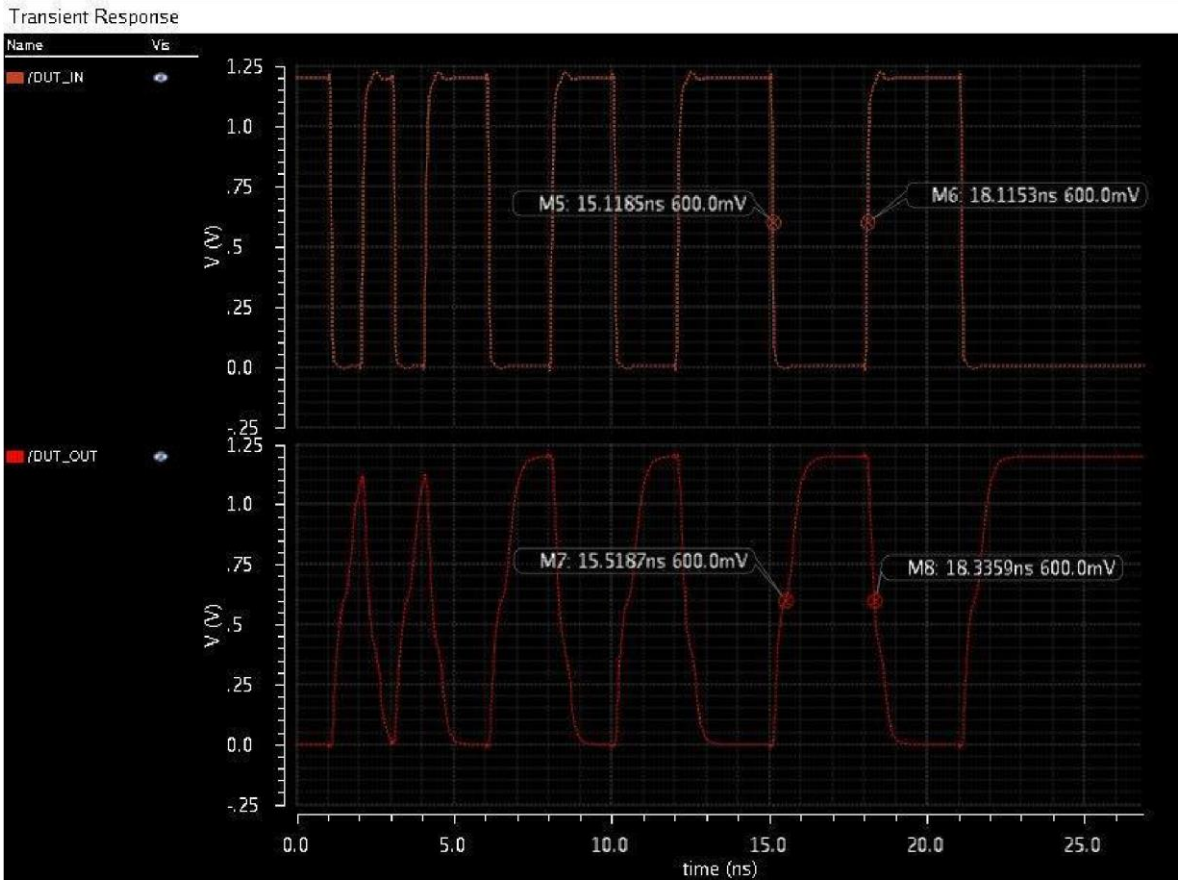


Figure 22 : Waveform of Custom Inverter with 8 fanouts

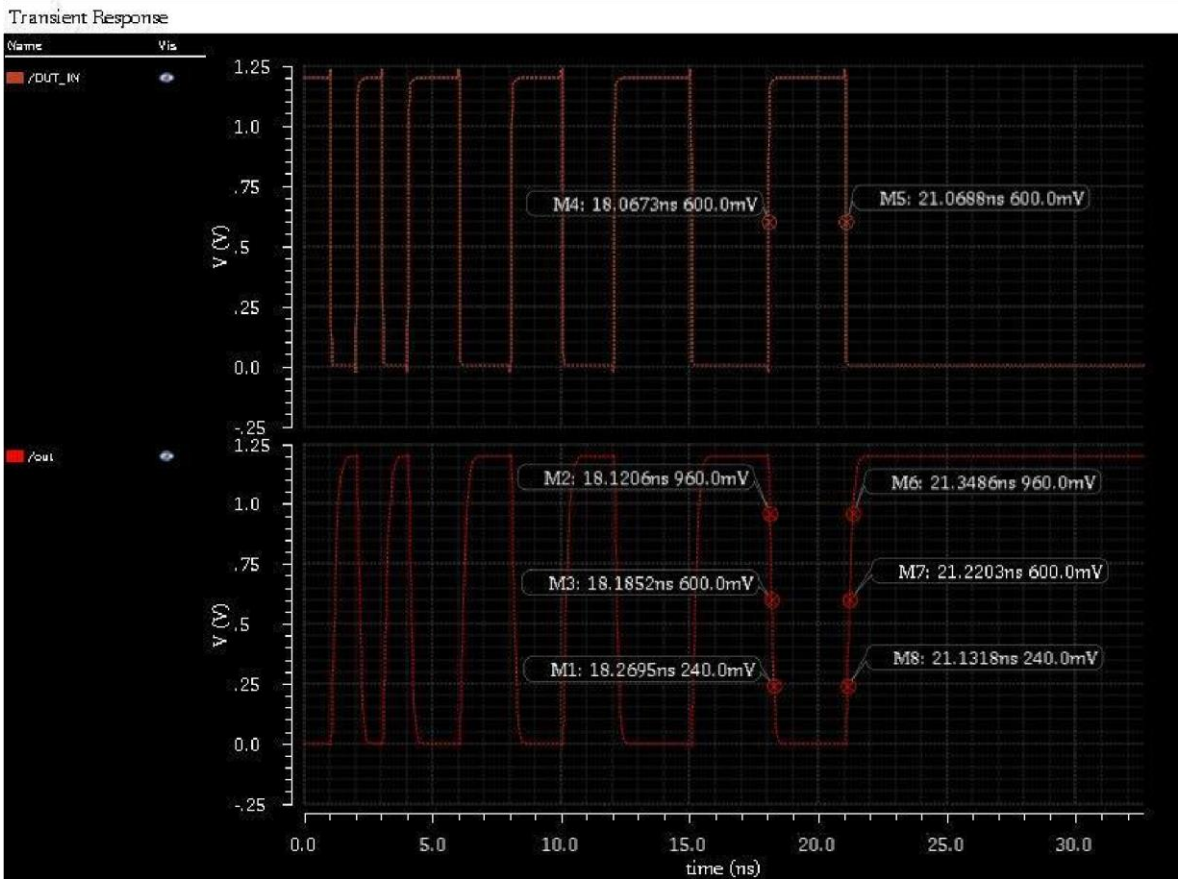


Figure 23 : Waveform of SOG Inverter with 0 fanout

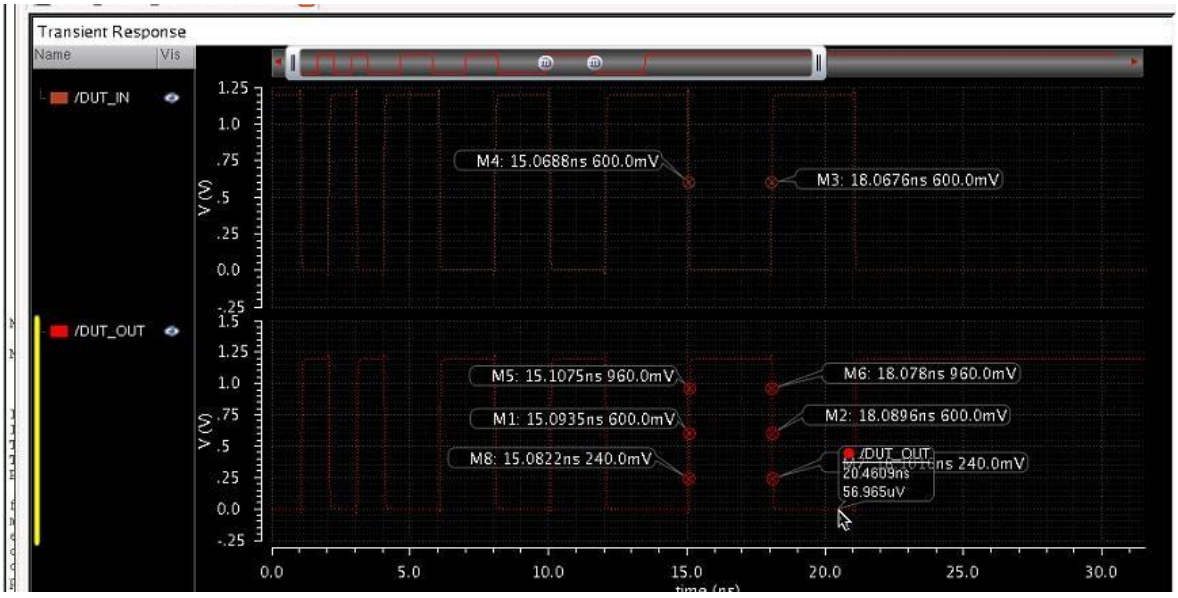


Figure 24 : Waveform of SOG Inverter with 1 fanout

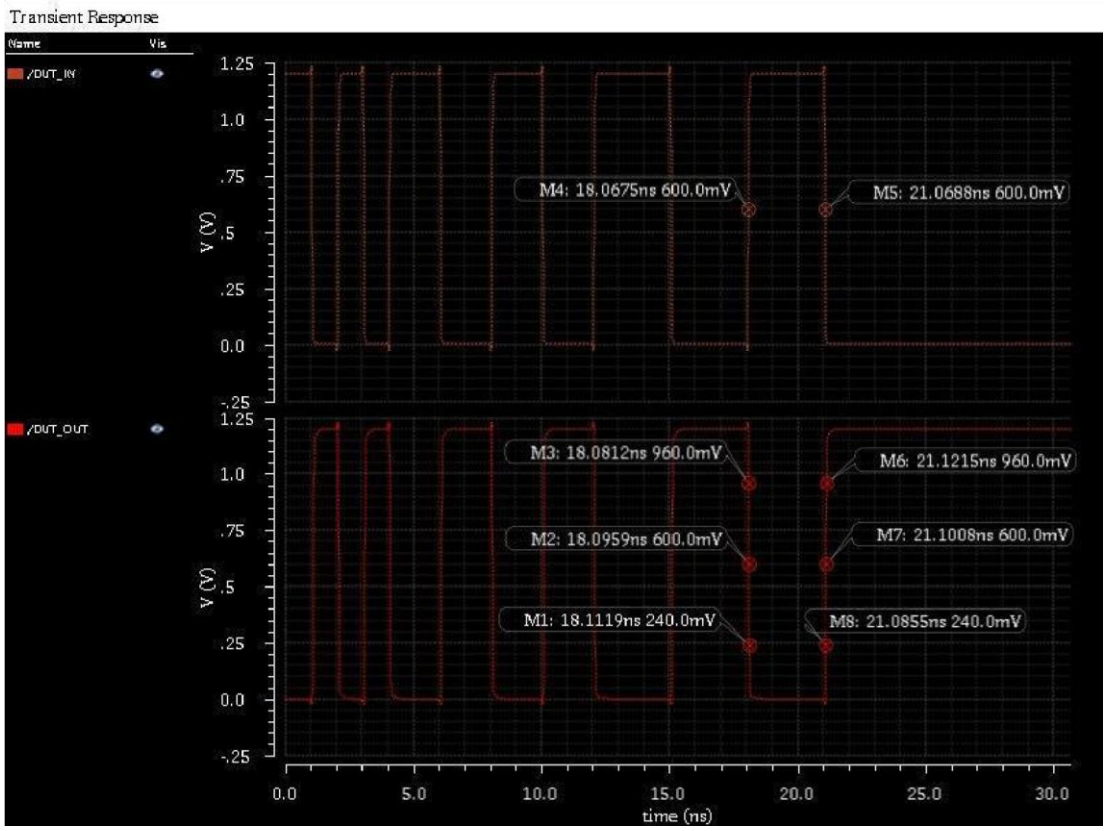


Figure 25: Waveform of SOG Inverter with 2 fanouts

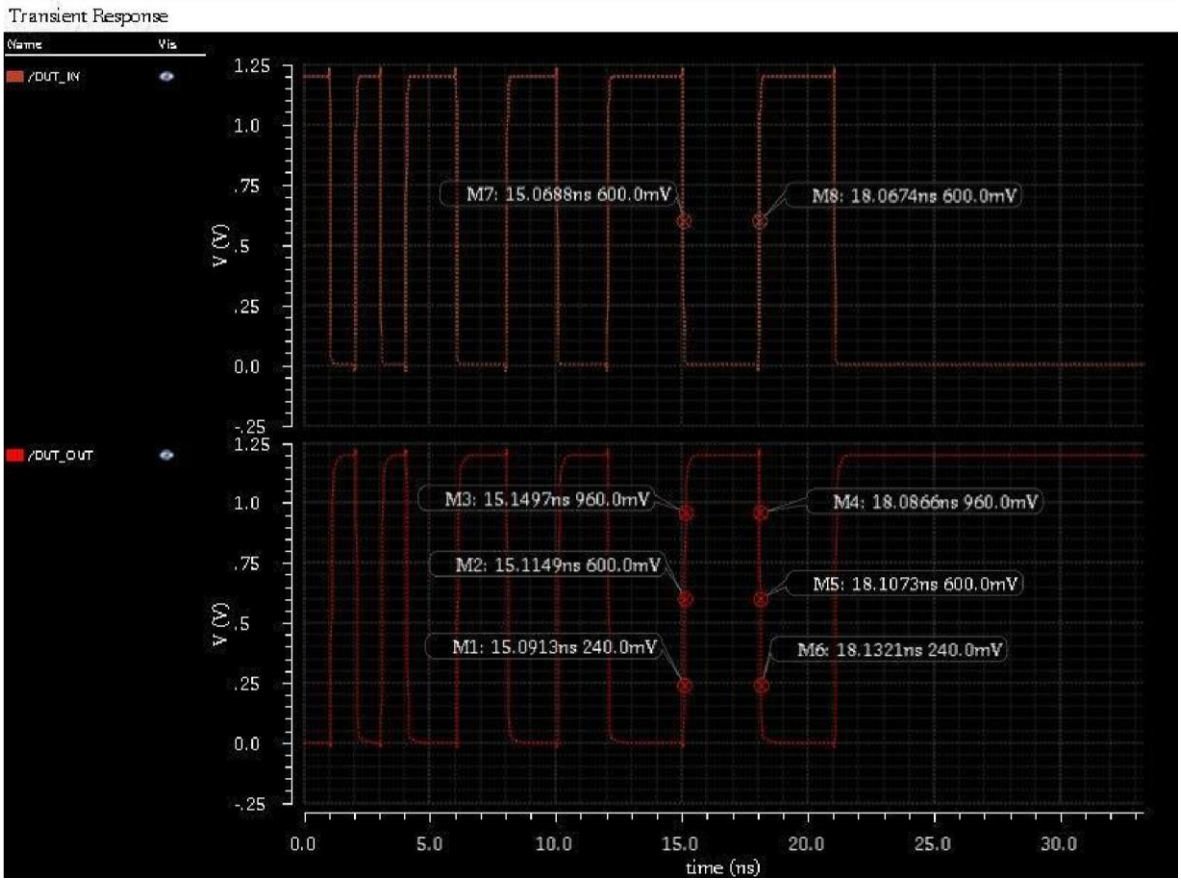


Figure 26: Waveform of SOG Inverter with 4 fanouts

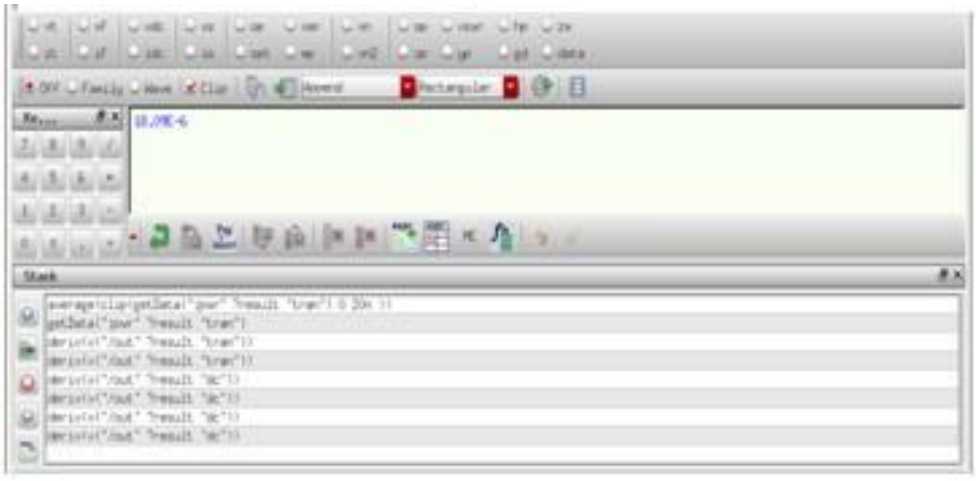


Figure 27: Power calculation for F04 Inverter SOG

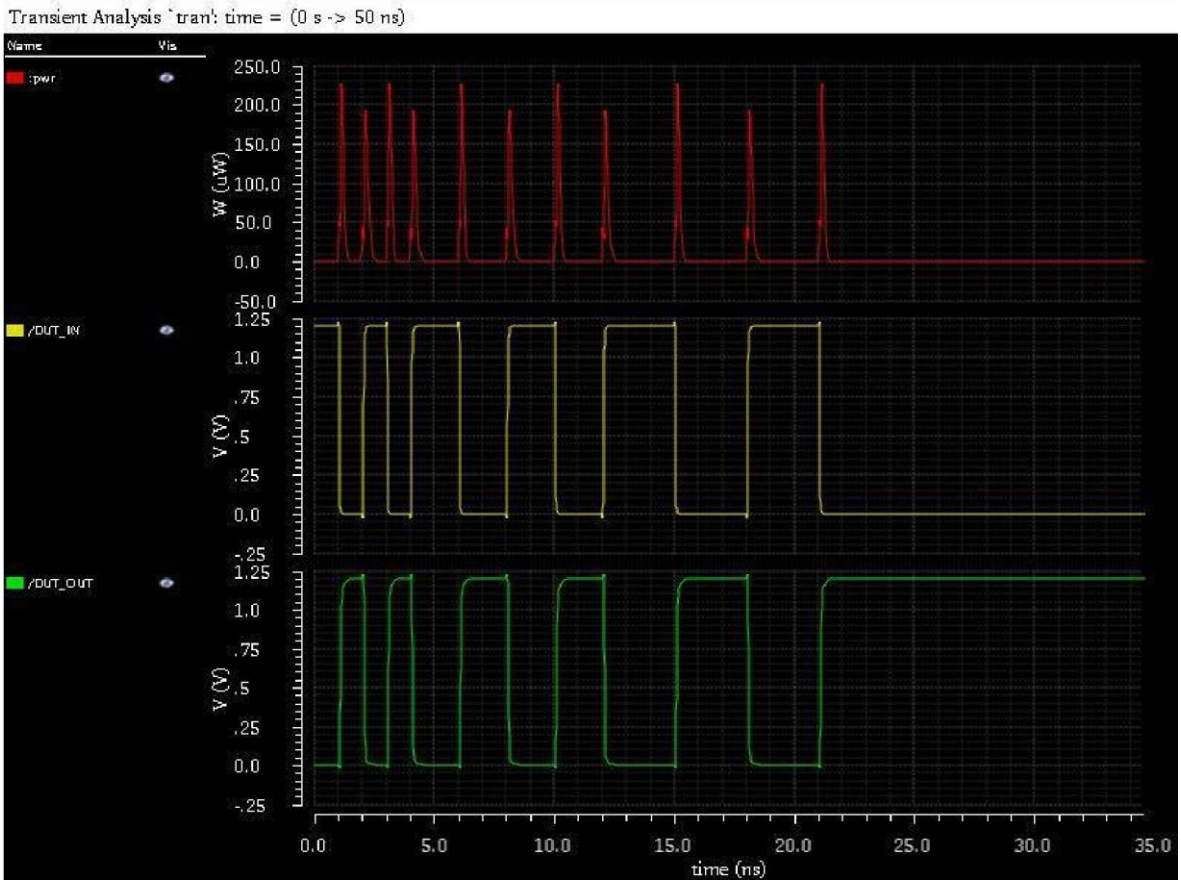


Figure 27 : Waveform of SOG Inverter displaying power with 4 fanouts

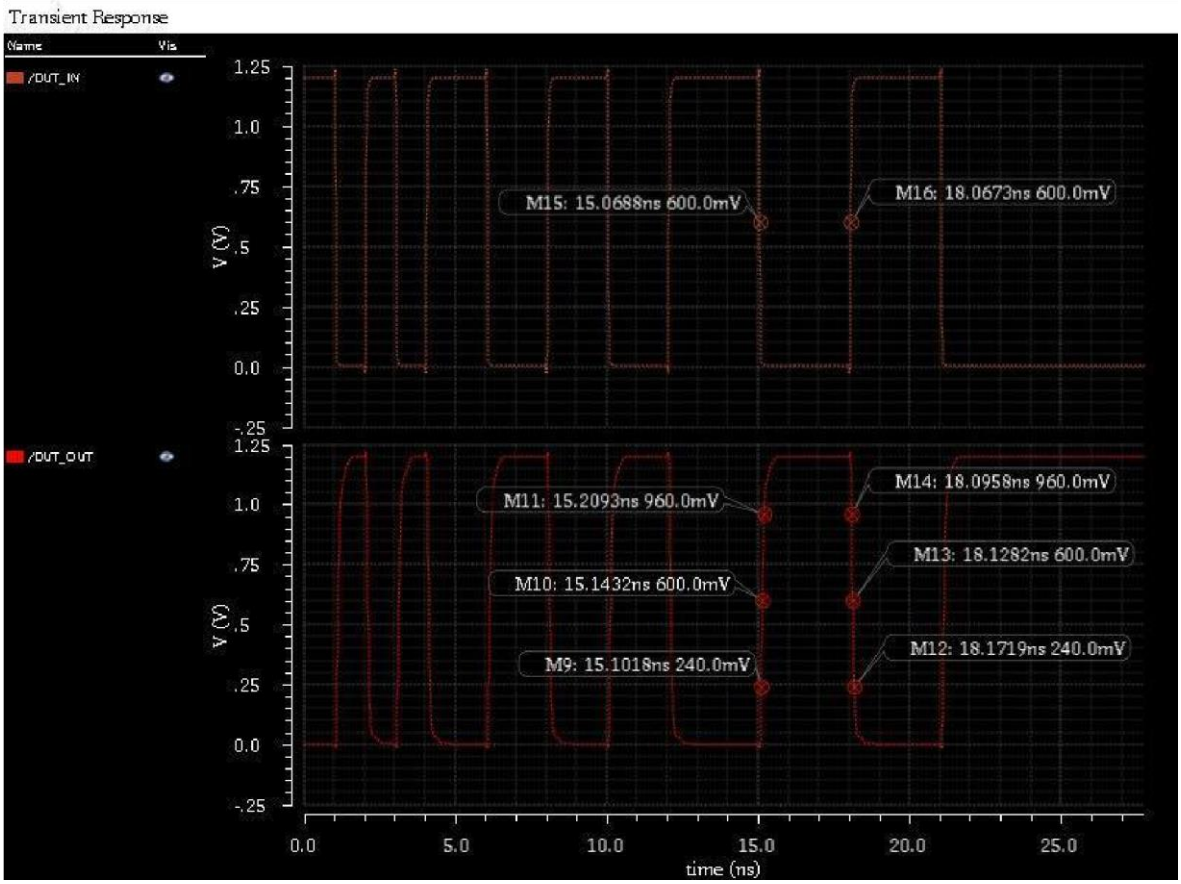


Figure 28 : Waveform of SOG Inverter with 8 fanouts

LAYOUTS OF CUSTOM AND SOG INVERTERS

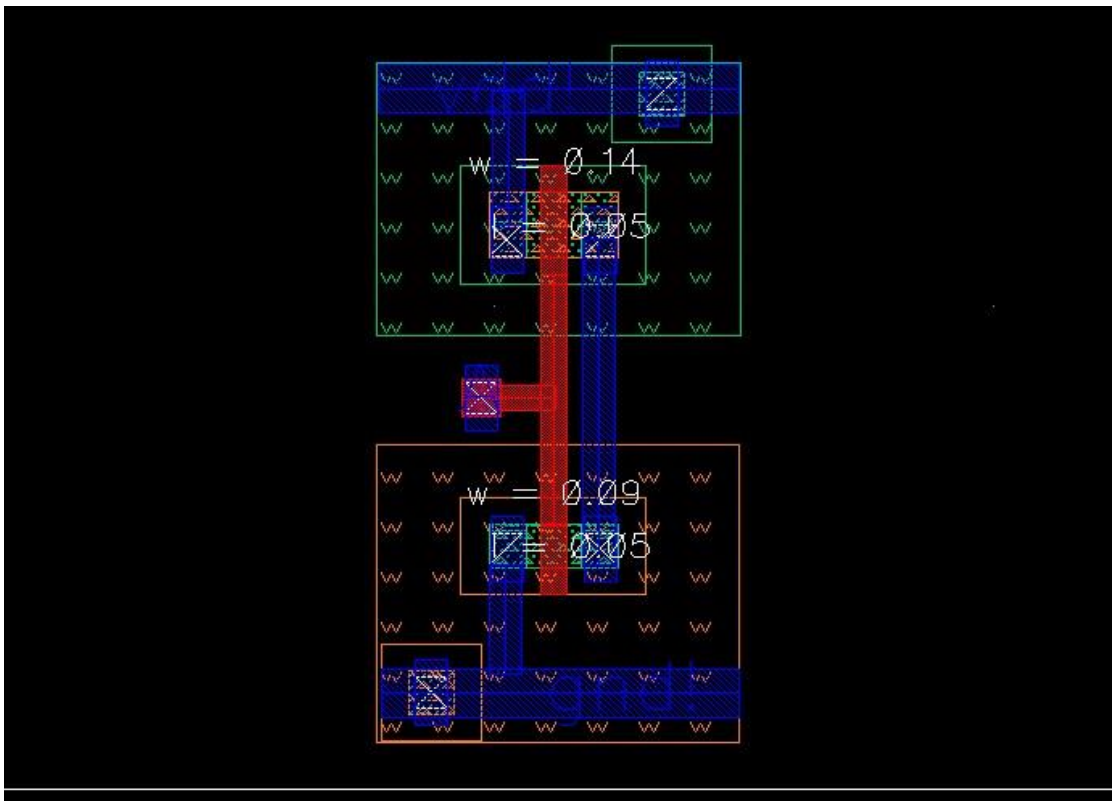


Figure 29: Layout of DUT Inverter

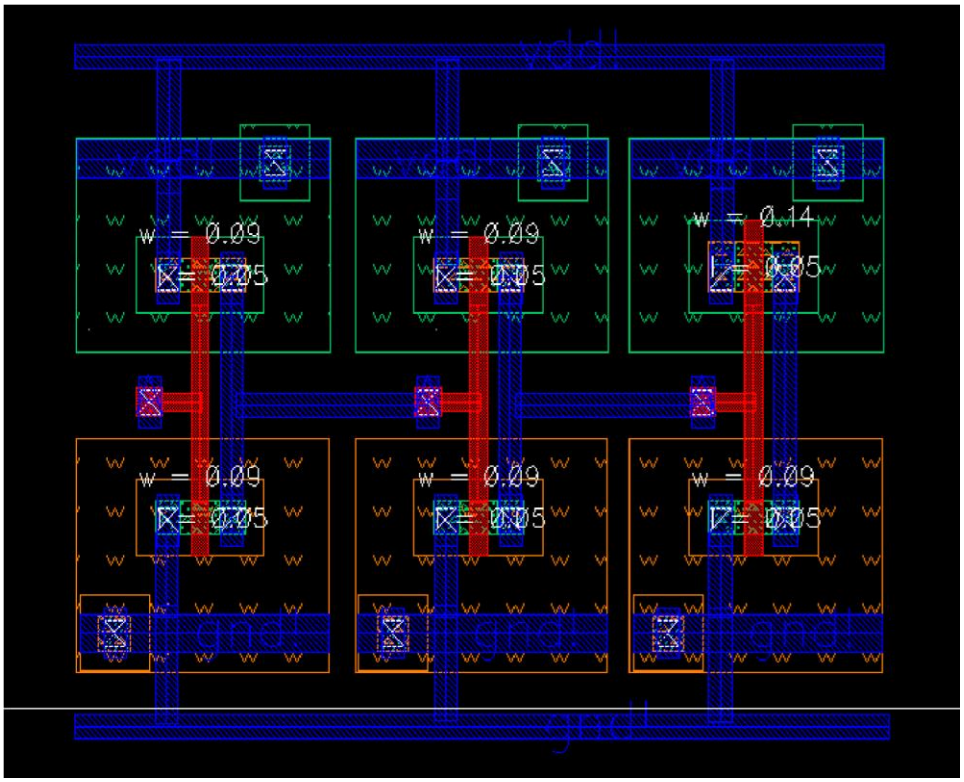


Figure 30: Layout of Custom Inverter with 0 fanout

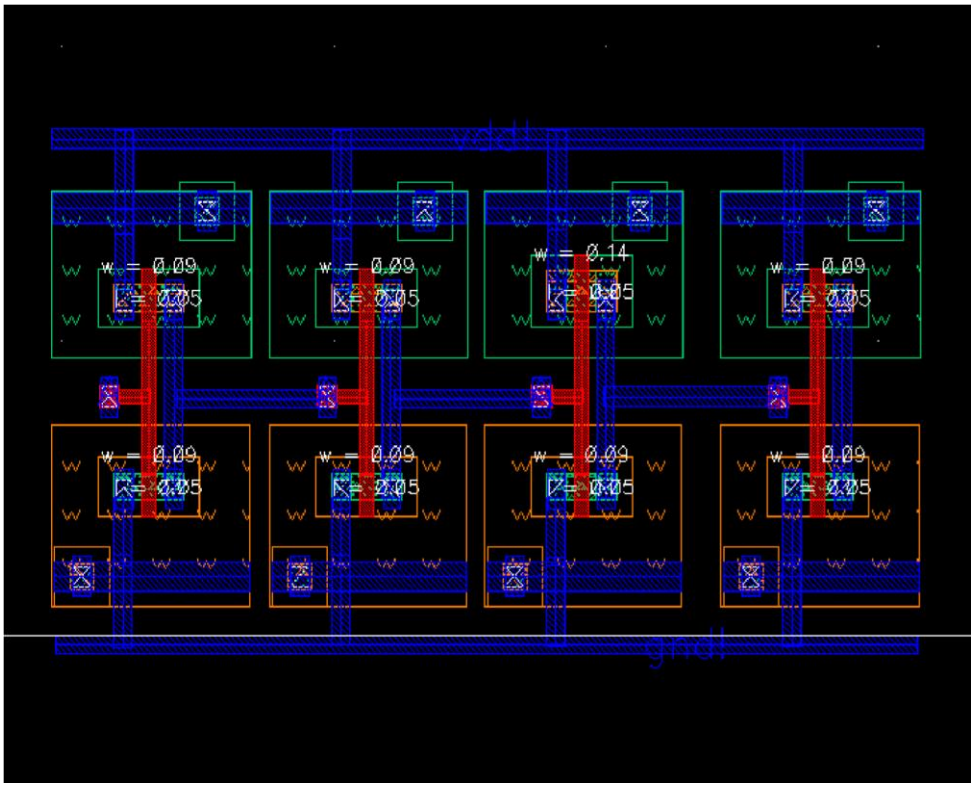


Figure 31: Layout of Custom Inverter with 1 fanout

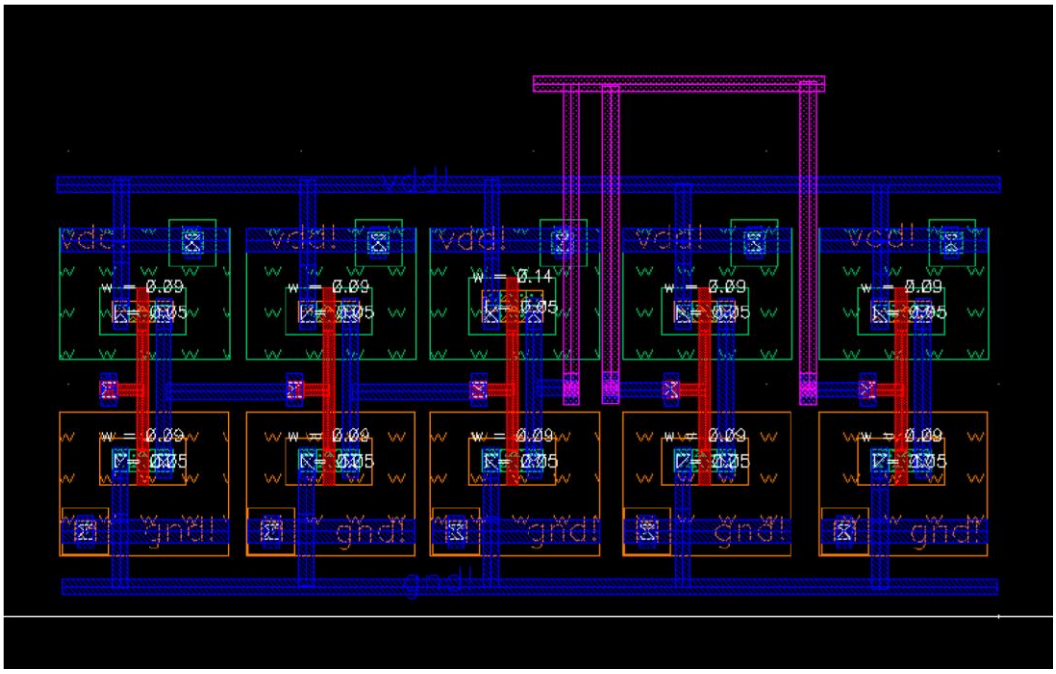


Figure 32: Layout of Custom Inverter with 2 fanouts

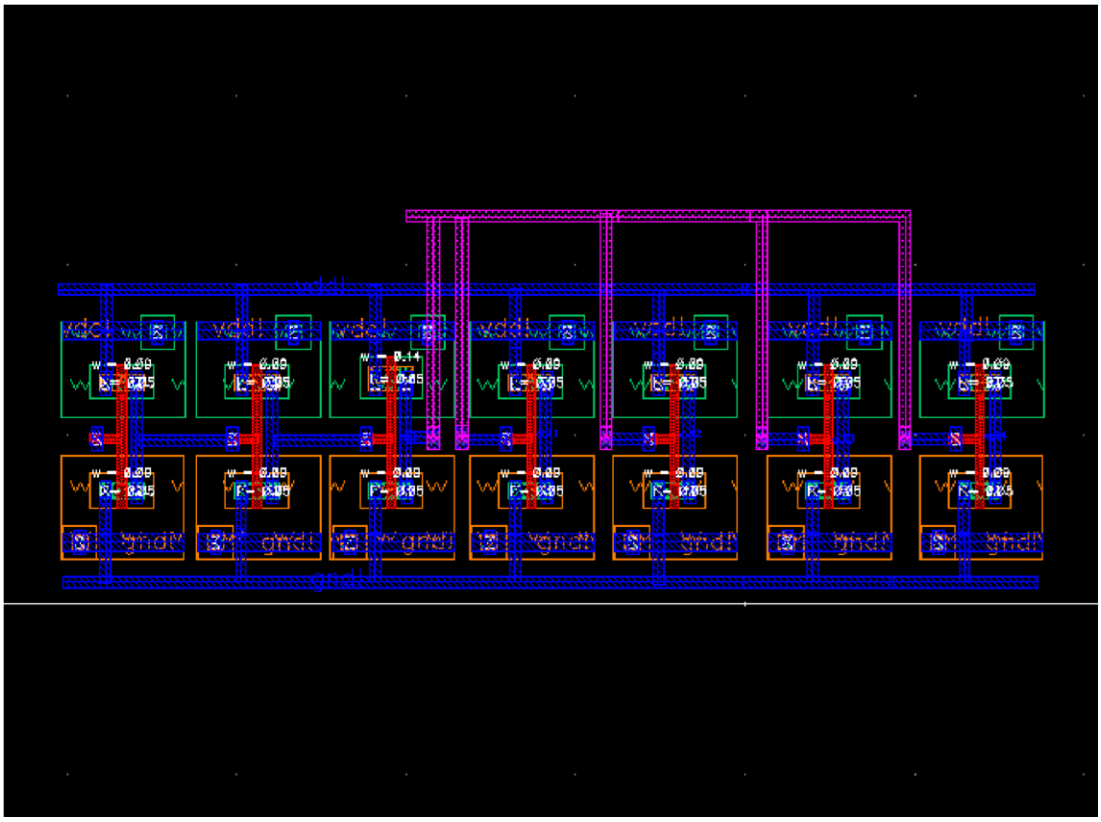


Figure 33: Layout of Custom Inverter with 4 fanouts

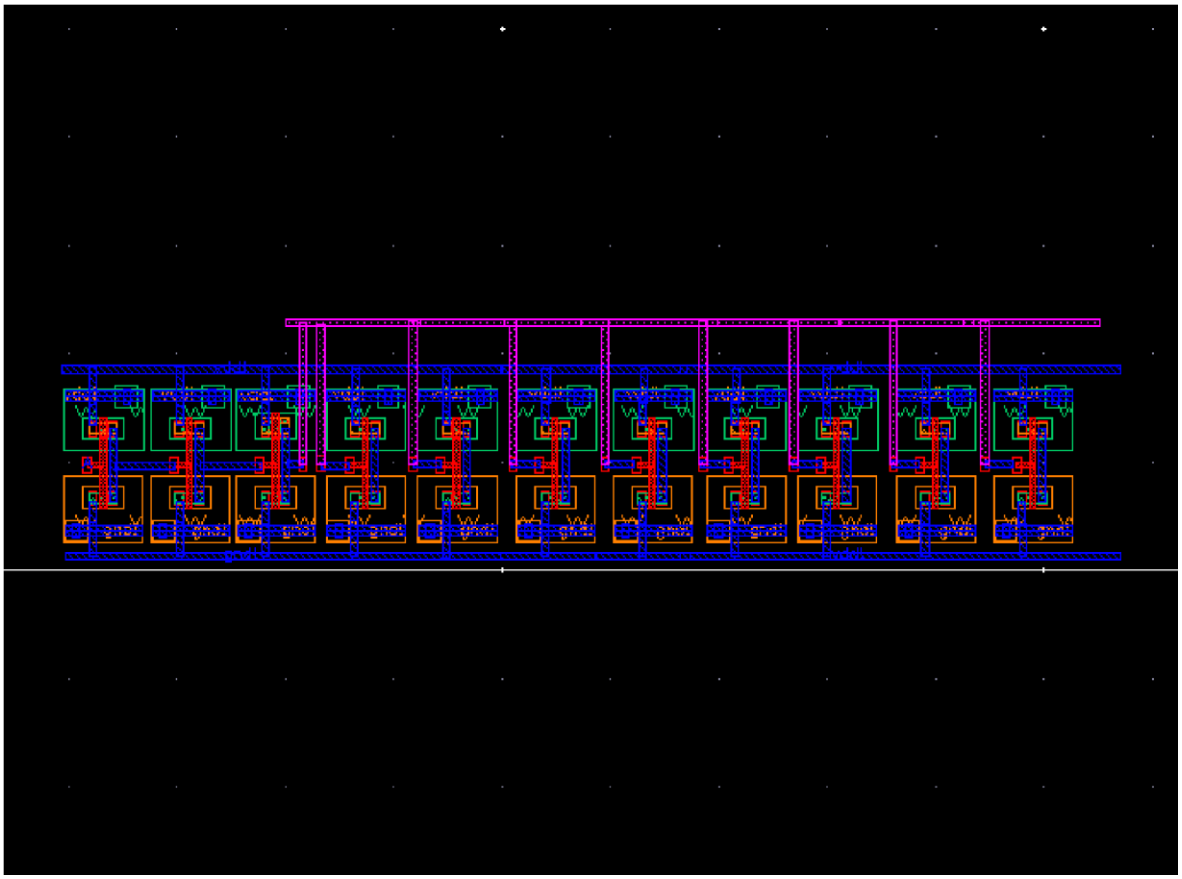


Figure 34: Layout of Custom Inverter with 8 fanouts

DRC and LVS Reports:

DRC FO0:

```
================================================================================
==========
=== CALIBRE::DRC-F SUMMARY REPORT
===
Execution Date/Time:        Mon Mar 13 03:45:53 2017
Calibre Version:            v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013
Rule File Pathname:         /u/soma2/cadence/DRC-files/_calibreDRC.rul_
Rule File Title:
Layout System:              GDS
Layout Path(s):             inverter_fa0_new2.calibre.db
Layout Primary Cell:        inverter_fa0_new2
Current Directory:          /u/soma2/cadence/DRC-files
User Name:                  soma2
Maximum Results/RuleCheck: 1000
```

```
Maximum Result Vertices:   4096
DRC Results Database:      inverter_fa0_new2.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       inverter_fa0_new2.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID =
NO
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:         COMMENT TEXT + RULE FILE INFORMATION
Layers:                    MEMORY-BASED
Keep Empty Checks:         YES
----------------------------------------------------------------------
----------
--- RUNTIME WARNINGS
---
----------------------------------------------------------------------
----------
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ...... TOTAL Original Geometry Count = 5
LAYER nwell ...... TOTAL Original Geometry Count = 5
LAYER active ..... TOTAL Original Geometry Count = 44
LAYER poly ....... TOTAL Original Geometry Count = 27
LAYER pimplant ... TOTAL Original Geometry Count = 4
LAYER nimplant ... TOTAL Original Geometry Count = 4
LAYER vth ........ TOTAL Original Geometry Count = 0
LAYER vtg ........ TOTAL Original Geometry Count = 0
LAYER metal1 ..... TOTAL Original Geometry Count = 31
LAYER metal2 ..... TOTAL Original Geometry Count = 0
LAYER metal3 ..... TOTAL Original Geometry Count = 0
LAYER metal4 ..... TOTAL Original Geometry Count = 0
LAYER metal5 ..... TOTAL Original Geometry Count = 0
LAYER metal6 ..... TOTAL Original Geometry Count = 0
LAYER metal7 ..... TOTAL Original Geometry Count = 0
LAYER metal8 ..... TOTAL Original Geometry Count = 0
LAYER metal9 ..... TOTAL Original Geometry Count = 0
LAYER metal10 .... TOTAL Original Geometry Count = 0
LAYER contact .... TOTAL Original Geometry Count = 17
LAYER via1 ....... TOTAL Original Geometry Count = 0
LAYER via2 ....... TOTAL Original Geometry Count = 0
LAYER via3 ....... TOTAL Original Geometry Count = 0
LAYER via4 ....... TOTAL Original Geometry Count = 0
LAYER via5 ....... TOTAL Original Geometry Count = 0
LAYER via6 ....... TOTAL Original Geometry Count = 0
LAYER via7 ....... TOTAL Original Geometry Count = 0
LAYER via8 ....... TOTAL Original Geometry Count = 0
LAYER via9 ....... TOTAL Original Geometry Count = 0
```

```
--------------------------------------------------------------------------
----------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK Well.1 ..... TOTAL Result Count = 0
RULECHECK Well.2 ..... TOTAL Result Count = 0
RULECHECK Well.4 ..... TOTAL Result Count = 0
RULECHECK Poly.1 ..... TOTAL Result Count = 0
RULECHECK Poly.2 ..... TOTAL Result Count = 0
RULECHECK Poly.3 ..... TOTAL Result Count = 0
RULECHECK Poly.4 ..... TOTAL Result Count = 0
RULECHECK Poly.5 ..... TOTAL Result Count = 0
RULECHECK Poly.6 ..... TOTAL Result Count = 0
RULECHECK Active.1 .... TOTAL Result Count = 0
RULECHECK Active.2 .... TOTAL Result Count = 0
RULECHECK Active.3 .... TOTAL Result Count = 0
RULECHECK Active.4 .... TOTAL Result Count = 0
RULECHECK Implant.1 ... TOTAL Result Count = 0
RULECHECK Implant.2 ... TOTAL Result Count = 0
RULECHECK Implant.3 ... TOTAL Result Count = 0
RULECHECK Implant.4 ... TOTAL Result Count = 0
RULECHECK Implant.6 ... TOTAL Result Count = 0
RULECHECK Contact.1 ... TOTAL Result Count = 0
RULECHECK Contact.2 ... TOTAL Result Count = 0
RULECHECK Contact.3 ... TOTAL Result Count = 0
RULECHECK Contact.4 ... TOTAL Result Count = 0
RULECHECK Contact.5 ... TOTAL Result Count = 0
RULECHECK Contact.6 ... TOTAL Result Count = 0
RULECHECK Metal1.1 .... TOTAL Result Count = 0
RULECHECK Metal1.2 .... TOTAL Result Count = 0
RULECHECK Metal1.3 .... TOTAL Result Count = 0
RULECHECK Metal1.4 .... TOTAL Result Count = 0
RULECHECK Via1.1 ..... TOTAL Result Count = 0
RULECHECK Via1.2 ..... TOTAL Result Count = 0
RULECHECK Via1.3 ..... TOTAL Result Count = 0
RULECHECK Via1.4 ..... TOTAL Result Count = 0
RULECHECK Metal2.1 .... TOTAL Result Count = 0
RULECHECK Metal2.2 .... TOTAL Result Count = 0
RULECHECK Metal2.3 .... TOTAL Result Count = 0
RULECHECK Metal2.4 .... TOTAL Result Count = 0
RULECHECK Via2.1 ..... TOTAL Result Count = 0
RULECHECK Via2.2 ..... TOTAL Result Count = 0
RULECHECK Via2.3 ..... TOTAL Result Count = 0
RULECHECK Via2.4 ..... TOTAL Result Count = 0
RULECHECK Metal3.1 .... TOTAL Result Count = 0
RULECHECK Metal3.2 .... TOTAL Result Count = 0
RULECHECK Metal3.3 .... TOTAL Result Count = 0
RULECHECK Metal3.4 .... TOTAL Result Count = 0
```

```
RULECHECK Via3.1 ..... TOTAL Result Count = 0
RULECHECK Via3.2 ..... TOTAL Result Count = 0
RULECHECK Via3.3 ..... TOTAL Result Count = 0
RULECHECK Via3.4 ..... TOTAL Result Count = 0
RULECHECK Metal4.1 .... TOTAL Result Count = 0
RULECHECK Metal4.2 .... TOTAL Result Count = 0
RULECHECK Metal4.3 .... TOTAL Result Count = 0
RULECHECK Via4.1 ..... TOTAL Result Count = 0
RULECHECK Via4.2 ..... TOTAL Result Count = 0
RULECHECK Via4.3 ..... TOTAL Result Count = 0
RULECHECK Via4.4 ..... TOTAL Result Count = 0
RULECHECK Metal5.1 .... TOTAL Result Count = 0
RULECHECK Metal5.2 .... TOTAL Result Count = 0
RULECHECK Metal5.3 .... TOTAL Result Count = 0
RULECHECK Via5.1 ..... TOTAL Result Count = 0
RULECHECK Via5.2 ..... TOTAL Result Count = 0
RULECHECK Via5.3 ..... TOTAL Result Count = 0
RULECHECK Via5.4 ..... TOTAL Result Count = 0
RULECHECK Metal6.1 .... TOTAL Result Count = 0
RULECHECK Metal6.2 .... TOTAL Result Count = 0
RULECHECK Metal6.3 .... TOTAL Result Count = 0
RULECHECK Via6.1 ..... TOTAL Result Count = 0
RULECHECK Via6.2 ..... TOTAL Result Count = 0
RULECHECK Via6.3 ..... TOTAL Result Count = 0
RULECHECK Via6.4 ..... TOTAL Result Count = 0
RULECHECK Metal7.1 .... TOTAL Result Count = 0
RULECHECK Metal7.2 .... TOTAL Result Count = 0
RULECHECK Metal7.3 .... TOTAL Result Count = 0
RULECHECK Via7.1 ..... TOTAL Result Count = 0
RULECHECK Via7.2 ..... TOTAL Result Count = 0
RULECHECK Via7.3 ..... TOTAL Result Count = 0
RULECHECK Via7.4 ..... TOTAL Result Count = 0
RULECHECK Metal8.1 .... TOTAL Result Count = 0
RULECHECK Metal8.2 .... TOTAL Result Count = 0
RULECHECK Metal8.3 .... TOTAL Result Count = 0
RULECHECK Via8.1 ..... TOTAL Result Count = 0
RULECHECK Via8.2 ..... TOTAL Result Count = 0
RULECHECK Via8.3 ..... TOTAL Result Count = 0
RULECHECK Via8.4 ..... TOTAL Result Count = 0
RULECHECK Metal9.1 .... TOTAL Result Count = 0
RULECHECK Metal9.2 .... TOTAL Result Count = 0
RULECHECK Metal9.3 .... TOTAL Result Count = 0
RULECHECK Via9.1 ..... TOTAL Result Count = 0
RULECHECK Via9.2 ..... TOTAL Result Count = 0
RULECHECK Via9.3 ..... TOTAL Result Count = 0
RULECHECK Via9.4 ..... TOTAL Result Count = 0
RULECHECK Metal10.1 ... TOTAL Result Count = 0
RULECHECK Metal10.2 ... TOTAL Result Count = 0
```

```
RULECHECK Metal10.3 ... TOTAL Result Count = 0
RULECHECK Metal1.5 .... TOTAL Result Count = 0
RULECHECK Metal1.6 .... TOTAL Result Count = 0
RULECHECK Metal1.7 .... TOTAL Result Count = 0
RULECHECK Metal1.8 .... TOTAL Result Count = 0
RULECHECK Metal1.9 .... TOTAL Result Count = 0
RULECHECK Metal2.5 .... TOTAL Result Count = 0
RULECHECK Metal2.6 .... TOTAL Result Count = 0
RULECHECK Metal2.7 .... TOTAL Result Count = 0
RULECHECK Metal2.8 .... TOTAL Result Count = 0
RULECHECK Metal2.9 .... TOTAL Result Count = 0
RULECHECK Metal3.5 .... TOTAL Result Count = 0
RULECHECK Metal3.6 .... TOTAL Result Count = 0
RULECHECK Metal3.7 .... TOTAL Result Count = 0
RULECHECK Metal3.8 .... TOTAL Result Count = 0
RULECHECK Metal3.9 .... TOTAL Result Count = 0
RULECHECK Metal4.5 .... TOTAL Result Count = 0
RULECHECK Metal4.6 .... TOTAL Result Count = 0
RULECHECK Metal4.7 .... TOTAL Result Count = 0
RULECHECK Metal4.8 .... TOTAL Result Count = 0
RULECHECK Metal5.5 .... TOTAL Result Count = 0
RULECHECK Metal5.6 .... TOTAL Result Count = 0
RULECHECK Metal5.7 .... TOTAL Result Count = 0
RULECHECK Metal5.8 .... TOTAL Result Count = 0
RULECHECK Metal6.5 .... TOTAL Result Count = 0
RULECHECK Metal6.6 .... TOTAL Result Count = 0
RULECHECK Metal6.7 .... TOTAL Result Count = 0
RULECHECK Metal6.8 .... TOTAL Result Count = 0
RULECHECK Metal7.5 .... TOTAL Result Count = 0
RULECHECK Metal7.6 .... TOTAL Result Count = 0
RULECHECK Metal7.7 .... TOTAL Result Count = 0
RULECHECK Metal8.5 .... TOTAL Result Count = 0
RULECHECK Metal8.6 .... TOTAL Result Count = 0
RULECHECK Metal8.7 .... TOTAL Result Count = 0
RULECHECK Metal9.5 .... TOTAL Result Count = 0
RULECHECK Metal9.6 .... TOTAL Result Count = 0
RULECHECK Metal10.5 ... TOTAL Result Count = 0
RULECHECK Metal10.6 ... TOTAL Result Count = 0
RULECHECK Grid.1 ...... TOTAL Result Count = 0
RULECHECK Grid.2 ...... TOTAL Result Count = 0
RULECHECK Grid.3 ...... TOTAL Result Count = 0
RULECHECK Grid.4 ...... TOTAL Result Count = 0
RULECHECK Grid.5 ...... TOTAL Result Count = 0
RULECHECK Grid.6 ...... TOTAL Result Count = 0
RULECHECK Grid.7 ...... TOTAL Result Count = 0
RULECHECK Grid.8 ...... TOTAL Result Count = 0
RULECHECK Grid.9 ...... TOTAL Result Count = 0
RULECHECK Grid.10 ..... TOTAL Result Count = 0
```

```
RULECHECK Grid.11 ..... TOTAL Result Count = 0
RULECHECK Grid.12 ..... TOTAL Result Count = 0
RULECHECK Grid.13 ..... TOTAL Result Count = 0
RULECHECK Grid.14 ..... TOTAL Result Count = 0
RULECHECK Grid.15 ..... TOTAL Result Count = 0
RULECHECK Grid.16 ..... TOTAL Result Count = 0
RULECHECK Grid.17 ..... TOTAL Result Count = 0
RULECHECK Grid.18 ..... TOTAL Result Count = 0
RULECHECK Grid.19 ..... TOTAL Result Count = 0
RULECHECK Grid.20 ..... TOTAL Result Count = 0
RULECHECK Grid.21 ..... TOTAL Result Count = 0
RULECHECK Grid.22 ..... TOTAL Result Count = 0
RULECHECK Grid.23 ..... TOTAL Result Count = 0
RULECHECK Grid.24 ..... TOTAL Result Count = 0
RULECHECK Grid.25 ..... TOTAL Result Count = 0
RULECHECK Grid.26 ..... TOTAL Result Count = 0
--------------------------------------------------------------------------
----------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 137
TOTAL DRC RuleChecks Executed:   156
TOTAL DRC Results Generated:     0
```

LVS Report of Custom Inverter with fanout 0

```
 Extraction Errors and Warnings for cell "Inv_FO0.calibre.db"
------------------------------------------------------------


WARNING:  Open circuit - Same name on different nets:
          Name:  "out2"
          (1)  at location  (19.93,7.1)  on layer  11 "metal1"  on net
id  4
```

(2) at location (20.54,7.11) on layer 11 "metal1" on net id 5
The name was assigned to net 4 .

```
##################################################
##                                              ##
##         C A L I B R E    S Y S T E M         ##
##                                              ##
##             L V S   R E P O R T              ##
##                                              ##
##################################################
```

```
REPORT FILE NAME:          Inv_FO0.lvs.report
LAYOUT NAME:               Inv_FO0.calibre.db
SOURCE NAME:               /u/soma2/cadence/LVS-files/Inv_FO0.src.net
('Inv_FO0')
RULE FILE:                 /u/soma2/cadence/LVS-files/_calibreLVS.rul_
RULE FILE TITLE:           LVS Rule File for FreePDK45
LVS MODE:                  Mask
RULE FILE NAME:            /u/soma2/cadence/LVS-files/_calibreLVS.rul_
CREATION TIME:             Mon Mar 13 22:10:00 2017
CURRENT DIRECTORY:         /u/soma2/cadence/LVS-files
USER NAME:                 soma2
CALIBRE VERSION:           v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013
```

```
**************************************************************************
************************************
                          OVERALL COMPARISON RESULTS
**************************************************************************
************************************
```

```
--------------------------------------------------------------------------------
--------------------------------------

NUMBERS OF OBJECTS
------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Nets:               6         6

 Instances:          3         3         mn (4 pins)
                     3         3         mp (4 pins)
                ------    ------
 Total Inst:         6         6



********************************************************************************
************************************
                                          LVS PARAMETERS
********************************************************************************
************************************


o LVS Setup:

   LVS COMPONENT TYPE PROPERTY            element
   LVS COMPONENT SUBTYPE PROPERTY         model
   // LVS PIN NAME PROPERTY
   LVS POWER NAME                         "VDD"
   LVS GROUND NAME                        "VSS" "GROUND"
   LVS CELL SUPPLY                        NO
   LVS RECOGNIZE GATES                    ALL
   LVS IGNORE PORTS                       YES
   LVS CHECK PORT NAMES                   NO
   LVS IGNORE TRIVIAL NAMED PORTS         NO
   LVS BUILTIN DEVICE PIN SWAP            YES
   LVS ALL CAPACITOR PINS SWAPPABLE       NO
   LVS DISCARD PINS BY DEVICE             NO
   LVS SOFT SUBSTRATE PINS                NO
   LVS INJECT LOGIC                       YES
   LVS EXPAND UNBALANCED CELLS            YES
   LVS FLATTEN INSIDE CELL                NO
   LVS EXPAND SEED PROMOTIONS             NO
   LVS PRESERVE PARAMETERIZED CELLS       NO
   LVS GLOBALS ARE PORTS                  YES
   LVS REVERSE WL                         NO
```

```
LVS SPICE PREFER PINS                    NO
LVS SPICE SLASH IS SPACE                 YES
LVS SPICE ALLOW FLOATING PINS            YES
// LVS SPICE ALLOW INLINE PARAMETERS
LVS SPICE ALLOW UNQUOTED STRINGS         NO
LVS SPICE CONDITIONAL LDD                NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS     NO
LVS SPICE IMPLIED MOS AREA               NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS               NO
LVS SPICE REDEFINE PARAM                 NO
LVS SPICE REPLICATE DEVICES              NO
LVS SPICE SCALE X PARAMETERS             NO
LVS SPICE STRICT WL                      NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                      NO
LVS EXACT SUBTYPES                       NO
LAYOUT CASE                              NO
SOURCE CASE                              NO
LVS COMPARE CASE                         NO
LVS DOWNCASE DEVICE                      NO
LVS REPORT MAXIMUM                       50
LVS PROPERTY RESOLUTION MAXIMUM          32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                         YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction

LVS REDUCE SERIES MOS                    YES
LVS REDUCE PARALLEL MOS                  YES
LVS REDUCE SEMI SERIES MOS               YES
LVS REDUCE SPLIT GATES                   YES
LVS REDUCE PARALLEL BIPOLAR              YES
LVS REDUCE SERIES CAPACITORS             YES
LVS REDUCE PARALLEL CAPACITORS           YES
LVS REDUCE SERIES RESISTORS              YES
LVS REDUCE PARALLEL RESISTORS            YES
LVS REDUCE PARALLEL DIODES               YES
LVS REDUCTION PRIORITY                   PARALLEL

LVS SHORT EQUIVALENT NODES               NO

// Trace Property
```

```
   TRACE PROPERTY  mn(nmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  w w 4e-09 ABSOLUTE


********************************************************************************
************************************
                                  INFORMATION AND WARNINGS
********************************************************************************
************************************


                  Matched    Matched    Unmatched    Unmatched
Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    ------
---
   Nets:               6          6            0            0

   Instances:          3          3            0            0
mn(NMOS_VTL)
                       3          3            0            0
mp(PMOS_VTL)
                  -------    -------    ---------    ---------
   Total Inst:         6          6            0            0


o Layout Names That Are Missing In The Source:

   Nets:         out2


o Initial Correspondence Points:
```

```
   Nets:         vdd! gnd!

****************************************************************************
************************************
                                          SUMMARY
****************************************************************************
************************************

Total CPU Time:      0 sec
Total Elapsed Time:  0 sec
```

DRC Report of Custom Inverter with fanout 1:

```
============================================================================
==========
=== CALIBRE::DRC-F SUMMARY REPORT
===
Execution Date/Time:       Sun Mar 12 03:14:43 2017
Calibre Version:           v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013
Rule File Pathname:        /u/soma2/cadence/DRC-files/_calibreDRC.rul_
Rule File Title:
Layout System:             GDS
Layout Path(s):            inverter_custom_fa1.calibre.db
Layout Primary Cell:       inverter_custom_fa0
Current Directory:         /u/soma2/cadence/DRC-files
User Name:                 soma2
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      inverter_custom_fa0.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       inverter_custom_fa0.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID =
NO
```

```
                              NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:            COMMENT TEXT + RULE FILE INFORMATION
Layers:                       MEMORY-BASED
Keep Empty Checks:            YES
--------------------------------------------------------------------------
----------
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------------
----------
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ...... TOTAL Original Geometry Count = 6
LAYER nwell ...... TOTAL Original Geometry Count = 5
LAYER active ..... TOTAL Original Geometry Count = 44
LAYER poly ....... TOTAL Original Geometry Count = 31
LAYER pimplant ... TOTAL Original Geometry Count = 4
LAYER nimplant ... TOTAL Original Geometry Count = 4
LAYER vth ........ TOTAL Original Geometry Count = 0
LAYER vtg ........ TOTAL Original Geometry Count = 0
LAYER metal1 ..... TOTAL Original Geometry Count = 33
LAYER metal2 ..... TOTAL Original Geometry Count = 0
LAYER metal3 ..... TOTAL Original Geometry Count = 0
LAYER metal4 ..... TOTAL Original Geometry Count = 0
LAYER metal5 ..... TOTAL Original Geometry Count = 0
LAYER metal6 ..... TOTAL Original Geometry Count = 0
LAYER metal7 ..... TOTAL Original Geometry Count = 0
LAYER metal8 ..... TOTAL Original Geometry Count = 0
LAYER metal9 ..... TOTAL Original Geometry Count = 0
LAYER metal10 .... TOTAL Original Geometry Count = 0
LAYER contact .... TOTAL Original Geometry Count = 17
LAYER via1 ....... TOTAL Original Geometry Count = 0
LAYER via2 ....... TOTAL Original Geometry Count = 0
LAYER via3 ....... TOTAL Original Geometry Count = 0
LAYER via4 ....... TOTAL Original Geometry Count = 0
LAYER via5 ....... TOTAL Original Geometry Count = 0
LAYER via6 ....... TOTAL Original Geometry Count = 0
LAYER via7 ....... TOTAL Original Geometry Count = 0
LAYER via8 ....... TOTAL Original Geometry Count = 0
LAYER via9 ....... TOTAL Original Geometry Count = 0
--------------------------------------------------------------------------
----------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK Well.1 ...... TOTAL Result Count = 0
RULECHECK Well.2 ...... TOTAL Result Count = 0
RULECHECK Well.4 ...... TOTAL Result Count = 0
```

```
RULECHECK Poly.1 ..... TOTAL Result Count = 0
RULECHECK Poly.2 ..... TOTAL Result Count = 0
RULECHECK Poly.3 ..... TOTAL Result Count = 0
RULECHECK Poly.4 ..... TOTAL Result Count = 0
RULECHECK Poly.5 ..... TOTAL Result Count = 0
RULECHECK Poly.6 ..... TOTAL Result Count = 0
RULECHECK Active.1 .... TOTAL Result Count = 0
RULECHECK Active.2 .... TOTAL Result Count = 0
RULECHECK Active.3 .... TOTAL Result Count = 0
RULECHECK Active.4 .... TOTAL Result Count = 0
RULECHECK Implant.1 ... TOTAL Result Count = 0
RULECHECK Implant.2 ... TOTAL Result Count = 0
RULECHECK Implant.3 ... TOTAL Result Count = 0
RULECHECK Implant.4 ... TOTAL Result Count = 0
RULECHECK Implant.6 ... TOTAL Result Count = 0
RULECHECK Contact.1 ... TOTAL Result Count = 0
RULECHECK Contact.2 ... TOTAL Result Count = 0
RULECHECK Contact.3 ... TOTAL Result Count = 0
RULECHECK Contact.4 ... TOTAL Result Count = 0
RULECHECK Contact.5 ... TOTAL Result Count = 0
RULECHECK Contact.6 ... TOTAL Result Count = 0
RULECHECK Metal1.1 .... TOTAL Result Count = 0
RULECHECK Metal1.2 .... TOTAL Result Count = 0
RULECHECK Metal1.3 .... TOTAL Result Count = 0
RULECHECK Metal1.4 .... TOTAL Result Count = 0
RULECHECK Via1.1 ...... TOTAL Result Count = 0
RULECHECK Via1.2 ...... TOTAL Result Count = 0
RULECHECK Via1.3 ...... TOTAL Result Count = 0
RULECHECK Via1.4 ...... TOTAL Result Count = 0
RULECHECK Metal2.1 .... TOTAL Result Count = 0
RULECHECK Metal2.2 .... TOTAL Result Count = 0
RULECHECK Metal2.3 .... TOTAL Result Count = 0
RULECHECK Metal2.4 .... TOTAL Result Count = 0
RULECHECK Via2.1 ...... TOTAL Result Count = 0
RULECHECK Via2.2 ...... TOTAL Result Count = 0
RULECHECK Via2.3 ...... TOTAL Result Count = 0
RULECHECK Via2.4 ...... TOTAL Result Count = 0
RULECHECK Metal3.1 .... TOTAL Result Count = 0
RULECHECK Metal3.2 .... TOTAL Result Count = 0
RULECHECK Metal3.3 .... TOTAL Result Count = 0
RULECHECK Metal3.4 .... TOTAL Result Count = 0
RULECHECK Via3.1 ...... TOTAL Result Count = 0
RULECHECK Via3.2 ...... TOTAL Result Count = 0
RULECHECK Via3.3 ...... TOTAL Result Count = 0
RULECHECK Via3.4 ...... TOTAL Result Count = 0
RULECHECK Metal4.1 .... TOTAL Result Count = 0
RULECHECK Metal4.2 .... TOTAL Result Count = 0
RULECHECK Metal4.3 .... TOTAL Result Count = 0
```

```
RULECHECK Via4.1 ..... TOTAL Result Count = 0
RULECHECK Via4.2 ..... TOTAL Result Count = 0
RULECHECK Via4.3 ..... TOTAL Result Count = 0
RULECHECK Via4.4 ..... TOTAL Result Count = 0
RULECHECK Metal5.1 .... TOTAL Result Count = 0
RULECHECK Metal5.2 .... TOTAL Result Count = 0
RULECHECK Metal5.3 .... TOTAL Result Count = 0
RULECHECK Via5.1 ..... TOTAL Result Count = 0
RULECHECK Via5.2 ..... TOTAL Result Count = 0
RULECHECK Via5.3 ..... TOTAL Result Count = 0
RULECHECK Via5.4 ..... TOTAL Result Count = 0
RULECHECK Metal6.1 .... TOTAL Result Count = 0
RULECHECK Metal6.2 .... TOTAL Result Count = 0
RULECHECK Metal6.3 .... TOTAL Result Count = 0
RULECHECK Via6.1 ..... TOTAL Result Count = 0
RULECHECK Via6.2 ..... TOTAL Result Count = 0
RULECHECK Via6.3 ..... TOTAL Result Count = 0
RULECHECK Via6.4 ..... TOTAL Result Count = 0
RULECHECK Metal7.1 .... TOTAL Result Count = 0
RULECHECK Metal7.2 .... TOTAL Result Count = 0
RULECHECK Metal7.3 .... TOTAL Result Count = 0
RULECHECK Via7.1 ..... TOTAL Result Count = 0
RULECHECK Via7.2 ..... TOTAL Result Count = 0
RULECHECK Via7.3 ..... TOTAL Result Count = 0
RULECHECK Via7.4 ..... TOTAL Result Count = 0
RULECHECK Metal8.1 .... TOTAL Result Count = 0
RULECHECK Metal8.2 .... TOTAL Result Count = 0
RULECHECK Metal8.3 .... TOTAL Result Count = 0
RULECHECK Via8.1 ..... TOTAL Result Count = 0
RULECHECK Via8.2 ..... TOTAL Result Count = 0
RULECHECK Via8.3 ..... TOTAL Result Count = 0
RULECHECK Via8.4 ..... TOTAL Result Count = 0
RULECHECK Metal9.1 .... TOTAL Result Count = 0
RULECHECK Metal9.2 .... TOTAL Result Count = 0
RULECHECK Metal9.3 .... TOTAL Result Count = 0
RULECHECK Via9.1 ..... TOTAL Result Count = 0
RULECHECK Via9.2 ..... TOTAL Result Count = 0
RULECHECK Via9.3 ..... TOTAL Result Count = 0
RULECHECK Via9.4 ..... TOTAL Result Count = 0
RULECHECK Metal10.1 ... TOTAL Result Count = 0
RULECHECK Metal10.2 ... TOTAL Result Count = 0
RULECHECK Metal10.3 ... TOTAL Result Count = 0
RULECHECK Metal1.5 .... TOTAL Result Count = 0
RULECHECK Metal1.6 .... TOTAL Result Count = 0
RULECHECK Metal1.7 .... TOTAL Result Count = 0
RULECHECK Metal1.8 .... TOTAL Result Count = 0
RULECHECK Metal1.9 .... TOTAL Result Count = 0
RULECHECK Metal2.5 .... TOTAL Result Count = 0
```

```
RULECHECK Metal2.6 .... TOTAL Result Count = 0
RULECHECK Metal2.7 .... TOTAL Result Count = 0
RULECHECK Metal2.8 .... TOTAL Result Count = 0
RULECHECK Metal2.9 .... TOTAL Result Count = 0
RULECHECK Metal3.5 .... TOTAL Result Count = 0
RULECHECK Metal3.6 .... TOTAL Result Count = 0
RULECHECK Metal3.7 .... TOTAL Result Count = 0
RULECHECK Metal3.8 .... TOTAL Result Count = 0
RULECHECK Metal3.9 .... TOTAL Result Count = 0
RULECHECK Metal4.5 .... TOTAL Result Count = 0
RULECHECK Metal4.6 .... TOTAL Result Count = 0
RULECHECK Metal4.7 .... TOTAL Result Count = 0
RULECHECK Metal4.8 .... TOTAL Result Count = 0
RULECHECK Metal5.5 .... TOTAL Result Count = 0
RULECHECK Metal5.6 .... TOTAL Result Count = 0
RULECHECK Metal5.7 .... TOTAL Result Count = 0
RULECHECK Metal5.8 .... TOTAL Result Count = 0
RULECHECK Metal6.5 .... TOTAL Result Count = 0
RULECHECK Metal6.6 .... TOTAL Result Count = 0
RULECHECK Metal6.7 .... TOTAL Result Count = 0
RULECHECK Metal6.8 .... TOTAL Result Count = 0
RULECHECK Metal7.5 .... TOTAL Result Count = 0
RULECHECK Metal7.6 .... TOTAL Result Count = 0
RULECHECK Metal7.7 .... TOTAL Result Count = 0
RULECHECK Metal8.5 .... TOTAL Result Count = 0
RULECHECK Metal8.6 .... TOTAL Result Count = 0
RULECHECK Metal8.7 .... TOTAL Result Count = 0
RULECHECK Metal9.5 .... TOTAL Result Count = 0
RULECHECK Metal9.6 .... TOTAL Result Count = 0
RULECHECK Metal10.5 ... TOTAL Result Count = 0
RULECHECK Metal10.6 ... TOTAL Result Count = 0
RULECHECK Grid.1 ...... TOTAL Result Count = 0
RULECHECK Grid.2 ...... TOTAL Result Count = 0
RULECHECK Grid.3 ...... TOTAL Result Count = 0
RULECHECK Grid.4 ...... TOTAL Result Count = 0
RULECHECK Grid.5 ...... TOTAL Result Count = 0
RULECHECK Grid.6 ...... TOTAL Result Count = 0
RULECHECK Grid.7 ...... TOTAL Result Count = 0
RULECHECK Grid.8 ...... TOTAL Result Count = 0
RULECHECK Grid.9 ...... TOTAL Result Count = 0
RULECHECK Grid.10 ..... TOTAL Result Count = 0
RULECHECK Grid.11 ..... TOTAL Result Count = 0
RULECHECK Grid.12 ..... TOTAL Result Count = 0
RULECHECK Grid.13 ..... TOTAL Result Count = 0
RULECHECK Grid.14 ..... TOTAL Result Count = 0
RULECHECK Grid.15 ..... TOTAL Result Count = 0
RULECHECK Grid.16 ..... TOTAL Result Count = 0
RULECHECK Grid.17 ..... TOTAL Result Count = 0
```

```
RULECHECK Grid.18 ..... TOTAL Result Count = 0
RULECHECK Grid.19 ..... TOTAL Result Count = 0
RULECHECK Grid.20 ..... TOTAL Result Count = 0
RULECHECK Grid.21 ..... TOTAL Result Count = 0
RULECHECK Grid.22 ..... TOTAL Result Count = 0
RULECHECK Grid.23 ..... TOTAL Result Count = 0
RULECHECK Grid.24 ..... TOTAL Result Count = 0
RULECHECK Grid.25 ..... TOTAL Result Count = 0
RULECHECK Grid.26 ..... TOTAL Result Count = 0
--------------------------------------------------------------------------
----------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 144
TOTAL DRC RuleChecks Executed:   156
TOTAL DRC Results Generated:     0
```

LVS Report of Custom Inverter with fanout 1:

```
 Extraction Errors and Warnings for cell "inverter_fa1.calibre.db"
-----------------------------------------------------------------


WARNING:  Open circuit - Same name on different nets:
          Name:  "out2"
          (1)  at location  (19.93,7.1)  on layer  11 "metal1"  on net
id  4
          (2)  at location  (20.54,7.11)  on layer  11 "metal1"  on net
id  5
          The name was assigned to net 4 .
```

##

```
                  ##                                                ##
                  ##        C A L I B R E   S Y S T E M             ##
                  ##                                                ##
                  ##            L V S   R E P O R T                 ##
                  ##                                                ##
                  ################################################
```

```
REPORT FILE NAME:         inverter_fa1.lvs.report
LAYOUT NAME:              inverter_fa1.calibre.db
SOURCE NAME:              /u/soma2/cadence/LVS-
files/inverter_fa1.src.net ('inverter_fa1')
RULE FILE:                /u/soma2/cadence/LVS-files/_calibreLVS.rul_
RULE FILE TITLE:          LVS Rule File for FreePDK45
LVS MODE:                 Mask
RULE FILE NAME:           /u/soma2/cadence/LVS-files/_calibreLVS.rul_
CREATION TIME:            Sun Mar 12 03:22:50 2017
CURRENT DIRECTORY:        /u/soma2/cadence/LVS-files
USER NAME:                soma2
CALIBRE VERSION:          v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013
```

```
**************************************************************************
************************************
                              OVERALL COMPARISON RESULTS
**************************************************************************
************************************
```

```
                        #       ###################       _   _
                      #         #                 #       *   *
                    #   #       #     CORRECT     #         |
                     # #        #                 #       \___/
                      #         ###################
```

```
--------------------------------------------------------------------------
---------------------------------------
```

NUMBERS OF OBJECTS

	Layout	Source	Component Type
Nets:	7	7	

```
 Instances:          4         4         mn (4 pins)
                     4         4         mp (4 pins)
                   ------    ------
 Total Inst:         8         8
```

```
*****************************************************************************
************************************
                                          LVS PARAMETERS
*****************************************************************************
************************************
```

o LVS Setup:

```
   LVS COMPONENT TYPE PROPERTY            element
   LVS COMPONENT SUBTYPE PROPERTY         model
   // LVS PIN NAME PROPERTY
   LVS POWER NAME                         "VDD"
   LVS GROUND NAME                        "VSS" "GROUND"
   LVS CELL SUPPLY                        NO
   LVS RECOGNIZE GATES                    ALL
   LVS IGNORE PORTS                       YES
   LVS CHECK PORT NAMES                   NO
   LVS IGNORE TRIVIAL NAMED PORTS         NO
   LVS BUILTIN DEVICE PIN SWAP            YES
   LVS ALL CAPACITOR PINS SWAPPABLE       NO
   LVS DISCARD PINS BY DEVICE             NO
   LVS SOFT SUBSTRATE PINS                NO
   LVS INJECT LOGIC                       YES
   LVS EXPAND UNBALANCED CELLS            YES
   LVS FLATTEN INSIDE CELL                NO
   LVS EXPAND SEED PROMOTIONS             NO
   LVS PRESERVE PARAMETERIZED CELLS       NO
   LVS GLOBALS ARE PORTS                  YES
   LVS REVERSE WL                         NO
   LVS SPICE PREFER PINS                  NO
   LVS SPICE SLASH IS SPACE               YES
   LVS SPICE ALLOW FLOATING PINS          YES
   // LVS SPICE ALLOW INLINE PARAMETERS
   LVS SPICE ALLOW UNQUOTED STRINGS       NO
   LVS SPICE CONDITIONAL LDD              NO
   LVS SPICE CULL PRIMITIVE SUBCIRCUITS   NO
   LVS SPICE IMPLIED MOS AREA             NO
   // LVS SPICE MULTIPLIER NAME
   LVS SPICE OVERRIDE GLOBALS             NO
   LVS SPICE REDEFINE PARAM               NO
```

```
LVS SPICE REPLICATE DEVICES            NO
LVS SPICE SCALE X PARAMETERS           NO
LVS SPICE STRICT WL                    NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                    NO
LVS EXACT SUBTYPES                     NO
LAYOUT CASE                            NO
SOURCE CASE                            NO
LVS COMPARE CASE                       NO
LVS DOWNCASE DEVICE                    NO
LVS REPORT MAXIMUM                     50
LVS PROPERTY RESOLUTION MAXIMUM        32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                       YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction

LVS REDUCE SERIES MOS                  YES
LVS REDUCE PARALLEL MOS                YES
LVS REDUCE SEMI SERIES MOS             YES
LVS REDUCE SPLIT GATES                 YES
LVS REDUCE PARALLEL BIPOLAR            YES
LVS REDUCE SERIES CAPACITORS           YES
LVS REDUCE PARALLEL CAPACITORS         YES
LVS REDUCE SERIES RESISTORS            YES
LVS REDUCE PARALLEL RESISTORS          YES
LVS REDUCE PARALLEL DIODES             YES
LVS REDUCTION PRIORITY                 PARALLEL

LVS SHORT EQUIVALENT NODES             NO

// Trace Property

TRACE PROPERTY  mn(nmos_vtl)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtl)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtl)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtl)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vth)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vth)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vth)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vth)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtg)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtg)  w w 4e-09 ABSOLUTE
```

```
   TRACE PROPERTY  mp(pmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  w w 4e-09 ABSOLUTE


********************************************************************************
************************************
                                INFORMATION AND WARNINGS
********************************************************************************
************************************


                  Matched    Matched    Unmatched    Unmatched
Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    ------
---
   Nets:               7          7            0            0

   Instances:          4          4            0            0
mn(NMOS_VTL)
                       4          4            0            0
mp(PMOS_VTL)
                  -------    -------    ---------    ---------
   Total Inst:         8          8            0            0


o Layout Names That Are Missing In The Source:

   Nets:         out2 Y


o Initial Correspondence Points:

   Nets:         in vdd! out gnd!


********************************************************************************
************************************
                                          SUMMARY
********************************************************************************
************************************

Total CPU Time:      0 sec
```

```
Total Elapsed Time:  0 sec
```

DRC Report of Custom Inverter with fanout 2:

```
================================================================================
==========
=== CALIBRE::DRC-F SUMMARY REPORT
===
Execution Date/Time:       Mon Mar 13 02:43:08 2017
Calibre Version:           v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013
Rule File Pathname:        /u/soma2/cadence/DRC-files/_calibreDRC.rul_
Rule File Title:
Layout System:             GDS
Layout Path(s):            inverter_fa2.calibre.db
Layout Primary Cell:       inverter_fa2
Current Directory:         /u/soma2/cadence/DRC-files
User Name:                 soma2
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      inverter_fa2.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       inverter_fa2.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID =
NO
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:         COMMENT TEXT + RULE FILE INFORMATION
Layers:                    MEMORY-BASED
Keep Empty Checks:         YES
--------------------------------------------------------------------------
----------
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------------
----------
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ...... TOTAL Original Geometry Count = 7
LAYER nwell ...... TOTAL Original Geometry Count = 7
LAYER active ..... TOTAL Original Geometry Count = 72
LAYER poly ....... TOTAL Original Geometry Count = 45
LAYER pimplant ... TOTAL Original Geometry Count = 6
LAYER nimplant ... TOTAL Original Geometry Count = 6
LAYER vth ........ TOTAL Original Geometry Count = 0
```

```
LAYER vtg ........ TOTAL Original Geometry Count = 0
LAYER metal1 ..... TOTAL Original Geometry Count = 54
LAYER metal2 ..... TOTAL Original Geometry Count = 5
LAYER metal3 ..... TOTAL Original Geometry Count = 0
LAYER metal4 ..... TOTAL Original Geometry Count = 0
LAYER metal5 ..... TOTAL Original Geometry Count = 0
LAYER metal6 ..... TOTAL Original Geometry Count = 0
LAYER metal7 ..... TOTAL Original Geometry Count = 0
LAYER metal8 ..... TOTAL Original Geometry Count = 0
LAYER metal9 ..... TOTAL Original Geometry Count = 0
LAYER metal10 .... TOTAL Original Geometry Count = 0
LAYER contact .... TOTAL Original Geometry Count = 27
LAYER via1 ....... TOTAL Original Geometry Count = 2
LAYER via2 ....... TOTAL Original Geometry Count = 0
LAYER via3 ....... TOTAL Original Geometry Count = 0
LAYER via4 ....... TOTAL Original Geometry Count = 0
LAYER via5 ....... TOTAL Original Geometry Count = 0
LAYER via6 ....... TOTAL Original Geometry Count = 0
LAYER via7 ....... TOTAL Original Geometry Count = 0
LAYER via8 ....... TOTAL Original Geometry Count = 0
LAYER via9 ....... TOTAL Original Geometry Count = 0
--------------------------------------------------------------------------
----------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK Well.1 ...... TOTAL Result Count = 0
RULECHECK Well.2 ...... TOTAL Result Count = 0
RULECHECK Well.4 ...... TOTAL Result Count = 0
RULECHECK Poly.1 ...... TOTAL Result Count = 0
RULECHECK Poly.2 ...... TOTAL Result Count = 0
RULECHECK Poly.3 ...... TOTAL Result Count = 0
RULECHECK Poly.4 ...... TOTAL Result Count = 0
RULECHECK Poly.5 ...... TOTAL Result Count = 0
RULECHECK Poly.6 ...... TOTAL Result Count = 0
RULECHECK Active.1 .... TOTAL Result Count = 0
RULECHECK Active.2 .... TOTAL Result Count = 0
RULECHECK Active.3 .... TOTAL Result Count = 0
RULECHECK Active.4 .... TOTAL Result Count = 0
RULECHECK Implant.1 ... TOTAL Result Count = 0
RULECHECK Implant.2 ... TOTAL Result Count = 0
RULECHECK Implant.3 ... TOTAL Result Count = 0
RULECHECK Implant.4 ... TOTAL Result Count = 0
RULECHECK Implant.6 ... TOTAL Result Count = 0
RULECHECK Contact.1 ... TOTAL Result Count = 0
RULECHECK Contact.2 ... TOTAL Result Count = 0
RULECHECK Contact.3 ... TOTAL Result Count = 0
RULECHECK Contact.4 ... TOTAL Result Count = 0
RULECHECK Contact.5 ... TOTAL Result Count = 0
```

```
RULECHECK Contact.6 ... TOTAL Result Count = 0
RULECHECK Metal1.1 .... TOTAL Result Count = 0
RULECHECK Metal1.2 .... TOTAL Result Count = 0
RULECHECK Metal1.3 .... TOTAL Result Count = 0
RULECHECK Metal1.4 .... TOTAL Result Count = 0
RULECHECK Via1.1 ...... TOTAL Result Count = 0
RULECHECK Via1.2 ...... TOTAL Result Count = 0
RULECHECK Via1.3 ...... TOTAL Result Count = 0
RULECHECK Via1.4 ...... TOTAL Result Count = 0
RULECHECK Metal2.1 .... TOTAL Result Count = 0
RULECHECK Metal2.2 .... TOTAL Result Count = 0
RULECHECK Metal2.3 .... TOTAL Result Count = 0
RULECHECK Metal2.4 .... TOTAL Result Count = 0
RULECHECK Via2.1 ...... TOTAL Result Count = 0
RULECHECK Via2.2 ...... TOTAL Result Count = 0
RULECHECK Via2.3 ...... TOTAL Result Count = 0
RULECHECK Via2.4 ...... TOTAL Result Count = 0
RULECHECK Metal3.1 .... TOTAL Result Count = 0
RULECHECK Metal3.2 .... TOTAL Result Count = 0
RULECHECK Metal3.3 .... TOTAL Result Count = 0
RULECHECK Metal3.4 .... TOTAL Result Count = 0
RULECHECK Via3.1 ...... TOTAL Result Count = 0
RULECHECK Via3.2 ...... TOTAL Result Count = 0
RULECHECK Via3.3 ...... TOTAL Result Count = 0
RULECHECK Via3.4 ...... TOTAL Result Count = 0
RULECHECK Metal4.1 .... TOTAL Result Count = 0
RULECHECK Metal4.2 .... TOTAL Result Count = 0
RULECHECK Metal4.3 .... TOTAL Result Count = 0
RULECHECK Via4.1 ...... TOTAL Result Count = 0
RULECHECK Via4.2 ...... TOTAL Result Count = 0
RULECHECK Via4.3 ...... TOTAL Result Count = 0
RULECHECK Via4.4 ...... TOTAL Result Count = 0
RULECHECK Metal5.1 .... TOTAL Result Count = 0
RULECHECK Metal5.2 .... TOTAL Result Count = 0
RULECHECK Metal5.3 .... TOTAL Result Count = 0
RULECHECK Via5.1 ...... TOTAL Result Count = 0
RULECHECK Via5.2 ...... TOTAL Result Count = 0
RULECHECK Via5.3 ...... TOTAL Result Count = 0
RULECHECK Via5.4 ...... TOTAL Result Count = 0
RULECHECK Metal6.1 .... TOTAL Result Count = 0
RULECHECK Metal6.2 .... TOTAL Result Count = 0
RULECHECK Metal6.3 .... TOTAL Result Count = 0
RULECHECK Via6.1 ...... TOTAL Result Count = 0
RULECHECK Via6.2 ...... TOTAL Result Count = 0
RULECHECK Via6.3 ...... TOTAL Result Count = 0
RULECHECK Via6.4 ...... TOTAL Result Count = 0
RULECHECK Metal7.1 .... TOTAL Result Count = 0
RULECHECK Metal7.2 .... TOTAL Result Count = 0
```

```
RULECHECK Metal7.3 .... TOTAL Result Count = 0
RULECHECK Via7.1 ...... TOTAL Result Count = 0
RULECHECK Via7.2 ...... TOTAL Result Count = 0
RULECHECK Via7.3 ...... TOTAL Result Count = 0
RULECHECK Via7.4 ...... TOTAL Result Count = 0
RULECHECK Metal8.1 .... TOTAL Result Count = 0
RULECHECK Metal8.2 .... TOTAL Result Count = 0
RULECHECK Metal8.3 .... TOTAL Result Count = 0
RULECHECK Via8.1 ...... TOTAL Result Count = 0
RULECHECK Via8.2 ...... TOTAL Result Count = 0
RULECHECK Via8.3 ...... TOTAL Result Count = 0
RULECHECK Via8.4 ...... TOTAL Result Count = 0
RULECHECK Metal9.1 .... TOTAL Result Count = 0
RULECHECK Metal9.2 .... TOTAL Result Count = 0
RULECHECK Metal9.3 .... TOTAL Result Count = 0
RULECHECK Via9.1 ...... TOTAL Result Count = 0
RULECHECK Via9.2 ...... TOTAL Result Count = 0
RULECHECK Via9.3 ...... TOTAL Result Count = 0
RULECHECK Via9.4 ...... TOTAL Result Count = 0
RULECHECK Metal10.1 ... TOTAL Result Count = 0
RULECHECK Metal10.2 ... TOTAL Result Count = 0
RULECHECK Metal10.3 ... TOTAL Result Count = 0
RULECHECK Metal1.5 .... TOTAL Result Count = 0
RULECHECK Metal1.6 .... TOTAL Result Count = 0
RULECHECK Metal1.7 .... TOTAL Result Count = 0
RULECHECK Metal1.8 .... TOTAL Result Count = 0
RULECHECK Metal1.9 .... TOTAL Result Count = 0
RULECHECK Metal2.5 .... TOTAL Result Count = 0
RULECHECK Metal2.6 .... TOTAL Result Count = 0
RULECHECK Metal2.7 .... TOTAL Result Count = 0
RULECHECK Metal2.8 .... TOTAL Result Count = 0
RULECHECK Metal2.9 .... TOTAL Result Count = 0
RULECHECK Metal3.5 .... TOTAL Result Count = 0
RULECHECK Metal3.6 .... TOTAL Result Count = 0
RULECHECK Metal3.7 .... TOTAL Result Count = 0
RULECHECK Metal3.8 .... TOTAL Result Count = 0
RULECHECK Metal3.9 .... TOTAL Result Count = 0
RULECHECK Metal4.5 .... TOTAL Result Count = 0
RULECHECK Metal4.6 .... TOTAL Result Count = 0
RULECHECK Metal4.7 .... TOTAL Result Count = 0
RULECHECK Metal4.8 .... TOTAL Result Count = 0
RULECHECK Metal5.5 .... TOTAL Result Count = 0
RULECHECK Metal5.6 .... TOTAL Result Count = 0
RULECHECK Metal5.7 .... TOTAL Result Count = 0
RULECHECK Metal5.8 .... TOTAL Result Count = 0
RULECHECK Metal6.5 .... TOTAL Result Count = 0
RULECHECK Metal6.6 .... TOTAL Result Count = 0
RULECHECK Metal6.7 .... TOTAL Result Count = 0
```

```
RULECHECK Metal6.8 .... TOTAL Result Count = 0
RULECHECK Metal7.5 .... TOTAL Result Count = 0
RULECHECK Metal7.6 .... TOTAL Result Count = 0
RULECHECK Metal7.7 .... TOTAL Result Count = 0
RULECHECK Metal8.5 .... TOTAL Result Count = 0
RULECHECK Metal8.6 .... TOTAL Result Count = 0
RULECHECK Metal8.7 .... TOTAL Result Count = 0
RULECHECK Metal9.5 .... TOTAL Result Count = 0
RULECHECK Metal9.6 .... TOTAL Result Count = 0
RULECHECK Metal10.5 ... TOTAL Result Count = 0
RULECHECK Metal10.6 ... TOTAL Result Count = 0
RULECHECK Grid.1 ...... TOTAL Result Count = 0
RULECHECK Grid.2 ...... TOTAL Result Count = 0
RULECHECK Grid.3 ...... TOTAL Result Count = 0
RULECHECK Grid.4 ...... TOTAL Result Count = 0
RULECHECK Grid.5 ...... TOTAL Result Count = 0
RULECHECK Grid.6 ...... TOTAL Result Count = 0
RULECHECK Grid.7 ...... TOTAL Result Count = 0
RULECHECK Grid.8 ...... TOTAL Result Count = 0
RULECHECK Grid.9 ...... TOTAL Result Count = 0
RULECHECK Grid.10 ..... TOTAL Result Count = 0
RULECHECK Grid.11 ..... TOTAL Result Count = 0
RULECHECK Grid.12 ..... TOTAL Result Count = 0
RULECHECK Grid.13 ..... TOTAL Result Count = 0
RULECHECK Grid.14 ..... TOTAL Result Count = 0
RULECHECK Grid.15 ..... TOTAL Result Count = 0
RULECHECK Grid.16 ..... TOTAL Result Count = 0
RULECHECK Grid.17 ..... TOTAL Result Count = 0
RULECHECK Grid.18 ..... TOTAL Result Count = 0
RULECHECK Grid.19 ..... TOTAL Result Count = 0
RULECHECK Grid.20 ..... TOTAL Result Count = 0
RULECHECK Grid.21 ..... TOTAL Result Count = 0
RULECHECK Grid.22 ..... TOTAL Result Count = 0
RULECHECK Grid.23 ..... TOTAL Result Count = 0
RULECHECK Grid.24 ..... TOTAL Result Count = 0
RULECHECK Grid.25 ..... TOTAL Result Count = 0
RULECHECK Grid.26 ..... TOTAL Result Count = 0
--------------------------------------------------------------------------
----------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 231
TOTAL DRC RuleChecks Executed:   156
TOTAL DRC Results Generated:     0
```

LVS Report of Custom Inverter with fanouts 2:

```
 Extraction Errors and Warnings for cell "inverter_fa2.calibre.db"
------------------------------------------------------------------


WARNING:  Open circuit - Same name on different nets:
          Name:  "out2"
          (1)  at location  (19.93,7.1)  on layer  11 "metal1"  on net
id  5
          (2)  at location  (20.54,7.11)  on layer  11 "metal1"  on net
id  6
          (3)  at location  (22.49,7.095)  on layer  11 "metal1"  on net
id  8
          The name was assigned to net 5 .




                  ################################################
                  ##                                            ##
                  ##         C A L I B R E   S Y S T E M        ##
                  ##                                            ##
                  ##             L V S   R E P O R T            ##
                  ##                                            ##
                  ################################################



REPORT FILE NAME:         inverter_fa2.lvs.report
LAYOUT NAME:              inverter_fa2.calibre.db
SOURCE NAME:              /u/soma2/cadence/LVS-
files/inverter_fa2.src.net ('inverter_fa2')
RULE FILE:                /u/soma2/cadence/LVS-files/_calibreLVS.rul_
RULE FILE TITLE:          LVS Rule File for FreePDK45
LVS MODE:                 Mask
RULE FILE NAME:           /u/soma2/cadence/LVS-files/_calibreLVS.rul_
CREATION TIME:            Mon Mar 13 02:44:17 2017
CURRENT DIRECTORY:        /u/soma2/cadence/LVS-files
USER NAME:                soma2
```

CALIBRE VERSION: v2013.2_35.25 Wed Jul 3 15:43:57 PDT 2013

****
****
OVERALL COMPARISON RESULTS
****
****

Warning: Ambiguity points were found and resolved arbitrarily.

NUMBERS OF OBJECTS

	Layout	Source	Component Type
Nets:	8	8	
Instances:	5	5	mn (4 pins)
	5	5	mp (4 pins)
Total Inst:	10	10	

****
****
LVS PARAMETERS
****
****

o LVS Setup:

```
   LVS COMPONENT TYPE PROPERTY            element
   LVS COMPONENT SUBTYPE PROPERTY         model
   // LVS PIN NAME PROPERTY
```

```
LVS POWER NAME                          "VDD"
LVS GROUND NAME                         "VSS" "GROUND"
LVS CELL SUPPLY                         NO
LVS RECOGNIZE GATES                     ALL
LVS IGNORE PORTS                        YES
LVS CHECK PORT NAMES                    NO
LVS IGNORE TRIVIAL NAMED PORTS          NO
LVS BUILTIN DEVICE PIN SWAP             YES
LVS ALL CAPACITOR PINS SWAPPABLE        NO
LVS DISCARD PINS BY DEVICE              NO
LVS SOFT SUBSTRATE PINS                 NO
LVS INJECT LOGIC                        YES
LVS EXPAND UNBALANCED CELLS             YES
LVS FLATTEN INSIDE CELL                 NO
LVS EXPAND SEED PROMOTIONS              NO
LVS PRESERVE PARAMETERIZED CELLS        NO
LVS GLOBALS ARE PORTS                   YES
LVS REVERSE WL                          NO
LVS SPICE PREFER PINS                   NO
LVS SPICE SLASH IS SPACE                YES
LVS SPICE ALLOW FLOATING PINS           YES
// LVS SPICE ALLOW INLINE PARAMETERS
LVS SPICE ALLOW UNQUOTED STRINGS        NO
LVS SPICE CONDITIONAL LDD               NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS    NO
LVS SPICE IMPLIED MOS AREA              NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS              NO
LVS SPICE REDEFINE PARAM                NO
LVS SPICE REPLICATE DEVICES             NO
LVS SPICE SCALE X PARAMETERS            NO
LVS SPICE STRICT WL                     NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                     NO
LVS EXACT SUBTYPES                      NO
LAYOUT CASE                             NO
SOURCE CASE                             NO
LVS COMPARE CASE                        NO
LVS DOWNCASE DEVICE                     NO
LVS REPORT MAXIMUM                      50
LVS PROPERTY RESOLUTION MAXIMUM         32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                        YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE
```

```
// Reduction

LVS REDUCE SERIES MOS                   YES
LVS REDUCE PARALLEL MOS                 YES
LVS REDUCE SEMI SERIES MOS              YES
LVS REDUCE SPLIT GATES                  YES
LVS REDUCE PARALLEL BIPOLAR             YES
LVS REDUCE SERIES CAPACITORS            YES
LVS REDUCE PARALLEL CAPACITORS          YES
LVS REDUCE SERIES RESISTORS             YES
LVS REDUCE PARALLEL RESISTORS           YES
LVS REDUCE PARALLEL DIODES              YES
LVS REDUCTION PRIORITY                  PARALLEL

LVS SHORT EQUIVALENT NODES              NO

// Trace Property

TRACE PROPERTY  mn(nmos_vtl)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtl)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtl)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtl)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vth)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vth)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vth)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vth)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtg)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtg)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtg)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtg)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_thkox)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_thkox)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_thkox)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_thkox)  w w 4e-09 ABSOLUTE


********************************************************************************
************************************
                                INFORMATION AND WARNINGS
********************************************************************************
************************************


                  Matched    Matched    Unmatched    Unmatched
Component
                   Layout     Source       Layout       Source    Type
```

```
                  -------    -------    ---------    ---------    ------
---
   Nets:                8          8            0            0

   Instances:           5          5            0            0
mn(NMOS_VTL)
                        5          5            0            0
mp(PMOS_VTL)
                  -------    -------    ---------    ---------
   Total Inst:         10         10            0            0


o Statistics:

   1 net was matched arbitrarily.


o Layout Names That Are Missing In The Source:

   Nets:         out2 Y out


o Initial Correspondence Points:

   Nets:         in vdd! gnd!


o Ambiguity Resolution Points:

      (Each one of the following objects belongs to a group of
indistinguishable objects.
       The listed objects were matched arbitrarily by the Ambiguity
Resolution feature of LVS.
       Arbitrary matching may be prevented by assigning names to these
objects or to adjacent nets).

       Layout                                                    Source
       ------                                                    ------

                                    Nets
                                    ----

       8(22.315,6.610)                                           net07



*************************************************************************
************************************
```

```
                                                SUMMARY
********************************************************************************
************************************

Total CPU Time:      0 sec
Total Elapsed Time:  0 sec
```

DRC Report of Custom Inverter with fanouts 4:

```
================================================================================
==========
=== CALIBRE::DRC-F SUMMARY REPORT
===
Execution Date/Time:       Mon Mar 13 05:12:22 2017
Calibre Version:           v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013
Rule File Pathname:        /u/soma2/cadence/DRC-files/_calibreDRC.rul_
Rule File Title:
Layout System:             GDS
Layout Path(s):            inverter_fa4.calibre.db
Layout Primary Cell:       inverter_fa4
Current Directory:         /u/soma2/cadence/DRC-files
User Name:                 soma2
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      inverter_fa4.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       inverter_fa4.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID =
NO
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:         COMMENT TEXT + RULE FILE INFORMATION
Layers:                    MEMORY-BASED
Keep Empty Checks:         YES
--------------------------------------------------------------------------------
----------
--- RUNTIME WARNINGS
---
```

```
--------------------------------------------------------------------------
----------
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ...... TOTAL Original Geometry Count = 10
LAYER nwell ...... TOTAL Original Geometry Count = 10
LAYER active ..... TOTAL Original Geometry Count = 102
LAYER poly ....... TOTAL Original Geometry Count = 63
LAYER pimplant ... TOTAL Original Geometry Count = 9
LAYER nimplant ... TOTAL Original Geometry Count = 9
LAYER vth ........ TOTAL Original Geometry Count = 0
LAYER vtg ........ TOTAL Original Geometry Count = 0
LAYER metal1 ..... TOTAL Original Geometry Count = 79
LAYER metal2 ..... TOTAL Original Geometry Count = 5
LAYER metal3 ..... TOTAL Original Geometry Count = 0
LAYER metal4 ..... TOTAL Original Geometry Count = 0
LAYER metal5 ..... TOTAL Original Geometry Count = 0
LAYER metal6 ..... TOTAL Original Geometry Count = 0
LAYER metal7 ..... TOTAL Original Geometry Count = 0
LAYER metal8 ..... TOTAL Original Geometry Count = 0
LAYER metal9 ..... TOTAL Original Geometry Count = 0
LAYER metal10 .... TOTAL Original Geometry Count = 0
LAYER contact .... TOTAL Original Geometry Count = 39
LAYER via1 ....... TOTAL Original Geometry Count = 4
LAYER via2 ....... TOTAL Original Geometry Count = 0
LAYER via3 ....... TOTAL Original Geometry Count = 0
LAYER via4 ....... TOTAL Original Geometry Count = 0
LAYER via5 ....... TOTAL Original Geometry Count = 0
LAYER via6 ....... TOTAL Original Geometry Count = 0
LAYER via7 ....... TOTAL Original Geometry Count = 0
LAYER via8 ....... TOTAL Original Geometry Count = 0
LAYER via9 ....... TOTAL Original Geometry Count = 0
--------------------------------------------------------------------------
----------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK Well.1 ...... TOTAL Result Count = 0
RULECHECK Well.2 ...... TOTAL Result Count = 0
RULECHECK Well.4 ...... TOTAL Result Count = 0
RULECHECK Poly.1 ...... TOTAL Result Count = 0
RULECHECK Poly.2 ...... TOTAL Result Count = 0
RULECHECK Poly.3 ...... TOTAL Result Count = 0
RULECHECK Poly.4 ...... TOTAL Result Count = 0
RULECHECK Poly.5 ...... TOTAL Result Count = 0
RULECHECK Poly.6 ...... TOTAL Result Count = 0
RULECHECK Active.1 .... TOTAL Result Count = 0
RULECHECK Active.2 .... TOTAL Result Count = 0
RULECHECK Active.3 .... TOTAL Result Count = 0
```

```
RULECHECK Active.4 .... TOTAL Result Count = 0
RULECHECK Implant.1 ... TOTAL Result Count = 0
RULECHECK Implant.2 ... TOTAL Result Count = 0
RULECHECK Implant.3 ... TOTAL Result Count = 0
RULECHECK Implant.4 ... TOTAL Result Count = 0
RULECHECK Implant.6 ... TOTAL Result Count = 0
RULECHECK Contact.1 ... TOTAL Result Count = 0
RULECHECK Contact.2 ... TOTAL Result Count = 0
RULECHECK Contact.3 ... TOTAL Result Count = 0
RULECHECK Contact.4 ... TOTAL Result Count = 0
RULECHECK Contact.5 ... TOTAL Result Count = 0
RULECHECK Contact.6 ... TOTAL Result Count = 0
RULECHECK Metal1.1 .... TOTAL Result Count = 0
RULECHECK Metal1.2 .... TOTAL Result Count = 0
RULECHECK Metal1.3 .... TOTAL Result Count = 0
RULECHECK Metal1.4 .... TOTAL Result Count = 0
RULECHECK Via1.1 ...... TOTAL Result Count = 0
RULECHECK Via1.2 ...... TOTAL Result Count = 0
RULECHECK Via1.3 ...... TOTAL Result Count = 0
RULECHECK Via1.4 ...... TOTAL Result Count = 0
RULECHECK Metal2.1 .... TOTAL Result Count = 0
RULECHECK Metal2.2 .... TOTAL Result Count = 0
RULECHECK Metal2.3 .... TOTAL Result Count = 0
RULECHECK Metal2.4 .... TOTAL Result Count = 0
RULECHECK Via2.1 ...... TOTAL Result Count = 0
RULECHECK Via2.2 ...... TOTAL Result Count = 0
RULECHECK Via2.3 ...... TOTAL Result Count = 0
RULECHECK Via2.4 ...... TOTAL Result Count = 0
RULECHECK Metal3.1 .... TOTAL Result Count = 0
RULECHECK Metal3.2 .... TOTAL Result Count = 0
RULECHECK Metal3.3 .... TOTAL Result Count = 0
RULECHECK Metal3.4 .... TOTAL Result Count = 0
RULECHECK Via3.1 ...... TOTAL Result Count = 0
RULECHECK Via3.2 ...... TOTAL Result Count = 0
RULECHECK Via3.3 ...... TOTAL Result Count = 0
RULECHECK Via3.4 ...... TOTAL Result Count = 0
RULECHECK Metal4.1 .... TOTAL Result Count = 0
RULECHECK Metal4.2 .... TOTAL Result Count = 0
RULECHECK Metal4.3 .... TOTAL Result Count = 0
RULECHECK Via4.1 ...... TOTAL Result Count = 0
RULECHECK Via4.2 ...... TOTAL Result Count = 0
RULECHECK Via4.3 ...... TOTAL Result Count = 0
RULECHECK Via4.4 ...... TOTAL Result Count = 0
RULECHECK Metal5.1 .... TOTAL Result Count = 0
RULECHECK Metal5.2 .... TOTAL Result Count = 0
RULECHECK Metal5.3 .... TOTAL Result Count = 0
RULECHECK Via5.1 ...... TOTAL Result Count = 0
RULECHECK Via5.2 ...... TOTAL Result Count = 0
```

```
RULECHECK Via5.3 ..... TOTAL Result Count = 0
RULECHECK Via5.4 ..... TOTAL Result Count = 0
RULECHECK Metal6.1 .... TOTAL Result Count = 0
RULECHECK Metal6.2 .... TOTAL Result Count = 0
RULECHECK Metal6.3 .... TOTAL Result Count = 0
RULECHECK Via6.1 ..... TOTAL Result Count = 0
RULECHECK Via6.2 ..... TOTAL Result Count = 0
RULECHECK Via6.3 ..... TOTAL Result Count = 0
RULECHECK Via6.4 ..... TOTAL Result Count = 0
RULECHECK Metal7.1 .... TOTAL Result Count = 0
RULECHECK Metal7.2 .... TOTAL Result Count = 0
RULECHECK Metal7.3 .... TOTAL Result Count = 0
RULECHECK Via7.1 ..... TOTAL Result Count = 0
RULECHECK Via7.2 ..... TOTAL Result Count = 0
RULECHECK Via7.3 ..... TOTAL Result Count = 0
RULECHECK Via7.4 ..... TOTAL Result Count = 0
RULECHECK Metal8.1 .... TOTAL Result Count = 0
RULECHECK Metal8.2 .... TOTAL Result Count = 0
RULECHECK Metal8.3 .... TOTAL Result Count = 0
RULECHECK Via8.1 ..... TOTAL Result Count = 0
RULECHECK Via8.2 ..... TOTAL Result Count = 0
RULECHECK Via8.3 ..... TOTAL Result Count = 0
RULECHECK Via8.4 ..... TOTAL Result Count = 0
RULECHECK Metal9.1 .... TOTAL Result Count = 0
RULECHECK Metal9.2 .... TOTAL Result Count = 0
RULECHECK Metal9.3 .... TOTAL Result Count = 0
RULECHECK Via9.1 ..... TOTAL Result Count = 0
RULECHECK Via9.2 ..... TOTAL Result Count = 0
RULECHECK Via9.3 ..... TOTAL Result Count = 0
RULECHECK Via9.4 ..... TOTAL Result Count = 0
RULECHECK Metal10.1 ... TOTAL Result Count = 0
RULECHECK Metal10.2 ... TOTAL Result Count = 0
RULECHECK Metal10.3 ... TOTAL Result Count = 0
RULECHECK Metal1.5 .... TOTAL Result Count = 0
RULECHECK Metal1.6 .... TOTAL Result Count = 0
RULECHECK Metal1.7 .... TOTAL Result Count = 0
RULECHECK Metal1.8 .... TOTAL Result Count = 0
RULECHECK Metal1.9 .... TOTAL Result Count = 0
RULECHECK Metal2.5 .... TOTAL Result Count = 0
RULECHECK Metal2.6 .... TOTAL Result Count = 0
RULECHECK Metal2.7 .... TOTAL Result Count = 0
RULECHECK Metal2.8 .... TOTAL Result Count = 0
RULECHECK Metal2.9 .... TOTAL Result Count = 0
RULECHECK Metal3.5 .... TOTAL Result Count = 0
RULECHECK Metal3.6 .... TOTAL Result Count = 0
RULECHECK Metal3.7 .... TOTAL Result Count = 0
RULECHECK Metal3.8 .... TOTAL Result Count = 0
RULECHECK Metal3.9 .... TOTAL Result Count = 0
```

```
RULECHECK Metal4.5 .... TOTAL Result Count = 0
RULECHECK Metal4.6 .... TOTAL Result Count = 0
RULECHECK Metal4.7 .... TOTAL Result Count = 0
RULECHECK Metal4.8 .... TOTAL Result Count = 0
RULECHECK Metal5.5 .... TOTAL Result Count = 0
RULECHECK Metal5.6 .... TOTAL Result Count = 0
RULECHECK Metal5.7 .... TOTAL Result Count = 0
RULECHECK Metal5.8 .... TOTAL Result Count = 0
RULECHECK Metal6.5 .... TOTAL Result Count = 0
RULECHECK Metal6.6 .... TOTAL Result Count = 0
RULECHECK Metal6.7 .... TOTAL Result Count = 0
RULECHECK Metal6.8 .... TOTAL Result Count = 0
RULECHECK Metal7.5 .... TOTAL Result Count = 0
RULECHECK Metal7.6 .... TOTAL Result Count = 0
RULECHECK Metal7.7 .... TOTAL Result Count = 0
RULECHECK Metal8.5 .... TOTAL Result Count = 0
RULECHECK Metal8.6 .... TOTAL Result Count = 0
RULECHECK Metal8.7 .... TOTAL Result Count = 0
RULECHECK Metal9.5 .... TOTAL Result Count = 0
RULECHECK Metal9.6 .... TOTAL Result Count = 0
RULECHECK Metal10.5 ... TOTAL Result Count = 0
RULECHECK Metal10.6 ... TOTAL Result Count = 0
RULECHECK Grid.1 ...... TOTAL Result Count = 0
RULECHECK Grid.2 ...... TOTAL Result Count = 0
RULECHECK Grid.3 ...... TOTAL Result Count = 0
RULECHECK Grid.4 ...... TOTAL Result Count = 0
RULECHECK Grid.5 ...... TOTAL Result Count = 0
RULECHECK Grid.6 ...... TOTAL Result Count = 0
RULECHECK Grid.7 ...... TOTAL Result Count = 0
RULECHECK Grid.8 ...... TOTAL Result Count = 0
RULECHECK Grid.9 ...... TOTAL Result Count = 0
RULECHECK Grid.10 ..... TOTAL Result Count = 0
RULECHECK Grid.11 ..... TOTAL Result Count = 0
RULECHECK Grid.12 ..... TOTAL Result Count = 0
RULECHECK Grid.13 ..... TOTAL Result Count = 0
RULECHECK Grid.14 ..... TOTAL Result Count = 0
RULECHECK Grid.15 ..... TOTAL Result Count = 0
RULECHECK Grid.16 ..... TOTAL Result Count = 0
RULECHECK Grid.17 ..... TOTAL Result Count = 0
RULECHECK Grid.18 ..... TOTAL Result Count = 0
RULECHECK Grid.19 ..... TOTAL Result Count = 0
RULECHECK Grid.20 ..... TOTAL Result Count = 0
RULECHECK Grid.21 ..... TOTAL Result Count = 0
RULECHECK Grid.22 ..... TOTAL Result Count = 0
RULECHECK Grid.23 ..... TOTAL Result Count = 0
RULECHECK Grid.24 ..... TOTAL Result Count = 0
RULECHECK Grid.25 ..... TOTAL Result Count = 0
RULECHECK Grid.26 ..... TOTAL Result Count = 0
```

```
--------------------------------------------------------------------------
----------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 330
TOTAL DRC RuleChecks Executed:   156
TOTAL DRC Results Generated:     0
```

LVS REPORT OF CUSTOM INVERTER FANOUT 4 :

```
 Extraction Errors and Warnings for cell "inverter_fa4.calibre.db"
------------------------------------------------------------------


WARNING:  Direct connection between different ports:
          Port names:  out2  out2

WARNING:  Open circuit - Same name on different nets:
          Name:  "out2"
          (1)  at location  (19.925,7.105)  on layer  11 "metal1"  on
net id  5
          (2)  at location  (20.575,7.1)  on layer  11 "metal1"  on net
id  6
          (3)  at location  (23.545,6.985)  on layer  11 "metal1"  on
net id  9
          (4)  at location  (23.68,7.09)  on layer  11 "metal1"  on net
id  9
          (5)  at location  (24.52,7.095)  on layer  11 "metal1"  on net
id  10
          The name was assigned to net 5 .

WARNING:  Unattached label:
          Name  "out2"  at location  (21.565,7.01)  on layer  11
"metal1"

WARNING:  Unattached label:
          Name  "out2"  at location  (22.42,7.005)  on layer  11
"metal1"

WARNING:  Unattached port pads; port ignored:
```

```
          Port name:  out2  on layer  11 "metal1"  at location
(21.565,7.01)

WARNING:  Unattached port pads; port ignored:
          Port name:  out2  on layer  11 "metal1"  at location
(22.42,7.005)
```

```
                  ################################################
                  ##                                            ##
                  ##         C A L I B R E   S Y S T E M        ##
                  ##                                            ##
                  ##             L V S   R E P O R T            ##
                  ##                                            ##
                  ################################################
```

```
REPORT FILE NAME:         inverter_fa4.lvs.report
LAYOUT NAME:              inverter_fa4.calibre.db
SOURCE NAME:              /u/soma2/cadence/LVS-
files/inverter_fa4.src.net ('inverter_fa4')
RULE FILE:                /u/soma2/cadence/LVS-files/_calibreLVS.rul_
RULE FILE TITLE:          LVS Rule File for FreePDK45
LVS MODE:                 Mask
RULE FILE NAME:           /u/soma2/cadence/LVS-files/_calibreLVS.rul_
CREATION TIME:            Mon Mar 13 22:11:50 2017
CURRENT DIRECTORY:        /u/soma2/cadence/LVS-files
USER NAME:                soma2
CALIBRE VERSION:          v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013
```

```
**************************************************************************
************************************
                              OVERALL COMPARISON RESULTS
**************************************************************************
************************************
```

```
                        #       ###################       _   _
                      #         #                 #       *   *
                    #   #       #     CORRECT     #         |
                     # #        #                 #       \___/
```

```
                    #           ###################

  Warning:  Ambiguity points were found and resolved arbitrarily.

--------------------------------------------------------------------------------
-------------------------------------

NUMBERS OF OBJECTS
------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Nets:              10        10

 Instances:          7         7         mn (4 pins)
                     7         7         mp (4 pins)
                ------    ------
 Total Inst:        14        14



********************************************************************************
************************************
                                        LVS PARAMETERS
********************************************************************************
************************************


o LVS Setup:

   LVS COMPONENT TYPE PROPERTY            element
   LVS COMPONENT SUBTYPE PROPERTY         model
   // LVS PIN NAME PROPERTY
   LVS POWER NAME                         "VDD"
   LVS GROUND NAME                        "VSS" "GROUND"
   LVS CELL SUPPLY                        NO
   LVS RECOGNIZE GATES                    ALL
   LVS IGNORE PORTS                       YES
   LVS CHECK PORT NAMES                   NO
   LVS IGNORE TRIVIAL NAMED PORTS         NO
   LVS BUILTIN DEVICE PIN SWAP            YES
   LVS ALL CAPACITOR PINS SWAPPABLE       NO
   LVS DISCARD PINS BY DEVICE             NO
   LVS SOFT SUBSTRATE PINS                NO
   LVS INJECT LOGIC                       YES
   LVS EXPAND UNBALANCED CELLS            YES
   LVS FLATTEN INSIDE CELL                NO
```

```
LVS EXPAND SEED PROMOTIONS              NO
LVS PRESERVE PARAMETERIZED CELLS        NO
LVS GLOBALS ARE PORTS                   YES
LVS REVERSE WL                          NO
LVS SPICE PREFER PINS                   NO
LVS SPICE SLASH IS SPACE                YES
LVS SPICE ALLOW FLOATING PINS           YES
// LVS SPICE ALLOW INLINE PARAMETERS
LVS SPICE ALLOW UNQUOTED STRINGS        NO
LVS SPICE CONDITIONAL LDD               NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS    NO
LVS SPICE IMPLIED MOS AREA              NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS              NO
LVS SPICE REDEFINE PARAM                NO
LVS SPICE REPLICATE DEVICES             NO
LVS SPICE SCALE X PARAMETERS            NO
LVS SPICE STRICT WL                     NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                     NO
LVS EXACT SUBTYPES                      NO
LAYOUT CASE                             NO
SOURCE CASE                             NO
LVS COMPARE CASE                        NO
LVS DOWNCASE DEVICE                     NO
LVS REPORT MAXIMUM                      50
LVS PROPERTY RESOLUTION MAXIMUM         32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                        YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction

LVS REDUCE SERIES MOS                   YES
LVS REDUCE PARALLEL MOS                 YES
LVS REDUCE SEMI SERIES MOS              YES
LVS REDUCE SPLIT GATES                  YES
LVS REDUCE PARALLEL BIPOLAR             YES
LVS REDUCE SERIES CAPACITORS            YES
LVS REDUCE PARALLEL CAPACITORS          YES
LVS REDUCE SERIES RESISTORS             YES
LVS REDUCE PARALLEL RESISTORS           YES
LVS REDUCE PARALLEL DIODES              YES
LVS REDUCTION PRIORITY                  PARALLEL
```

```
   LVS SHORT EQUIVALENT NODES              NO

   // Trace Property

   TRACE PROPERTY  mn(nmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtl)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vth)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_vtg)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  w w 4e-09 ABSOLUTE


********************************************************************************
************************************
                                  INFORMATION AND WARNINGS
********************************************************************************
************************************


                  Matched    Matched    Unmatched    Unmatched
Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    ------
---
   Nets:               10         10            0            0

   Instances:           7          7            0            0
mn(NMOS_VTL)
                        7          7            0            0
mp(PMOS_VTL)
                  -------    -------    ---------    ---------
   Total Inst:         14         14            0            0


o Statistics:
```

3 nets were matched arbitrarily.

o Isolated Layout Ports:

(Layout ports which are not connected to any net).

out2 out2

o Layout Names That Are Missing In The Source:

Nets: out2

o Initial Correspondence Points:

Nets: gnd!

o Ambiguity Resolution Points:

(Each one of the following objects belongs to a group of indistinguishable objects.
The listed objects were matched arbitrarily by the Ambiguity Resolution feature of LVS.
Arbitrary matching may be prevented by assigning names to these objects or to adjacent nets).

Layout		Source
	Nets	
10(24.345,6.610)		net05
9(23.485,6.610)		net06
8(22.315,6.610)		net07

****

SUMMARY

****

Total CPU Time: 0 sec

```
Total Elapsed Time:  0 sec
```

DRC REPORT OF CUSTOM INVERTER WITH 8 FANOUTS :

```
================================================================================
==========
=== CALIBRE::DRC-F SUMMARY REPORT
===
Execution Date/Time:       Mon Mar 13 05:11:09 2017
Calibre Version:           v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013
Rule File Pathname:        /u/soma2/cadence/DRC-files/_calibreDRC.rul_
Rule File Title:
Layout System:             GDS
Layout Path(s):            inverter_fa8.calibre.db
Layout Primary Cell:       inverter_fa8
Current Directory:         /u/soma2/cadence/DRC-files
User Name:                 soma2
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      inverter_fa8.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       inverter_fa8.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID =
NO
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:         COMMENT TEXT + RULE FILE INFORMATION
Layers:                    MEMORY-BASED
Keep Empty Checks:         YES
--------------------------------------------------------------------------
----------
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------------
----------
--- ORIGINAL LAYER STATISTICS
---
LAYER pwell ...... TOTAL Original Geometry Count = 13
LAYER nwell ...... TOTAL Original Geometry Count = 13
LAYER active ..... TOTAL Original Geometry Count = 156
LAYER poly ....... TOTAL Original Geometry Count = 98
```

```
LAYER pimplant ... TOTAL Original Geometry Count = 12
LAYER nimplant ... TOTAL Original Geometry Count = 12
LAYER vth ........ TOTAL Original Geometry Count = 0
LAYER vtg ........ TOTAL Original Geometry Count = 0
LAYER metal1 ..... TOTAL Original Geometry Count = 120
LAYER metal2 ..... TOTAL Original Geometry Count = 9
LAYER metal3 ..... TOTAL Original Geometry Count = 0
LAYER metal4 ..... TOTAL Original Geometry Count = 0
LAYER metal5 ..... TOTAL Original Geometry Count = 0
LAYER metal6 ..... TOTAL Original Geometry Count = 0
LAYER metal7 ..... TOTAL Original Geometry Count = 0
LAYER metal8 ..... TOTAL Original Geometry Count = 0
LAYER metal9 ..... TOTAL Original Geometry Count = 0
LAYER metal10 .... TOTAL Original Geometry Count = 0
LAYER contact .... TOTAL Original Geometry Count = 56
LAYER via1 ....... TOTAL Original Geometry Count = 7
LAYER via2 ....... TOTAL Original Geometry Count = 0
LAYER via3 ....... TOTAL Original Geometry Count = 0
LAYER via4 ....... TOTAL Original Geometry Count = 0
LAYER via5 ....... TOTAL Original Geometry Count = 0
LAYER via6 ....... TOTAL Original Geometry Count = 0
LAYER via7 ....... TOTAL Original Geometry Count = 0
LAYER via8 ....... TOTAL Original Geometry Count = 0
LAYER via9 ....... TOTAL Original Geometry Count = 0
--------------------------------------------------------------------------
----------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK Well.1 ...... TOTAL Result Count = 0
RULECHECK Well.2 ...... TOTAL Result Count = 0
RULECHECK Well.4 ...... TOTAL Result Count = 0
RULECHECK Poly.1 ...... TOTAL Result Count = 0
RULECHECK Poly.2 ...... TOTAL Result Count = 0
RULECHECK Poly.3 ...... TOTAL Result Count = 0
RULECHECK Poly.4 ...... TOTAL Result Count = 0
RULECHECK Poly.5 ...... TOTAL Result Count = 0
RULECHECK Poly.6 ...... TOTAL Result Count = 0
RULECHECK Active.1 .... TOTAL Result Count = 0
RULECHECK Active.2 .... TOTAL Result Count = 0
RULECHECK Active.3 .... TOTAL Result Count = 0
RULECHECK Active.4 .... TOTAL Result Count = 0
RULECHECK Implant.1 ... TOTAL Result Count = 0
RULECHECK Implant.2 ... TOTAL Result Count = 0
RULECHECK Implant.3 ... TOTAL Result Count = 0
RULECHECK Implant.4 ... TOTAL Result Count = 0
RULECHECK Implant.6 ... TOTAL Result Count = 0
RULECHECK Contact.1 ... TOTAL Result Count = 0
RULECHECK Contact.2 ... TOTAL Result Count = 0
```

```
RULECHECK Contact.3 ... TOTAL Result Count = 0
RULECHECK Contact.4 ... TOTAL Result Count = 0
RULECHECK Contact.5 ... TOTAL Result Count = 0
RULECHECK Contact.6 ... TOTAL Result Count = 0
RULECHECK Metal1.1 .... TOTAL Result Count = 0
RULECHECK Metal1.2 .... TOTAL Result Count = 0
RULECHECK Metal1.3 .... TOTAL Result Count = 0
RULECHECK Metal1.4 .... TOTAL Result Count = 0
RULECHECK Via1.1 ...... TOTAL Result Count = 0
RULECHECK Via1.2 ...... TOTAL Result Count = 0
RULECHECK Via1.3 ...... TOTAL Result Count = 0
RULECHECK Via1.4 ...... TOTAL Result Count = 0
RULECHECK Metal2.1 .... TOTAL Result Count = 0
RULECHECK Metal2.2 .... TOTAL Result Count = 0
RULECHECK Metal2.3 .... TOTAL Result Count = 0
RULECHECK Metal2.4 .... TOTAL Result Count = 0
RULECHECK Via2.1 ...... TOTAL Result Count = 0
RULECHECK Via2.2 ...... TOTAL Result Count = 0
RULECHECK Via2.3 ...... TOTAL Result Count = 0
RULECHECK Via2.4 ...... TOTAL Result Count = 0
RULECHECK Metal3.1 .... TOTAL Result Count = 0
RULECHECK Metal3.2 .... TOTAL Result Count = 0
RULECHECK Metal3.3 .... TOTAL Result Count = 0
RULECHECK Metal3.4 .... TOTAL Result Count = 0
RULECHECK Via3.1 ...... TOTAL Result Count = 0
RULECHECK Via3.2 ...... TOTAL Result Count = 0
RULECHECK Via3.3 ...... TOTAL Result Count = 0
RULECHECK Via3.4 ...... TOTAL Result Count = 0
RULECHECK Metal4.1 .... TOTAL Result Count = 0
RULECHECK Metal4.2 .... TOTAL Result Count = 0
RULECHECK Metal4.3 .... TOTAL Result Count = 0
RULECHECK Via4.1 ...... TOTAL Result Count = 0
RULECHECK Via4.2 ...... TOTAL Result Count = 0
RULECHECK Via4.3 ...... TOTAL Result Count = 0
RULECHECK Via4.4 ...... TOTAL Result Count = 0
RULECHECK Metal5.1 .... TOTAL Result Count = 0
RULECHECK Metal5.2 .... TOTAL Result Count = 0
RULECHECK Metal5.3 .... TOTAL Result Count = 0
RULECHECK Via5.1 ...... TOTAL Result Count = 0
RULECHECK Via5.2 ...... TOTAL Result Count = 0
RULECHECK Via5.3 ...... TOTAL Result Count = 0
RULECHECK Via5.4 ...... TOTAL Result Count = 0
RULECHECK Metal6.1 .... TOTAL Result Count = 0
RULECHECK Metal6.2 .... TOTAL Result Count = 0
RULECHECK Metal6.3 .... TOTAL Result Count = 0
RULECHECK Via6.1 ...... TOTAL Result Count = 0
RULECHECK Via6.2 ...... TOTAL Result Count = 0
RULECHECK Via6.3 ...... TOTAL Result Count = 0
```

```
RULECHECK Via6.4 ..... TOTAL Result Count = 0
RULECHECK Metal7.1 .... TOTAL Result Count = 0
RULECHECK Metal7.2 .... TOTAL Result Count = 0
RULECHECK Metal7.3 .... TOTAL Result Count = 0
RULECHECK Via7.1 ..... TOTAL Result Count = 0
RULECHECK Via7.2 ..... TOTAL Result Count = 0
RULECHECK Via7.3 ..... TOTAL Result Count = 0
RULECHECK Via7.4 ..... TOTAL Result Count = 0
RULECHECK Metal8.1 .... TOTAL Result Count = 0
RULECHECK Metal8.2 .... TOTAL Result Count = 0
RULECHECK Metal8.3 .... TOTAL Result Count = 0
RULECHECK Via8.1 ..... TOTAL Result Count = 0
RULECHECK Via8.2 ..... TOTAL Result Count = 0
RULECHECK Via8.3 ..... TOTAL Result Count = 0
RULECHECK Via8.4 ..... TOTAL Result Count = 0
RULECHECK Metal9.1 .... TOTAL Result Count = 0
RULECHECK Metal9.2 .... TOTAL Result Count = 0
RULECHECK Metal9.3 .... TOTAL Result Count = 0
RULECHECK Via9.1 ..... TOTAL Result Count = 0
RULECHECK Via9.2 ..... TOTAL Result Count = 0
RULECHECK Via9.3 ..... TOTAL Result Count = 0
RULECHECK Via9.4 ..... TOTAL Result Count = 0
RULECHECK Metal10.1 ... TOTAL Result Count = 0
RULECHECK Metal10.2 ... TOTAL Result Count = 0
RULECHECK Metal10.3 ... TOTAL Result Count = 0
RULECHECK Metal1.5 .... TOTAL Result Count = 0
RULECHECK Metal1.6 .... TOTAL Result Count = 0
RULECHECK Metal1.7 .... TOTAL Result Count = 0
RULECHECK Metal1.8 .... TOTAL Result Count = 0
RULECHECK Metal1.9 .... TOTAL Result Count = 0
RULECHECK Metal2.5 .... TOTAL Result Count = 0
RULECHECK Metal2.6 .... TOTAL Result Count = 0
RULECHECK Metal2.7 .... TOTAL Result Count = 0
RULECHECK Metal2.8 .... TOTAL Result Count = 0
RULECHECK Metal2.9 .... TOTAL Result Count = 0
RULECHECK Metal3.5 .... TOTAL Result Count = 0
RULECHECK Metal3.6 .... TOTAL Result Count = 0
RULECHECK Metal3.7 .... TOTAL Result Count = 0
RULECHECK Metal3.8 .... TOTAL Result Count = 0
RULECHECK Metal3.9 .... TOTAL Result Count = 0
RULECHECK Metal4.5 .... TOTAL Result Count = 0
RULECHECK Metal4.6 .... TOTAL Result Count = 0
RULECHECK Metal4.7 .... TOTAL Result Count = 0
RULECHECK Metal4.8 .... TOTAL Result Count = 0
RULECHECK Metal5.5 .... TOTAL Result Count = 0
RULECHECK Metal5.6 .... TOTAL Result Count = 0
RULECHECK Metal5.7 .... TOTAL Result Count = 0
RULECHECK Metal5.8 .... TOTAL Result Count = 0
```

```
RULECHECK Metal6.5 .... TOTAL Result Count = 0
RULECHECK Metal6.6 .... TOTAL Result Count = 0
RULECHECK Metal6.7 .... TOTAL Result Count = 0
RULECHECK Metal6.8 .... TOTAL Result Count = 0
RULECHECK Metal7.5 .... TOTAL Result Count = 0
RULECHECK Metal7.6 .... TOTAL Result Count = 0
RULECHECK Metal7.7 .... TOTAL Result Count = 0
RULECHECK Metal8.5 .... TOTAL Result Count = 0
RULECHECK Metal8.6 .... TOTAL Result Count = 0
RULECHECK Metal8.7 .... TOTAL Result Count = 0
RULECHECK Metal9.5 .... TOTAL Result Count = 0
RULECHECK Metal9.6 .... TOTAL Result Count = 0
RULECHECK Metal10.5 ... TOTAL Result Count = 0
RULECHECK Metal10.6 ... TOTAL Result Count = 0
RULECHECK Grid.1 ...... TOTAL Result Count = 0
RULECHECK Grid.2 ...... TOTAL Result Count = 0
RULECHECK Grid.3 ...... TOTAL Result Count = 0
RULECHECK Grid.4 ...... TOTAL Result Count = 0
RULECHECK Grid.5 ...... TOTAL Result Count = 0
RULECHECK Grid.6 ...... TOTAL Result Count = 0
RULECHECK Grid.7 ...... TOTAL Result Count = 0
RULECHECK Grid.8 ...... TOTAL Result Count = 0
RULECHECK Grid.9 ...... TOTAL Result Count = 0
RULECHECK Grid.10 ..... TOTAL Result Count = 0
RULECHECK Grid.11 ..... TOTAL Result Count = 0
RULECHECK Grid.12 ..... TOTAL Result Count = 0
RULECHECK Grid.13 ..... TOTAL Result Count = 0
RULECHECK Grid.14 ..... TOTAL Result Count = 0
RULECHECK Grid.15 ..... TOTAL Result Count = 0
RULECHECK Grid.16 ..... TOTAL Result Count = 0
RULECHECK Grid.17 ..... TOTAL Result Count = 0
RULECHECK Grid.18 ..... TOTAL Result Count = 0
RULECHECK Grid.19 ..... TOTAL Result Count = 0
RULECHECK Grid.20 ..... TOTAL Result Count = 0
RULECHECK Grid.21 ..... TOTAL Result Count = 0
RULECHECK Grid.22 ..... TOTAL Result Count = 0
RULECHECK Grid.23 ..... TOTAL Result Count = 0
RULECHECK Grid.24 ..... TOTAL Result Count = 0
RULECHECK Grid.25 ..... TOTAL Result Count = 0
RULECHECK Grid.26 ..... TOTAL Result Count = 0
--------------------------------------------------------------------------
----------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 496
TOTAL DRC RuleChecks Executed:   156
```

```
TOTAL DRC Results Generated:     0
```

LVS REPORT OF CUSTOM INVERTER WITH 8 FANOUTS :

```
 Extraction Errors and Warnings for cell "inverter_fa8.calibre.db"
------------------------------------------------------------------


WARNING:  Open circuit - Same name on different nets:
          Name:  "out2"
          (1)  at location  (19.93,7.1)  on layer  11 "metal1"  on net
id  5
          (2)  at location  (20.54,7.11)  on layer  11 "metal1"  on net
id  6
          (3)  at location  (21.65,7.1)  on layer  11 "metal1"  on net
id  7
          (4)  at location  (22.49,7.095)  on layer  11 "metal1"  on net
id  8
          (5)  at location  (24.205,7.1)  on layer  11 "metal1"  on net
id  10
          (6)  at location  (25.045,7.095)  on layer  11 "metal1"  on
net id  11
          (7)  at location  (26.045,7.095)  on layer  11 "metal1"  on
net id  12
          (8)  at location  (27.16,7.095)  on layer  11 "metal1"  on net
id  13
          (9)  at location  (27.97,7.095)  on layer  11 "metal1"  on net
id  14
          The name was assigned to net 5 .
```

```
                ################################################
                ##                                            ##
                ##        C A L I B R E   S Y S T E M         ##
                ##                                            ##
```

```
                  ##            L V S   R E P O R T             ##
                  ##                                            ##
                  ################################################


REPORT FILE NAME:         inverter_fa8.lvs.report
LAYOUT NAME:              inverter_fa8.calibre.db
SOURCE NAME:              /u/soma2/cadence/LVS-
files/inverter_fa8.src.net ('inverter_fa8')
RULE FILE:                /u/soma2/cadence/LVS-files/_calibreLVS.rul_
RULE FILE TITLE:          LVS Rule File for FreePDK45
LVS MODE:                 Mask
RULE FILE NAME:           /u/soma2/cadence/LVS-files/_calibreLVS.rul_
CREATION TIME:            Mon Mar 13 22:15:57 2017
CURRENT DIRECTORY:        /u/soma2/cadence/LVS-files
USER NAME:                soma2
CALIBRE VERSION:          v2013.2_35.25    Wed Jul 3 15:43:57 PDT 2013

**************************************************************************
************************************
                              OVERALL COMPARISON RESULTS
**************************************************************************
************************************

                        #       ###################       _   _
                       #        #                 #       *   *
                    #   #       #     CORRECT     #         |
                     # #        #                 #       \___/
                      #         ###################

  Warning:  Ambiguity points were found and resolved arbitrarily.

--------------------------------------------------------------------------
---------------------------------------

NUMBERS OF OBJECTS
------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Nets:              14        14

 Instances:         11        11         mn (4 pins)
                    11        11         mp (4 pins)
```

```
                ------    ------
 Total Inst:        22        22


********************************************************************************
************************************
                                        LVS PARAMETERS
********************************************************************************
************************************


o LVS Setup:

   LVS COMPONENT TYPE PROPERTY            element
   LVS COMPONENT SUBTYPE PROPERTY         model
   // LVS PIN NAME PROPERTY
   LVS POWER NAME                         "VDD"
   LVS GROUND NAME                        "VSS" "GROUND"
   LVS CELL SUPPLY                        NO
   LVS RECOGNIZE GATES                    ALL
   LVS IGNORE PORTS                       YES
   LVS CHECK PORT NAMES                   NO
   LVS IGNORE TRIVIAL NAMED PORTS         NO
   LVS BUILTIN DEVICE PIN SWAP            YES
   LVS ALL CAPACITOR PINS SWAPPABLE       NO
   LVS DISCARD PINS BY DEVICE             NO
   LVS SOFT SUBSTRATE PINS                NO
   LVS INJECT LOGIC                       YES
   LVS EXPAND UNBALANCED CELLS            YES
   LVS FLATTEN INSIDE CELL                NO
   LVS EXPAND SEED PROMOTIONS             NO
   LVS PRESERVE PARAMETERIZED CELLS       NO
   LVS GLOBALS ARE PORTS                  YES
   LVS REVERSE WL                         NO
   LVS SPICE PREFER PINS                  NO
   LVS SPICE SLASH IS SPACE               YES
   LVS SPICE ALLOW FLOATING PINS          YES
   // LVS SPICE ALLOW INLINE PARAMETERS
   LVS SPICE ALLOW UNQUOTED STRINGS       NO
   LVS SPICE CONDITIONAL LDD              NO
   LVS SPICE CULL PRIMITIVE SUBCIRCUITS   NO
   LVS SPICE IMPLIED MOS AREA             NO
   // LVS SPICE MULTIPLIER NAME
   LVS SPICE OVERRIDE GLOBALS             NO
   LVS SPICE REDEFINE PARAM               NO
   LVS SPICE REPLICATE DEVICES            NO
   LVS SPICE SCALE X PARAMETERS           NO
```

```
LVS SPICE STRICT WL                     NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                     NO
LVS EXACT SUBTYPES                      NO
LAYOUT CASE                             NO
SOURCE CASE                             NO
LVS COMPARE CASE                        NO
LVS DOWNCASE DEVICE                     NO
LVS REPORT MAXIMUM                      50
LVS PROPERTY RESOLUTION MAXIMUM         32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                        YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction

LVS REDUCE SERIES MOS                   YES
LVS REDUCE PARALLEL MOS                 YES
LVS REDUCE SEMI SERIES MOS              YES
LVS REDUCE SPLIT GATES                  YES
LVS REDUCE PARALLEL BIPOLAR             YES
LVS REDUCE SERIES CAPACITORS            YES
LVS REDUCE PARALLEL CAPACITORS          YES
LVS REDUCE SERIES RESISTORS             YES
LVS REDUCE PARALLEL RESISTORS           YES
LVS REDUCE PARALLEL DIODES              YES
LVS REDUCTION PRIORITY                  PARALLEL

LVS SHORT EQUIVALENT NODES              NO

// Trace Property

TRACE PROPERTY  mn(nmos_vtl)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtl)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtl)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtl)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vth)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vth)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vth)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vth)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtg)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mn(nmos_vtg)  w w 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtg)  l l 4e-09 ABSOLUTE
TRACE PROPERTY  mp(pmos_vtg)  w w 4e-09 ABSOLUTE
```

```
   TRACE PROPERTY  mn(nmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mn(nmos_thkox)  w w 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  l l 4e-09 ABSOLUTE
   TRACE PROPERTY  mp(pmos_thkox)  w w 4e-09 ABSOLUTE


********************************************************************************
************************************
                                  INFORMATION AND WARNINGS
********************************************************************************
************************************


                   Matched    Matched    Unmatched    Unmatched
Component
                    Layout     Source       Layout       Source    Type
                   -------    -------    ---------    ---------    ------
---
   Nets:                14         14            0            0

   Instances:           11         11            0            0
mn(NMOS_VTL)
                        11         11            0            0
mp(PMOS_VTL)
                   -------    -------    ---------    ---------
   Total Inst:          22         22            0            0


o Statistics:

   7 nets were matched arbitrarily.


o Layout Names That Are Missing In The Source:

   Nets:         out2 Y


o Initial Correspondence Points:

   Nets:         in vdd!


o Ambiguity Resolution Points:

      (Each one of the following objects belongs to a group of
indistinguishable objects.
```

The listed objects were matched arbitrarily by the Ambiguity Resolution feature of LVS.

Arbitrary matching may be prevented by assigning names to these objects or to adjacent nets).

Layout	Source
Nets	
14(27.795,6.610)	net13
13(26.985,6.610)	net12
12(25.870,6.610)	net11
11(24.870,6.610)	net10
10(24.010,6.610)	net9
9(23.360,6.610)	net8
8(22.315,6.610)	net7

****
****
SUMMARY
****
****

Total CPU Time: 0 sec
Total Elapsed Time: 0 sec