



PRELIMINARY

DATA

SHEET

MAY, 1976

MCS6500 MICROPROCESSORS

The MCS6500 Microprocessor Family Concept ----

The MCS6500 Series Microprocessors represent the first totally software compatible microprocessor family. This family of products includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. All of the microprocessors in the MCS6500 group are software compatible within the group and are bus compatible with the M6800 product offering.

The family includes five microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for the multi processor system applications where maximum timing control is mandatory. All versions of the microprocessors are available in 1 MHz and 2 MHz ("A" suffix on product numbers) maximum operating frequencies.

Features of the MCS6500 Family

- . Single five volt supply
- . N channel, silicon gate, depletion load technology
- . Eight bit parallel processing
- . 56 Instructions
- . Decimal and binary arithmetic
- . Thirteen addressing modes
- . True indexing capability
- . Programmable stack pointer
- . Variable length stack
- . Interrupt capability
- . Non-maskable interrupt
- . Use with any type or speed memory
- . Bi-directional Data Bus
- . Instruction decoding and control
- . Addressable memory range of up to 65K bytes
- . "Ready" input
- . Direct memory access capability
- . Bus compatible with MC6800
- . Choice of external or on-board clocks
- . 1MHz and 2MHz operation
- . On-the-chip clock options
 - * External single clock input
 - * RC time base input
 - * Crystal time base input
- . 40 and 28 pin package versions
- . Pipeline architecture

Members of the Family

Microprocessors with On-Board Clock Oscillator

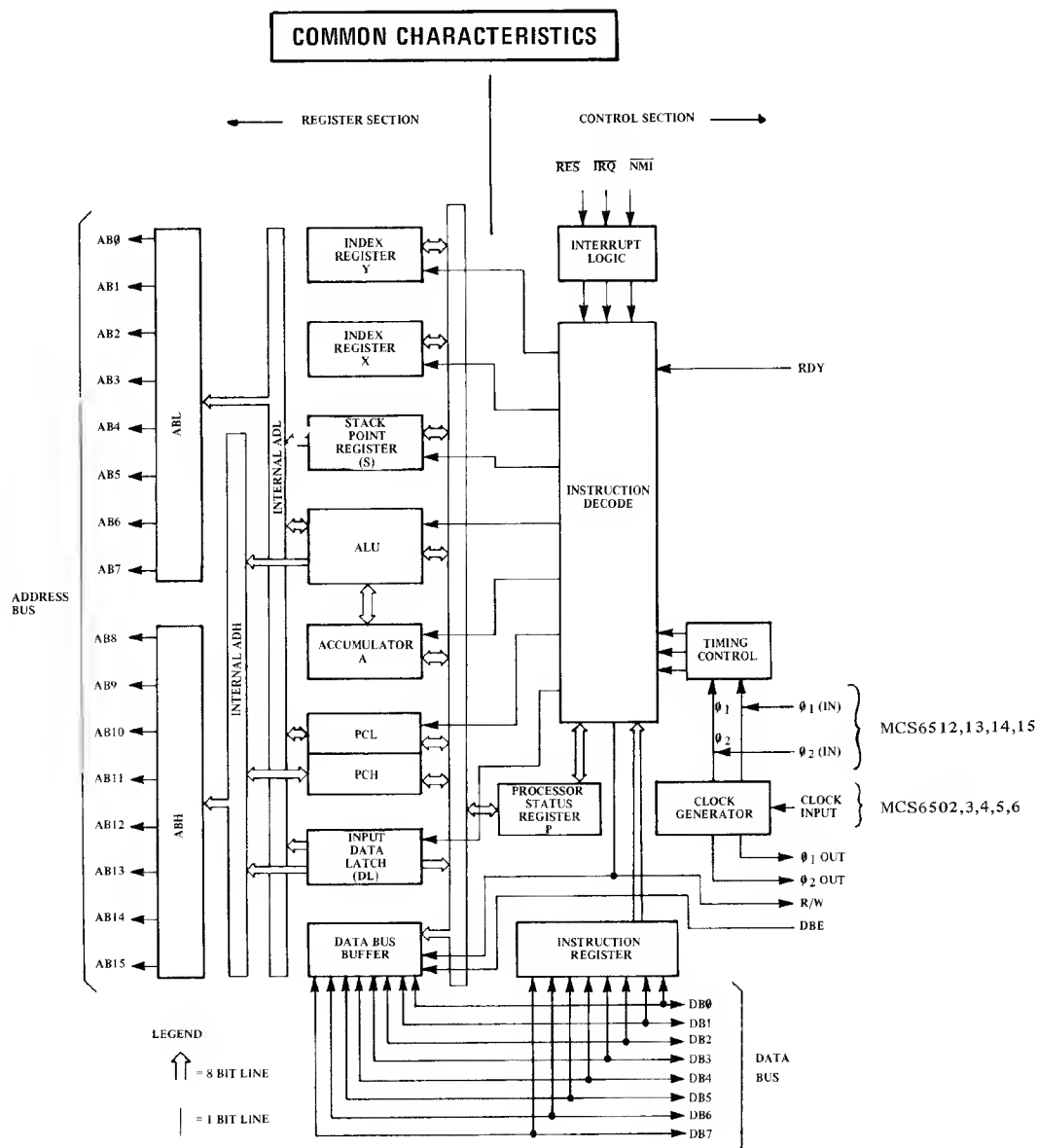
- MCS6502
- MCS6503
- MCS6504
- MCS6505
- MCS6506

Microprocessors with External Two Phase Clock Input

- MCS6512
- MCS6513
- MCS6514
- MCS6515

Comments on the Data Sheet

The data sheet is constructed to review first the basic "Common Characteristics" - those features which are common to the general family of microprocessors. Subsequent to a review of the family characteristics will be sections devoted to each member of the group with specific features of each.



- Note: 1. Clock Generator is not included on MCS6512,13,14,15
 2. Addressing Capability and control options vary with each of the MCS6500 Products.

MCS6500 Internal Architecture

COMMON CHARACTERISTICS

MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	V _{CC}	-0.3 to +7.0	Vdc
INPUT VOLTAGE	V _{IN}	-0.3 to +7.0	Vdc
OPERATING TEMPERATURE	T _A	0 to +70	°C
STORAGE TEMPERATURE	T _{STG}	-55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

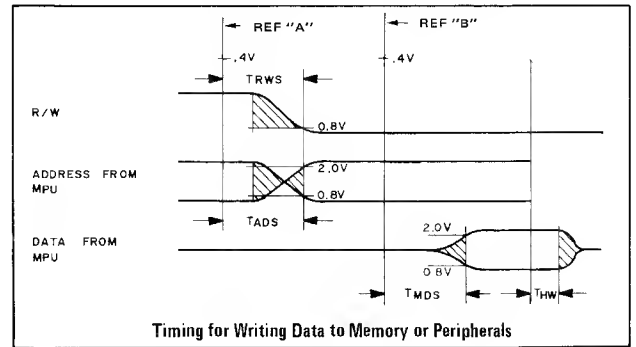
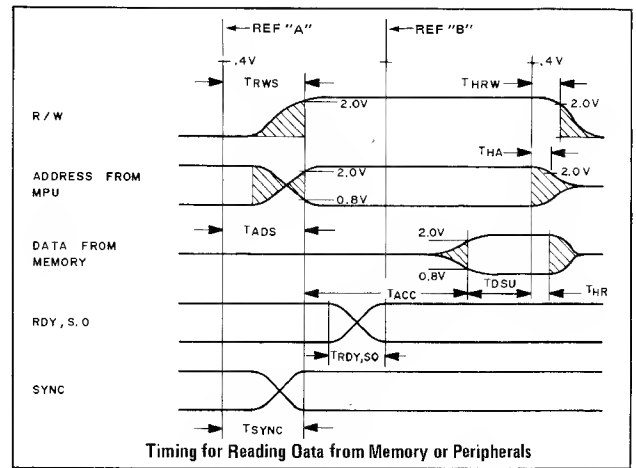
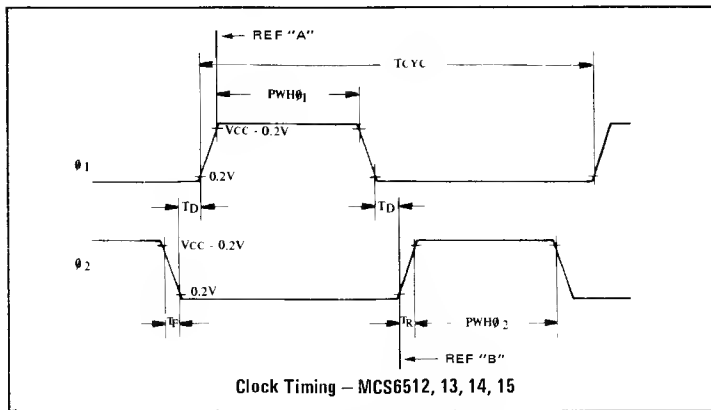
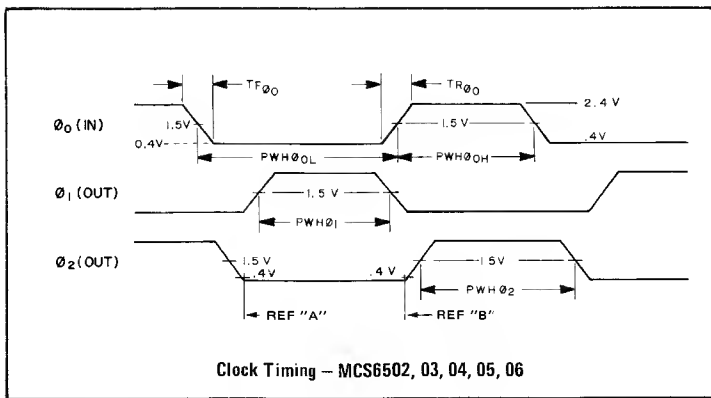
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 25° C)

Ø₁, Ø₂ applies to MCS6512, 13, 14, 15, Ø₀ (in) applies to MCS6502, 03, 04, 05 and 06

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage Logic, Ø ₀ (in) Ø ₁ , Ø ₂	V _{IH}	V _{SS} + 2.4 V _{CC} - 0.2	- -	V _{CC} V _{CC} + 0.25	Vdc
Input Low Voltage Logic, Ø ₀ (in) Ø ₁ , Ø ₂	V _{IL}	V _{SS} - 0.3 V _{SS} - 0.3	- -	V _{SS} + 0.4 V _{SS} + 0.2	Vdc
Input High Threshold Voltage RES, NMI, RDY, IRQ, Data, S.O.	V _{IHT}	V _{SS} + 2.0	-	-	Vdc
Input Low Threshold Voltage RES, NMI, RDY, IRQ, Data, S.O.	V _{ILT}	-	-	V _{SS} + 0.8	Vdc
Input Leakage Current (V _{in} = 0 to 5.25V, V _{CC} = 0) Logic (Excl. RDY, S.O.) Ø ₁ , Ø ₂ Ø ₀ (in)	I _{in}	- - -	- - -	2.5 100 10.0	µA µA µA
Three-State (Off State) Input Current (V _{in} = 0.4 to 2.4V, V _{CC} = 5.25V) Data Lines	I _{TSI}	-	-	10	µA
Output High Voltage (I _{LOAD} = -100µAdc, V _{CC} = 4.75V) SYNC, Data, A0-A15, R/W	V _{OH}	V _{SS} + 2.4	-	-	Vdc
Output Low Voltage (I _{LOAD} = 1.6mAdc, V _{CC} = 4.75V) SYNC, Data, A0-A15, R/W	V _{OL}	-	-	V _{SS} + 0.4	Vdc
Power Dissipation	P _D	-	.25	.70	W
Capacitance (V _{in} = 0, T _A = 25° C, f = 1MHz) Logic Data A0-A15, R/W, SYNC Ø ₀ (in) Ø ₁ Ø ₂	C C _{in} C _{out} C _{Ø₀(in)} C _{Ø₁} C _{Ø₂}	- - - - - -	- - - - 30 50	10 15 12 15 50 80	pF

Note: IRQ and NMI require 3K pull-up resistors.

COMMON CHARACTERISTICS



Note: "REF." means Reference Points on clocks.

COMMON CHARACTERISTICS

INSTRUCTION SET – ALPHABETIC SEQUENCE

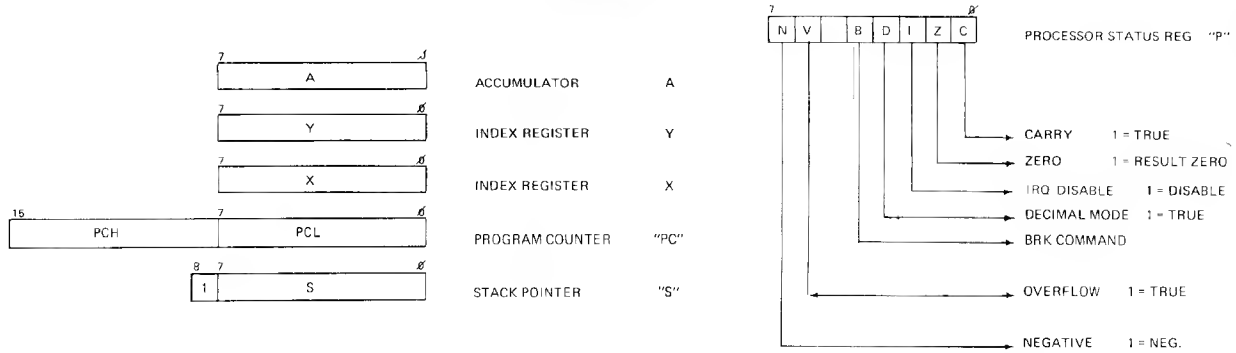
ADC Add Memory to Accumulator with Carry	DEC Decrement Memory by One	PHA Push Accumulator on Stack
AND "AND" Memory with Accumulator	DEX Decrement Index X by One	PHP Push Processor Status on Stack
ASL Shift left One Bit (Memory or Accumulator)	DEY Decrement Index Y by One	PLA Pull Accumulator from Stack
		PLP Pull Processor Status from Stack
BCC Branch on Carry Clear	EOR "Exclusive-or" Memory with Accumulator	ROL Rotate One Bit Left (Memory or Accumulator)
BCS Branch on Carry Set		ROR Rotate One Bit Right (Memory or Accumulator)
BEQ Branch on Result Zero	INC Increment Memory by One	RTI Return from Interrupt
BIT Test Bits in Memory with Accumulator	INX Increment Index X by One	RTS Return from Subroutine
BMI Branch on Result Minus	INY Increment Index Y by One	
BNE Branch on Result not Zero		
BPL Branch on Result Plus	JMP Jump to New Location	SBC Subtract Memory from Accumulator with Borrow
BRK Force Break	JSR Jump to New Location Saving Return Address	SEC Set Carry Flag
BVC Branch on Overflow Clear		SED Set Decimal Mode
BVS Branch on Overflow Set	LDA Load Accumulator with Memory	SEI Set Interrupt Disable Status
	LDX Load Index X with Memory	STA Store Accumulator in Memory
CLC Clear Carry Flag	LDY Load Index Y with Memory	STX Store Index X in Memory
CLD Clear Decimal Mode	LSR Shift One Bit Right (Memory or Accumulator)	STY Store Index Y in Memory
CLI Clear Interrupt Disable Bit		
CLV Clear Overflow Flag	NOP No Operation	IAX Transfer Accumulator to Index X
CMP Compare Memory and Accumulator	ORA "OR" Memory with Accumulator	IAY Transfer Accumulator to Index Y
CPX Compare Memory and Index X		TSX Transfer Stack Pointer to Index X
CPY Compare Memory and Index Y		TXA Transfer Index X to Accumulator
		TXS Transfer Index X to Stack Pointer
		TYA Transfer Index Y to Accumulator

ADDRESSING MODES

- ACCUMULATOR ADDRESSING - This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.
- IMMEDIATE ADDRESSING - In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.
- ABSOLUTE ADDRESSING - In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.
- ZERO PAGE ADDRESSING - The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.
- INDEXED ZERO PAGE ADDRESSING - (X, Y indexing) - This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.
- INDEXED ABSOLUTE ADDRESSING - (X, Y indexing) - This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.
- IMPLIED ADDRESSING - In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.
- RELATIVE ADDRESSING - Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.
 The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.
- INDEXED INDIRECT ADDRESSING - In indexed indirect addressing (referred to as (Indirect,X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.
- INDIRECT INDEXED ADDRESSING - In indirect indexed addressing (referred to as (Indirect),Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.
- ABSOLUTE INDIRECT - The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

COMMON CHARACTERISTICS

PROGRAMMING MODEL



INSTRUCTION SET — OP CODES, Execution Time, Memory Requirements

INSTRUCTIONS	IMMEDIATE	ABSOLUTE	ZERO PAGE	ACCUM.	IMPLIED	(IND) X	(IND) Y	Z PAGE X	ABS X	ABS Y	RELATIVE	INDIRECT	Z PAGE Y	CONDITION CODES
MEMORIC	OPERATION	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	N P C I D V
ADC	A ← M ← A	(4) 11	69 2 2	6D 4 3	65 3 2									✓ ✓ ✓ ✓ ✓
AND	A ← M ← A	(1) 29	2 2	2D 4 3	25 3 2									✓ ✓ ✓ ✓ ✓
ASL	← A ← 2A			0E 6 3	06 5 2	0A 2 1								✓ ✓ ✓ ✓ ✓
BCC	BRANCH ON C=0	(2) 12												✓ ✓ ✓ ✓ ✓
BCS	BRANCH ON C=1	(2) 13												✓ ✓ ✓ ✓ ✓
BEQ	BRANCH ON Z=1	(2) 14												✓ ✓ ✓ ✓ ✓
BIT	A ← M			2C 4 3	24 3 2									M ₁ ✓ ✓ ✓ ✓ M ₆
BMI	BRANCH ON N=1	(2) 15												✓ ✓ ✓ ✓ ✓
BNE	BRANCH ON Z=0	(2) 16												✓ ✓ ✓ ✓ ✓
BPL	BRANCH ON N=0	(2) 17												✓ ✓ ✓ ✓ ✓
BRK	(See Fig. 1)													✓ ✓ ✓ ✓ ✓
BVC	BRANCH ON V=0	(2) 18												✓ ✓ ✓ ✓ ✓
BVS	BRANCH ON V=1	(2) 19												✓ ✓ ✓ ✓ ✓
CLC	← C													✓ ✓ ✓ ✓ ✓
CLD	← D													✓ ✓ ✓ ✓ ✓
CLI	← I													✓ ✓ ✓ ✓ ✓
CLV	← V													✓ ✓ ✓ ✓ ✓
CMP	A ← M	(1) 20	2 2	CD 4 3	CD 3 2									✓ ✓ ✓ ✓ ✓
CPX	X ← M	(2) 21	2 2	ED 4 3	ED 3 2									✓ ✓ ✓ ✓ ✓
CPY	Y ← M	(2) 22	2 2	FD 4 3	FD 3 2									✓ ✓ ✓ ✓ ✓
DEC	M ← M - 1			CE 6 3	CE 5 2									✓ ✓ ✓ ✓ ✓
DEX	X ← X - 1													✓ ✓ ✓ ✓ ✓
DEY	Y ← Y - 1													✓ ✓ ✓ ✓ ✓
EOR	A ← M ← A	(1) 23	2 2	AD 4 3	AD 3 2									✓ ✓ ✓ ✓ ✓
INC	M ← M + 1			EE 6 3	EE 5 2									✓ ✓ ✓ ✓ ✓
INX	X ← X + 1													✓ ✓ ✓ ✓ ✓
INY	Y ← Y + 1													✓ ✓ ✓ ✓ ✓
JMP	JUMP TO NEW LOC			4C 3 3										✓ ✓ ✓ ✓ ✓
JSR	(See Fig. 2) JUMP SUB			20 6 3										✓ ✓ ✓ ✓ ✓
LDA	M ← A	(1) 24	2 2	AD 4 3	AD 3 2									✓ ✓ ✓ ✓ ✓
LDX	M ← X	(1) 25	2 2	AE 4 3	AE 3 2									✓ ✓ ✓ ✓ ✓
LDY	M ← Y	(1) 26	2 2	AF 4 3	AF 3 2									✓ ✓ ✓ ✓ ✓
LSR	← A ← 2A			4E 6 3	46 5 2	4A 2 1								✓ ✓ ✓ ✓ ✓
NOP	NO OPERATION													✓ ✓ ✓ ✓ ✓
ORA	A ← M ← A	(1) 27	2 2	AD 4 3	AD 3 2									✓ ✓ ✓ ✓ ✓
PHA	A ← M ₁ S ← S													✓ ✓ ✓ ✓ ✓
PHP	P ← M ₁ S ← S													✓ ✓ ✓ ✓ ✓
PLA	S ← S M ₁ ← A													✓ ✓ ✓ ✓ ✓
PLP	S ← S M ₁ ← P													✓ ✓ ✓ ✓ ✓
ROL	← A ← 2A			2E 6 3	26 5 2	2A 2 1								✓ ✓ ✓ ✓ ✓
ROR	← A ← 2A			2E 6 3	26 5 2	2A 2 1								✓ ✓ ✓ ✓ ✓
RTI	(See Fig. 1) RETURN INT													✓ ✓ ✓ ✓ ✓
RTS	(See Fig. 2) RETURN SUB													✓ ✓ ✓ ✓ ✓
SBC	A ← M ← A	(1) 28	2 2	ED 4 3	ED 3 2									✓ ✓ ✓ ✓ ✓
SEC	← C													✓ ✓ ✓ ✓ ✓
SED	← D													✓ ✓ ✓ ✓ ✓
SET	← I													✓ ✓ ✓ ✓ ✓
STA	A ← M			8D 4 3	85 3 2									✓ ✓ ✓ ✓ ✓
STX	X ← M			8E 4 3	86 3 2									✓ ✓ ✓ ✓ ✓
STY	Y ← M			8C 4 3	84 3 2									✓ ✓ ✓ ✓ ✓
TAX	A ← X													✓ ✓ ✓ ✓ ✓
TAY	A ← Y													✓ ✓ ✓ ✓ ✓
TSX	X ← X													✓ ✓ ✓ ✓ ✓
TXA	X ← A													✓ ✓ ✓ ✓ ✓
TXS	X ← S													✓ ✓ ✓ ✓ ✓
TYA	Y ← A													✓ ✓ ✓ ✓ ✓

- (1) ADD 1 TO "N" IF PAGE BOUNDARY IS CROSSED
 (2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
 (3) CARRY NOT = BORROW
 (4) IF IN DECIMAL MODE Z FLAG IS INVALID
 ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT
- X INDEX X
 Y INDEX Y
 A ACCUMULATOR
 M MEMORY PER EFFECTIVE ADDRESS
 M₁ MEMORY PER STACK POINTER
- ← ADD
 ← SUBTRACT
 AND
 OR
- EXCLUSIVE OR
 MODIFIED
 NOT MODIFIED
 MEMORY BIT 7
 MEMORY BIT 6
- N NO CYCLES
 # NO BYTES

1 MHz TIMING

Clock Timing - MCS6512, 13, 14, 15

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Cycle Time	T_{CYC}	1000	---	---	nsec
Clock Pulse Width (Measured at $V_{CC} - 0.2V$)	$PWH_{\phi 1}$ $PWH_{\phi 2}$	430 470	---	---	nsec
Fall Time (Measured from 0.2V to $V_{CC} - 0.2V$)	T_F	---	---	25	nsec
Delay Time between Clocks (Measured at 0.2V)	T_D	0	---	---	nsec

CLOCK TIMING - MCS6502, 03, 04, 05, 06

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Cycle Time	T_{CYC}	1000	--	--	ns
$\phi_o(IN)$ Pulse Width (measured at 1.5V)	PWH_{ϕ_o}	460	--	520	ns
$\phi_o(IN)$ Rise, Fall Time	TR_{ϕ_o}, TF_{ϕ_o}	--	--	10	ns
Delay Time Between Clocks (measured at 1.5V)	T_D	5	--	--	ns
$\phi_1(OUT)$ Pulse Width (measured at 1.5V)	PWH_{ϕ_1}	$PWH_{\phi_{oL}} - 20$	--	$PWH_{\phi_{oL}}$	ns
$\phi_2(OUT)$ Pulse Width (measured at 1.5V)	PWH_{ϕ_2}	$PWH_{\phi_{oH}} - 40$	--	$PWH_{\phi_{oH}} - 10$	ns
$\phi_1(OUT), \phi_2(OUT)$ Rise, Fall Time (Load = 30pf (measured .8V to 2.0 V) + 1 TTL)	T_R, T_F	--	--	25	ns

READ/WRITE TIMING

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Read/Write Setup Time from MCS6500	T_{RWS}	--	100	300	ns
Address Setup Time from MCS6500	T_{ADS}	--	100	300	ns
Memory Read Access Time	T_{ACC}	--	--	575	ns
Data Stability Time Period	T_{DSU}	100	--	--	ns
Data Hold Time - Read	T_{HR}	10	--	--	ns
Data Hold Time - Write	T_{HW}	30	60	--	ns
Data Setup Time from MCS6500	T_{MDS}	--	150	200	ns
RDY, S.O. Setup Time	T_{RDY}	100	--	--	ns
SYNC Setup Time from MCS6500	T_{SYNC}	--	--	350	ns
Address Hold Time	T_{HA}	30	60	--	ns
R/W Hold Time	T_{HRW}	30	60	--	ns

2 MHz TIMING

Clock Timing - MCS6512, 13, 14, 15, 16

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Cycle Time	T_{CYC}	500	---	---	nsec
Clock Pulse Width (Measured at $V_{CC} - 0.2V$)	$PWH_{\phi 1}$ $PWH_{\phi 2}$	215 255	---	---	nsec
Fall Time (Measured from 0.2V to $V_{CC} - 0.2V$)	T_F	---	---	12	nsec
Delay Time between Clocks (Measured at 0.2V)	T_D	0	---	---	nsec

CLOCK TIMING - MCS6502, 03, 04, 05, 06

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Cycle Time	T_{CYC}	500	--	--	ns
$\phi_o(IN)$ Pulse Width (measured at 1.5V)	PWH_{ϕ_o}	240	--	260	ns
$\phi_o(IN)$ Rise, Fall Time	TR_{ϕ_o}, TF_{ϕ_o}	--	--	10	ns
Delay Time Between Clocks (measured at 1.5V)	T_D	5	--	--	ns
$\phi_1(OUT)$ Pulse Width (measured at 1.5V)	PWH_{ϕ_1}	$PWH_{\phi_{oL}} - 20$	--	$PWH_{\phi_{oL}}$	ns
$\phi_2(OUT)$ Pulse Width (measured at 1.5V)	PWH_{ϕ_2}	$PWH_{\phi_{oH}} - 40$	--	$PWH_{\phi_{oH}} - 10$	ns
$\phi_1(OUT), \phi_2(OUT)$ Rise, Fall Time (Load = 30pf (measured .8V to 2.0 V) + 1 TTL)	T_R, T_F	--	--	25	ns

READ/WRITE TIMING

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Read/Write Setup Time from MCS6500A	T_{RWS}	--	100	150	ns
Address Setup Time from MCS6500A	T_{ADS}	--	100	150	ns
Memory Read Access Time	T_{ACC}	--	--	300	ns
Data Stability Time Period	T_{DSU}	50	--	--	ns
Data Hold Time - Read	T_{HR}	10	--	--	ns
Data Hold Time - Write	T_{HW}	30	60	--	ns
Data Setup Time from MCS6500A	T_{MDS}	--	75	100	ns
RDY, S.O. Setup Time	T_{RDY}	50	--	--	ns
SYNC Setup Time from MCS6500A	T_{SYNC}	--	--	175	ns
Address Hold Time	T_{HA}	30	60	--	ns
R/W Hold Time	T_{HRW}	30	60	--	ns

COMMON CHARACTERISTICS

Clocks (ϕ_1, ϕ_2)

The MCS651X requires a two phase non-overlapping clock that runs at the Vcc voltage level.

The MCS650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled. Details of this feature are discussed in the MCS6502 portion of this data sheet.

Address Bus (A_0 - A_{15}) (See sections on each micro for respective address lines on those devices.)

These outputs are TTL compatible, capable of driving one standard TTL load and 130pf.

Data Bus (D_0 - D_7)

Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130pf.

Data Bus Enable (DBE)

This TTL compatible input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two (ϕ_2) clock, thus allowing data output from microprocessor only during ϕ_2 . During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

Ready (RDY)

This input signal allows the user to single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one (ϕ_1) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two (ϕ_2) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If Ready is low during a write cycle, it is ignored until the following read operation.

Interrupt Request (IRQ)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K Ω external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt (NMI)

A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

NMI is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for IRQ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

NMI also requires an external 3K Ω resistor to Vcc for proper wire-OR operations.

Inputs IRQ and NMI are hardware interrupts lines that are sampled during ϕ_2 (phase 2) and will begin the appropriate interrupt routine on the ϕ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)

A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of ϕ_1 .

SYNC

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ_1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After Vcc reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (SYNC) signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

MCS6502 – 40 Pin Package

V _{ss}	1	40	RES
RDY	2	39	$\overline{\text{O}}_2(\text{OUT})$
$\overline{\text{O}}_1(\text{OUT})$	3	38	S/O
$\overline{\text{I}}\overline{\text{R}}\overline{\text{Q}}$	4	37	$\overline{\text{O}}_0(\text{IN})$
N.C.	5	36	N.C.
NMI	6	35	N.C.
SYNC	7	34	R/W
V _{cc}	8	33	OB0
AB0	9	32	OB1
AB1	10	31	OB2
AB2	11	30	OB3
AB3	12	29	OB4
AB4	13	28	DB5
AB5	14	27	DB6
AB6	15	26	OB7
AB7	16	25	AB15
AB8	17	24	AB14
AB9	18	23	AB13
AB10	19	22	AB12
AB11	20	21	V _{ss}

MCS6502

- * 65K Addressable Bytes of Memory
- * $\overline{\text{I}}\overline{\text{R}}\overline{\text{Q}}$ Interrupt * $\overline{\text{N}}\overline{\text{M}}\overline{\text{I}}$ Interrupt
- * On-the-chip Clock
 - ✓ TTL Level Single Phase Input
 - ✓ RC Time Base Input
 - ✓ Crystal Time Base Input
- * SYNC Signal
(can be used for single instruction execution)
- * RDY Signal
(can be used for single cycle execution)
- * Two Phase Output Clock for Timing of Support Chips

Features of MCS6502

MCS6503 – 28 Pin Package

RES	1	28	$\overline{\text{O}}_2(\text{OUT})$
V _{ss}	2	27	$\overline{\text{O}}_0(\text{IN})$
$\overline{\text{I}}\overline{\text{R}}\overline{\text{Q}}$	3	26	R/W
NMI	4	25	DB0
V _{cc}	5	24	DB1
AB0	6	23	DB2
AB1	7	22	DB3
AB2	8	21	DB4
AB3	9	20	DB5
AB4	10	19	DB6
AB5	11	18	DB7
AB6	12	17	AB11
AB7	13	16	AB10
AB8	14	15	AB9

MCS6503

- * 4K Addressable Bytes of Memory (AB00-AB11)
- * On-the-chip Clock
- * $\overline{\text{I}}\overline{\text{R}}\overline{\text{Q}}$ Interrupt
- * $\overline{\text{N}}\overline{\text{M}}\overline{\text{I}}$ Interrupt
- * 8 Bit Bi-Directional Data Bus

Features of MCS6503

MCS6504 – 28 Pin Package

RES	1	28	$\overline{\text{O}}_2(\text{OUT})$
V _{ss}	2	27	$\overline{\text{O}}_0(\text{IN})$
$\overline{\text{I}}\overline{\text{R}}\overline{\text{Q}}$	3	26	R/W
V _{cc}	4	25	DB0
AB0	5	24	DB1
AB1	6	23	DB2
AB2	7	22	DB3
AB3	8	21	DB4
AB4	9	20	DB5
AB5	10	19	DB6
AB6	11	18	DB7
AB7	12	17	AB12
AB8	13	16	AB11
AB9	14	15	AB10

MCS6504

- * 8K Addressable Bytes of Memory (AB00-AB12)
- * On-the-chip Clock
- * $\overline{\text{I}}\overline{\text{R}}\overline{\text{Q}}$ Interrupt
- * 8 Bit Bi-Directional Data Bus

Features of MCS6504

MCS6505 – 28 Pin Package

RES	1	28	ϕ_2 (OUT)
Vss	2	27	ϕ_0 (IN)
RDY	3	26	R/W
IRQ	4	25	DB0
Vcc	5	24	DB1
AB0	6	23	DB2
AB1	7	22	DB3
AB2	8	21	DB4
AB3	9	20	DB5
AB4	10	19	DB6
AB5	11	18	DB7
AB6	12	17	AB11
AB7	13	16	AB10
AB8	14	15	AB9

MCS6505

- * 4K Addressable Bytes of Memory (AB00-AB11)
- * On-the-chip Clock
- * $\overline{\text{IRQ}}$ Interrupt
- * RDY Signal
- * 8 Bit Bi-Directional Data Bus

Features of MCS6505

MCS6506 – 28 Pin Package

RES	1	28	ϕ_2 (OUT)
Vss	2	27	ϕ_0 (IN)
ϕ_1 (OUT)	3	26	R/W
IRQ	4	25	DB0
Vcc	5	24	DB1
AB0	6	23	DB2
AB1	7	22	DB3
AB2	8	21	DB4
AB3	9	20	DB5
AB4	10	19	DB6
AB5	11	18	DB7
AB6	12	17	AB11
AB7	13	16	AB10
AB8	14	15	AB9

MCS6506

- * 4K Addressable Bytes of Memory (AB00-AB11)
- * On-the-chip Clock
- * $\overline{\text{IRQ}}$ Interrupt
- * Two phases off
- * 8 Bit Bi-Directional Data Bus

Features of MCS6506

MCS6512 – 40 Pin Package

Vss	1	40	RES
RDY	2	39	ϕ_2 (OUT)
ϕ_1	3	38	S.O.
IRQ	4	37	ϕ_2
Vss	5	36	DBE
NMI	6	35	N.C.
SYNC	7	34	R/W
Vcc	8	33	DB0
AB0	9	32	DB1
AB1	10	31	DB2
AB2	11	30	DB3
AB3	12	29	DB4
AB4	13	28	DB5
AB5	14	27	DB6
AB6	15	26	DB7
AB7	16	25	AB15
AB8	17	24	AB14
AB9	18	23	AB13
AB10	19	22	AB12
AB11	20	21	Vss

MCS6512

- * 65K Addressable Bytes of Memory
- * $\overline{\text{IRQ}}$ Interrupt
- * $\overline{\text{NMI}}$ Interrupt
- * RDY Signal
- * 8 Bit Bi-Directional Data Bus
- * SYNC Signal
- * Two phase input
- * Data Bus Enable

Features of MCS6512

MCS6513 – 28 Pin Package

Vss	1	28	RES
ϕ_1	2	27	ϕ_2
IRQ	3	26	R/W
NMI	4	25	DB0
Vcc	5	24	DB1
AB0	6	23	DB2
AB1	7	22	DB3
AB2	8	21	DB4
AB3	9	20	DB5
AB4	10	19	DB6
AB5	11	18	DB7
AB6	12	17	AB11
AB7	13	16	AB10
AB8	14	15	AB9

MCS6513

- * 4K Addressable Bytes of Memory (AB00-AB11)
- * Two phase clock input
- * $\overline{\text{IRQ}}$ Interrupt
- * $\overline{\text{NMI}}$ Interrupt
- * 8 Bit Bi-Directional Data Bus

Features of MCS6513

MCS6514 – 28 Pin Package

Vss	1	28	RES
ϕ_1	2	27	ϕ_2
IRQ	3	26	R/W
Vcc	4	25	DB0
AB0	5	24	DB1
AB1	6	23	DB2
AB2	7	22	DB3
AB3	8	21	DB4
AB4	9	20	DB5
AB5	10	19	DB6
AB6	11	18	DB7
AB7	12	17	AB12
AB8	13	16	AB11
AB9	14	15	AB10

MCS6514

- * 8K Addressable Bytes of Memory (AB00-AB12)
- * Two phase clock input
- * $\overline{\text{IRQ}}$ Interrupt
- * 8 Bit Bi-Directional Data Bus

Features of MCS6514

MCS6515 – 28 Pin Package

Vss	1	28	RES
RDY	2	27	ϕ_2
ϕ_1	3	26	R/W
IRQ	4	25	DB0
Vcc	5	24	DB1
AB0	6	23	DB2
AB1	7	22	DB3
AB2	8	21	DB4
AB3	9	20	DB5
AB4	10	19	DB6
AB5	11	18	DB7
AB6	12	17	AB11
AB7	13	16	AB10
AB8	14	15	AB9

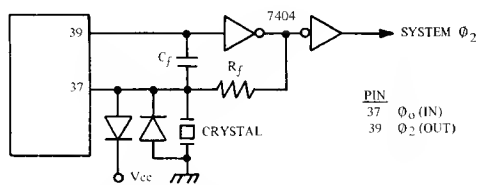
MCS6515

- * 4K Addressable Bytes of Memory (AB00-AB11)
- * Two phase clock input
- * $\overline{\text{IRQ}}$ Interrupt
- * 8 Bit Bi-Directional Data Bus

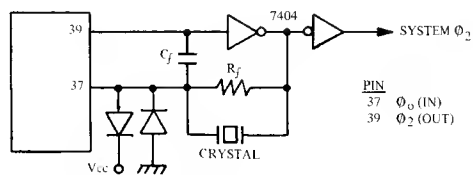
Features of MCS6515

TIME BASE GENERATION OF INPUT CLOCK

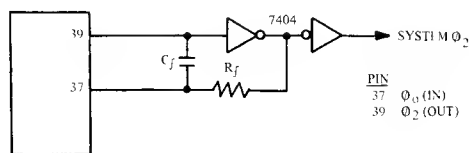
MCS6502



MCS6502 Parallel Mode Crystal Controlled Oscillator

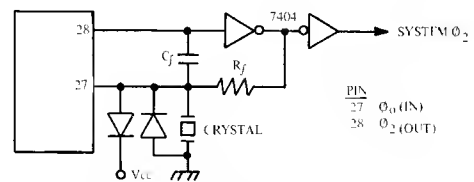


MCS6502 Series Mode Crystal Controlled Oscillator

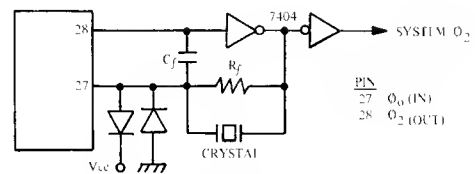


MCS6502 Time Base Generator - RC Network

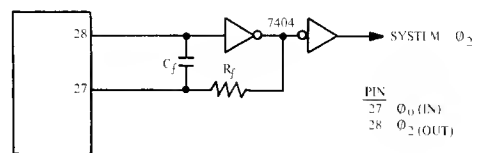
MCS6503, MCS6504, MCS6505, MCS6506



MCS6503, 4, 5, 6 Parallel Mode Crystal Controlled Oscillator



MCS6503, 4, 5, 6 Series Mode Crystal Controlled Oscillator



MCS6503, MCS6504, MCS6505, MCS6506 Time Base Generation RC Network