UNIVERSITY OF COLOMBO, SRI LANKA

FACULTY OF TECHNOLOGY

LEVEL I EXAMINATION IN TECHNOLOGY - SEMESTER II– 2022

IA 1301 – ANALOG AND DIGITAL ELECTRONICS I

Two (02) hours

Answer only 4 questions.

Electronic calculators are allowed.

No. of pages: 13

Important Instructions to Candidates

- If a page or part of this question paper is not printed, please inform the supervisor immediately.
- Enter your index number on all pages of the answer script.
- Write the answers to the questions in the space provided in the question paper.
- Electronic devices capable of storing and retrieving text, including electronic dictionaries and mobile phones are not allowed.
- If you have any doubt about the interpretation of the wording of a question, make your own assumption, but clearly state it in the script.

Index No: …….....

Q	M
1	
2	
3	
4	
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Total	

Index No: ……..…..

01. You are asked to design a 1 kW single-phase full bridge diode rectifier to drive a DC motor. The DC motor rated voltage and current are 120 V and 8 A respectively.

(a). Draw the circuit diagram for the rectifier without the smoothing capacitor.

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(3 marks)

(b). Calculate the required AC voltage (r.m.s) input to the rectifier.

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(8 marks)

(c). Calculate the turns ratio of the required transformer if the supply voltage is 230 V (AC r.m.s).

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(3 marks)

(d). Explain a method to vary the rectifier voltage output continuously.

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(3 marks)

(e). Assume that now a smoothing capacitor is connected to the output of the rectifier. Draw the rectifier input current waveform.
Hint: The output current waveform of the DC motor is purely DC.

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(4 marks)

(f). Briefly explain a method to obtain DC voltages in two polarities (positive and negative). Draw relevant circuit diagrams.

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(4 marks)

02. You are asked to design an inverting OP-AMP with a gain of 1000.

(a). Draw the amplifier circuit and derive an equation for the output gain. Provide suitable values for the circuit elements.

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(5 marks)

(b). If the open loop gain of the OP-AMP IC is 100 000. Calculate the actual gain that is provided by the amplifier.

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(10 marks)

(c). Draw the closed loop system diagram for the OP-AMP amplifier circuits.

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(2 marks)

(d). Show that for the inverting OP-AMP, $\frac{Feedback\ resistance}{Input\ resistance} \cong \frac{1}{Feedback\ gain}$

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(8 marks)

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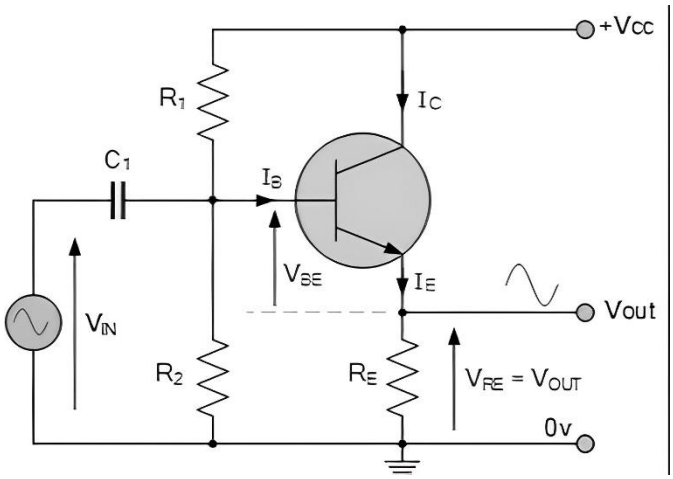
03. Consider the transistor amplifier circuit shown in Figure 3.1.



$R_1 = 4.7\ k\Omega$
$R_2 = 5.6\ k\Omega$
$R_E = 4.7\ k\Omega$
Vcc = 12 V
Transistor $\beta = 100$.

Figure 3.1 Transistor amplifier circuit

(a). State the transistor amplifier configuration.

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(2 marks)

(b). Calculate the base biasing voltage V_B.

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(3 marks)

(c). Calculate the Emitter biasing voltage V_E and V_{CE}.

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(5 marks)

(d). Calculate the Emitter current $I_{E.}$

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(3 marks)

(e). Draw Ic $_{(SAT)}$ Vs. V_{CE} graph.

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(5 marks)

(f). The output voltage is given by the following equation where the internal emitter resistance $r_e^{/} \approx \frac{25\ mV}{I_E}$.

$$V_{out} = \frac{V_{in} \times R_E}{r_e^{/} + R_E}$$

Calculate the voltage gain of the amplifier.

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(4 marks)

(g). What is the current gain of the amplifier?

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(3 marks)

04. a). A combinational logic circuit has three inputs (*A, B* and *C*) and two outputs (*P* and *Q*). The logic expression for *P* is given by,

$$P = A + \bar{A}\bar{B} + ABC$$

(i). Convert the logic expression for *P* into **standard** Sum of Products (SOP) form.

(4 marks)

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(ii). Hence fill the column corresponding to *P* in Table 4.1.

(2 marks)

Table 4.1

A	B	C	P	Q
0	0	0		0
0	0	1		0
0	1	0		1
0	1	1		1
1	0	0		1
1	0	1		1
1	1	0		0
1	1	1		0

(iii). Obtain the **standard** Product of Sums (POS) expression for *Q* (in Table 4.1). *(4 marks)*

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(iv). Obtain the most simplified SOP expression for *Q*. *(4 marks)*

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(v). Construct the logic circuit for *Q* using two-input NAND gates. *(4 marks)*

b). An indicator light has to be turned on in a vehicle dashboard when the driver or/and the passenger in the front seat have not fastened the seatbelts when the engine is on.

The indicator light is turned on when the output signal *IND* is 1.

The signal *ENG* becomes 1 when the engine is on. The signals from the pressure sensors in the driver seat and the passenger seat (*D_seat* and *P_seat* respectively) become 1 when

the seats are occupied. *D_belt* and *P_belt* signals from the seat belt buckles of the driver and the passenger seats become 1 when the belts are fastened.

Design the logic circuit for the above system.

Note: Constructing the truth table is not mandatory

(7 marks)

05. a). What is the main difference between a latch and a flip-flop? *(2 marks)*

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b). Construct a JK flip-flop by modifying a 'NAND gate based SR latch with an enable input'. Inputs and outputs must be labelled.

(5 marks)

c). Show that a T flip-flop can be constructed using a JK flip flop (use the block diagram of JK flip flop).

(3 marks)

d) (i). Consider Figure 5.1 and fill Table 5.1. *(8 marks)*

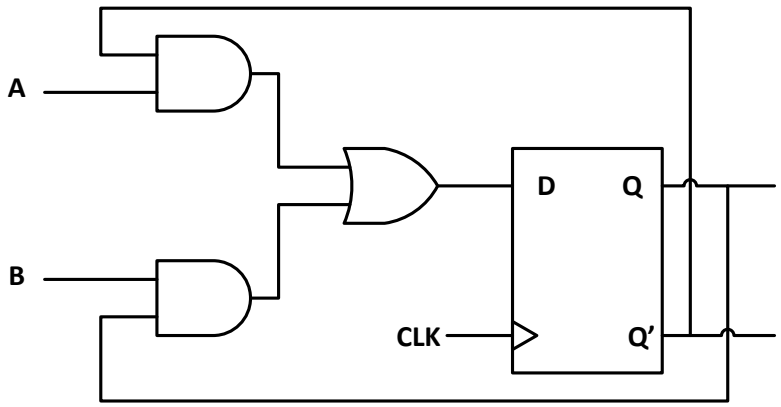

Figure 5.1

Table 5.1

A	B	Q_n	Q'_n	Q_{n+1}	Q'_{n+1}
1	0	0	1		
1	0	1	0		
0	1	0	1		
0	1	1	0		
1	1	0	1		
1	1	1	0		
0	0	0	1		
0	0	1	0		

(ii). Hence identify the sequential logic device in Figure 5.1. *(3 marks)*

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e). Consider the circuit in Figure 5.2 and complete the timing diagram in Figure 5.3.

(4 marks)

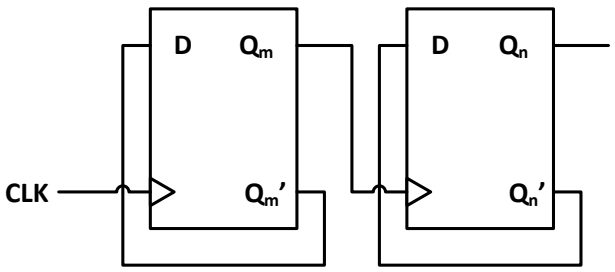

Figure 5.2

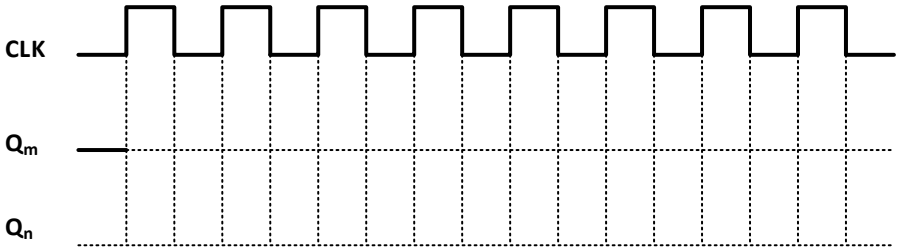

Figure 5.3

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