

System-on-Chip Approach to High Performance Audio Signal Processing and Transport

MRes System Engineering Project Proposal (Draft)

Ilya Dmitrichenko

February 28, 2011

Abstract

Looking at recent innovative products for general and application-specific embedded computing, majority is Systems-on-Chip, some integrate a greater deal of peripherals and most are low-cost and low-power; not to mention rapid improvements of various performance factors. However it appears that in audio application area there are fewer innovative devices and most of the vendors in the field apply proprietary technologies. On large, these are featuring an FPGA along with system control computer and separate peripheral controllers.

1 Introduction

Most of interesting SoC devices on the market, dominated by ARM cores, rather rarely include high performance FPU. Some incorporate GPUs. There are ways of using GPU for many types of signal processing applications, however not many had yet been found particularly versatile for audio. This may be an interesting subject, though the purpose of this project is to bring yet another platform, which had been primarily deployed in area with a different nature of requirements. For flexibility and other architectural reasons, popular x86 family is not being considered. Although multiple other alternatives are to be studied and discussed.

2 Aims & Objectives

This project aims at developing a suitable hardware closely coupled with high-level software framework to facilitate research in the field of distributed audio processing and control, also capable to incorporate real-time network streaming and data storage, applying latest technology standards. During the primary phase main interest is to implement a platform using open-source software and hardware, with major orientation into the second, utilising OpenSPARC architecture [9, 5]. OpenSPARC provides multi-core general-purpose high performance host processor and by being open-source it can be greatly extended to provide a configurable datapath pipeline with semi-fixed audio function units. It also features network and storage interface controllers, therefore in later phase technologies such as Audio Video Bridging [3, 1, 2] can be integrated to build a distributed system with multiple nodes of different function classes.

Various proprietary technologies exist, which provide accelerated audio processing. However, these are not accessible to researchers, only end-user application software is provided by most vendors.

Dedicated DSP chips can be utilised, however the algorithm code requires extensive modifications to run functions that DSP chip provides. Popular open-source software that is available to audio researchers [12, 13, 11] has been utilising host CPU (largely x86) to carry out most of DSP routines. This is a practically proven concept, though often when multichannel sound is concerned, it is desired that each channel

is processed by equaliser and compressor before it is mixed. Another important aspect is floating-point conversion. These components often become particularly intensive in computation. It is not disagreed that GPU approach may be applied [6, 7, 8], though the aim is to build a single-chip device. The benefits of OpenSPARC are its free open-source license as well as advanced 64-bit architecture [10] with all necessary peripherals.

Additional issues to be addressed in the project to certain extend, would be in the area of multi-threaded and multi-application host audio processing. Hardware embedded in the CPU chip would provide facilities to accelerate signal processing, which traditionally had been handled by software or analogue outboard. The configurable datapath with semi-fixed function blocks is modeling the analogue mixing console with outboard dynamics and equalisers, as well as patch-bays.

This should be achieved without creating a new instruction set, i.e. only adding special function registers and a clock domain. Certainly, the memory controller will need to be coupled with a domain specific extension, providing an optimal software interface. With this architecture it should be possible to incorporate such implementation into a different system, such as less expensive ARM-based solution or other. However, in the duration of first phase of the project, minimum complexity has to be taken care of. This implies that some of more advanced DSP units may have to be implemented in the later phase. The aim is to produce the basis for further work.

The purpose is dual, it is a very challenging research project as well as potential building block for commercial audio systems.

3 Technical Requirements

OpenSPARC is a large multi-core SoC, however it is possible to build a smaller system [4] on FPGA, optimised for the size of available target device.

References

- [1] AVnu Alliance. AVB for Professional Use.
- [2] AVnu Alliance. AVB Networking Technology.
- [3] IEEE. The Audio/Video Bridging Task Group.
- [4] Sun Microsystems. OpenSPARC on FPGA.
- [5] Sun Microsystems. OpenSPARC Documents and Source Code.
- [6] Jonathan Moore, David; Wakefield. The potential of high performance computing in audio engineering. In *Audio Engineering Society Convention 126*, 5 2009.
- [7] Vesa; Smith Julius O. Savioja, Lauri; Välimäki. Real-time additive synthesis with one million sinusoids using a gpu. In *Audio Engineering Society Convention 128*, 5 2010.
- [8] Nicolas Tsingos. Using programmable graphics hardware for acoustics and audio rendering. In *Audio Engineering Society Convention 127*, 10 2009.
- [9] D.L. Weaver. *OpenSPARC Internals*. Sun Microsystems, 2008.
- [10] D.L. Weaver, T. Germond, and SPARC International. *The SPARC architecture manual: version 9*. PTR Prentice Hall, 1994.
- [11] Wikipedia. Information on CSound software.
- [12] Wikipedia. Information on Pure Data software.
- [13] Wikipedia. Information on SuperCollider software.