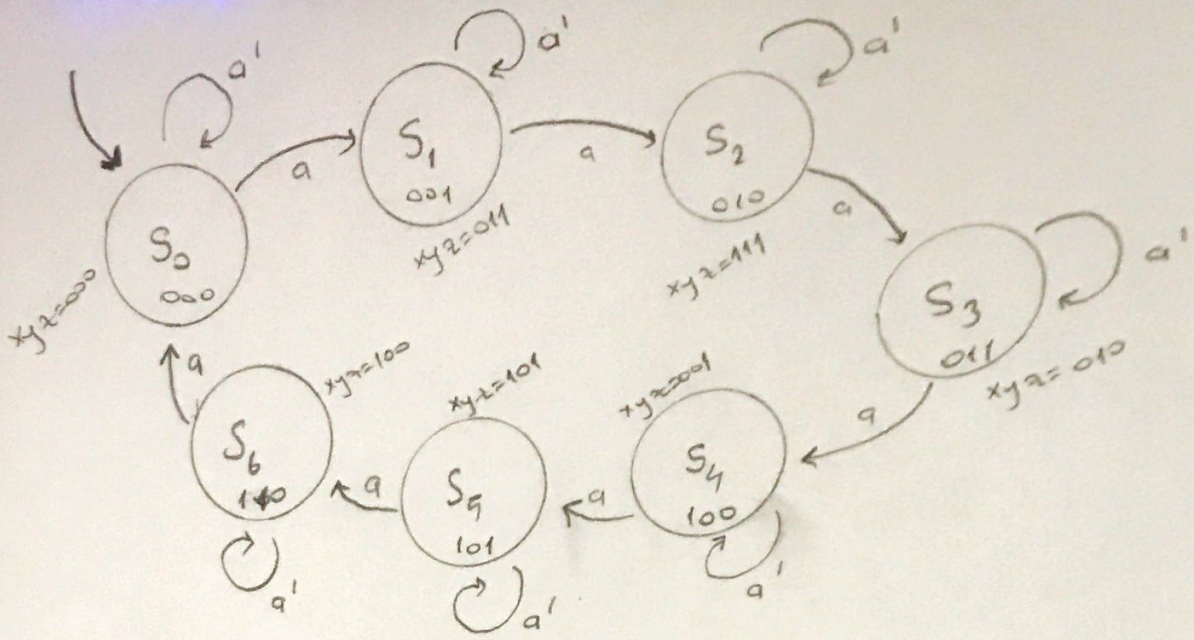



⇒ 7 states (3 bits register)

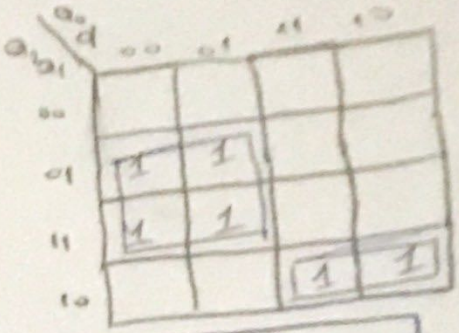
⇒ a is input. ($a_2, a_1, a_0$)

⇒ outputs → xyz ($n_2, n_1, n_0$)

| | $a_2$ | $a_1$ | $a_0$ | a | $n_2$ | $n_1$ | $n_0$ | x | y | z |
|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $S_0$ | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| $S_1$ | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| $S_2$ | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| $S_3$ | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| $S_4$ | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| $S_5$ | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| $S_6$ | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| undef | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

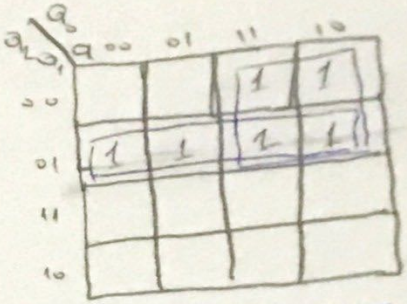
| States | $q_2$ | $q_1$ | $q_0$ |
|---|---|---|---|
| $S_0$ | 0 | 0 | 0 |
| $S_1$ | 0 | 0 | 1 |
| $S_2$ | 0 | 1 | 0 |
| $S_3$ | 0 | 1 | 1 |
| $S_4$ | 1 | 0 | 0 |
| $S_5$ | 1 | 0 | 1 |
| $S_6$ | 1 | 1 | 1 |

for x:



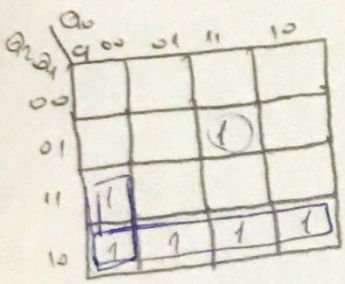
$x = q_1 q_0' + q_2 q_1' q_0$

for y:



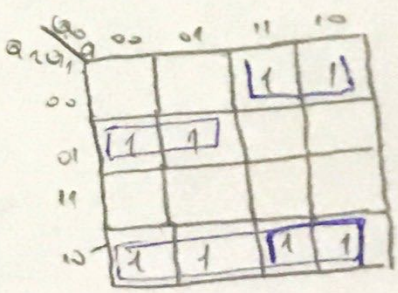
$y = q_2' q_0 + q_2' q_1$

for $n_2$:



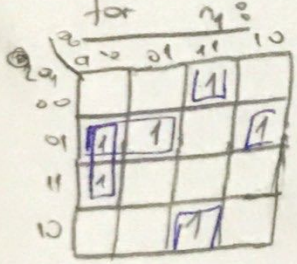
$n_2 = q_2' q_1 q_0 q + q_2 q_1' + q_2 q_0' q'$

for z:



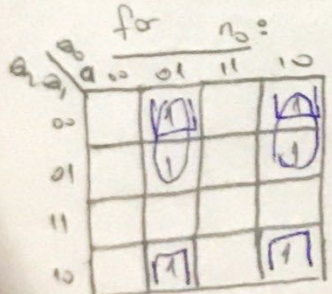
$z = q_1' q_0 + q_2' q_1 q_0' + q_2 q_1'$

for $n_1$:



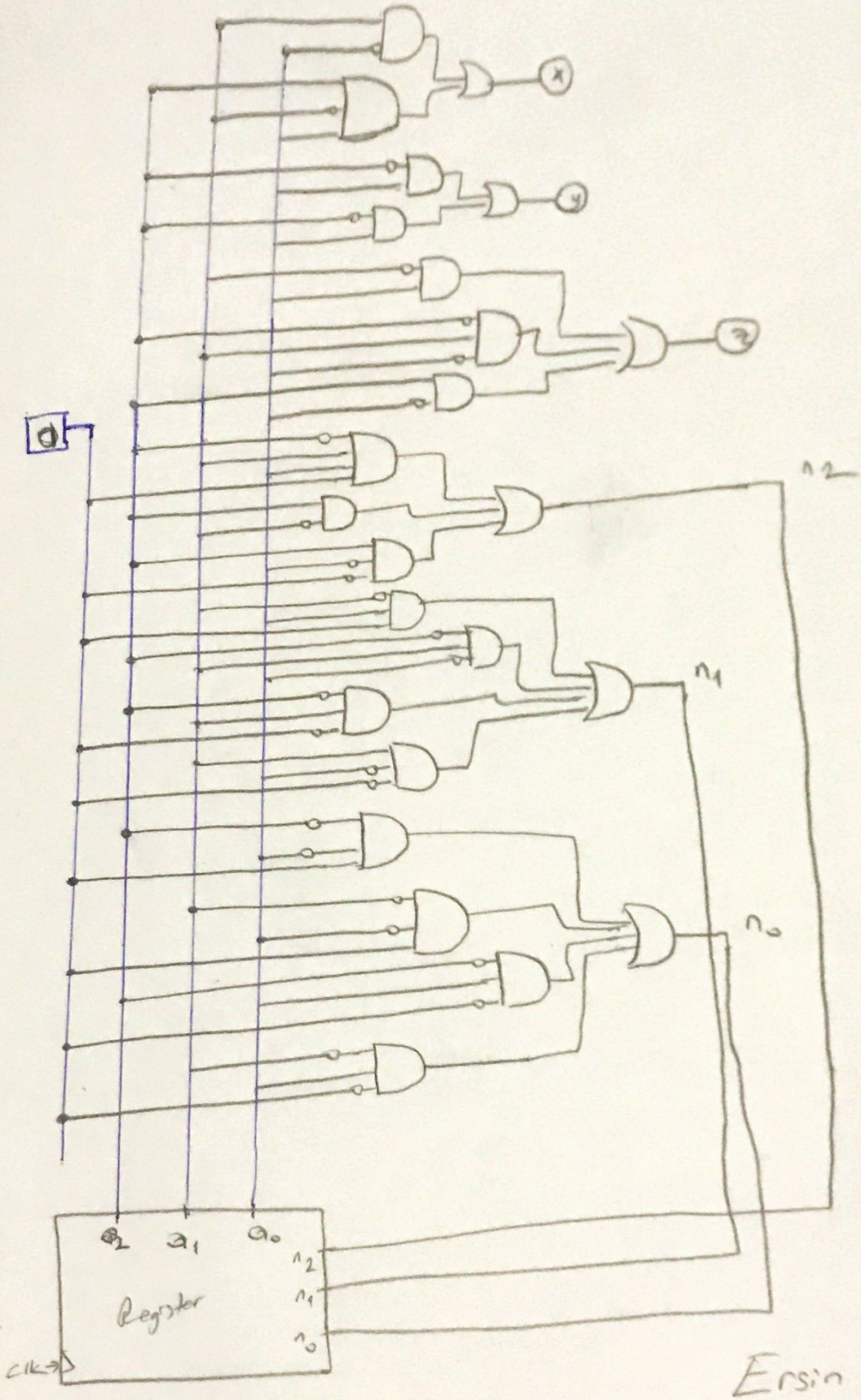
$n_1 = q_1' q_0 q + q_2' q_1 q_0' + q_2 q_1 q' + q_1 q_0' q'$

for $n_0$:



$n_0 = q_1' q_0' q + q_1' q_0 q' + q_2' q_0' q + q_2' q_0 q'$

# Combinational Circuit

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