EGE UNIVERSITY LOGIC DESIGN LABORATORY
EXPERIMENT-4

Combinational Circuit Design

Cover Page
Logic Design Lab4
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EXPERIMENTAL WORK

Design a combinational circuit that accepts 4-bit number (ABCD) and generates 3-bit binary number output (XYZ) that approximates the square root of the number. (For example, if the square root is 3.5 or larger, give the result of 4. If the square root is <3.5 and >= 2.5, give a result of 3.)

Problem Description

Verilen 4 bitlik sayının karekökünü alıp yuvarladık. Daha sonra 3 bitlik outputu yazdık. 3 bitin her biri için Karnough Map leri oluşturduk ve hepsi için ayrı ayrı çözdük, sadeleştirdik. Daha sonra devreleri simulator.io da yalnız NAND ile ve yalnız NOR ile kurduk. Kurduğumuz devrelerde bazen NOT gateler birbirini götürdü, dolayısıyla götüren kapılar görünmemekte.

1- Fill the truth table and obtain the boolean functions for X, Y and Z outputs using Karnaugh maps.

TRUTH TABLE

Inputs				Outputs		
A	B	C	D	X	Y	Z
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	1	0
0	1	1	1	0	1	1
1	0	0	0	0	1	1
1	0	0	1	0	1	1
1	0	1	0	0	1	1
1	0	1	1	0	1	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0

KARNAUGH MAP OPTIMIZATION

0	0	0	0
0	0	0	0
0	1	1	1
0	0	0	0

X= ABC+ABD

0	0	1	0
1	1	1	1
1	0	0	0
1	1	1	1

Y= A’B+AB’+A’CD+BC’D’

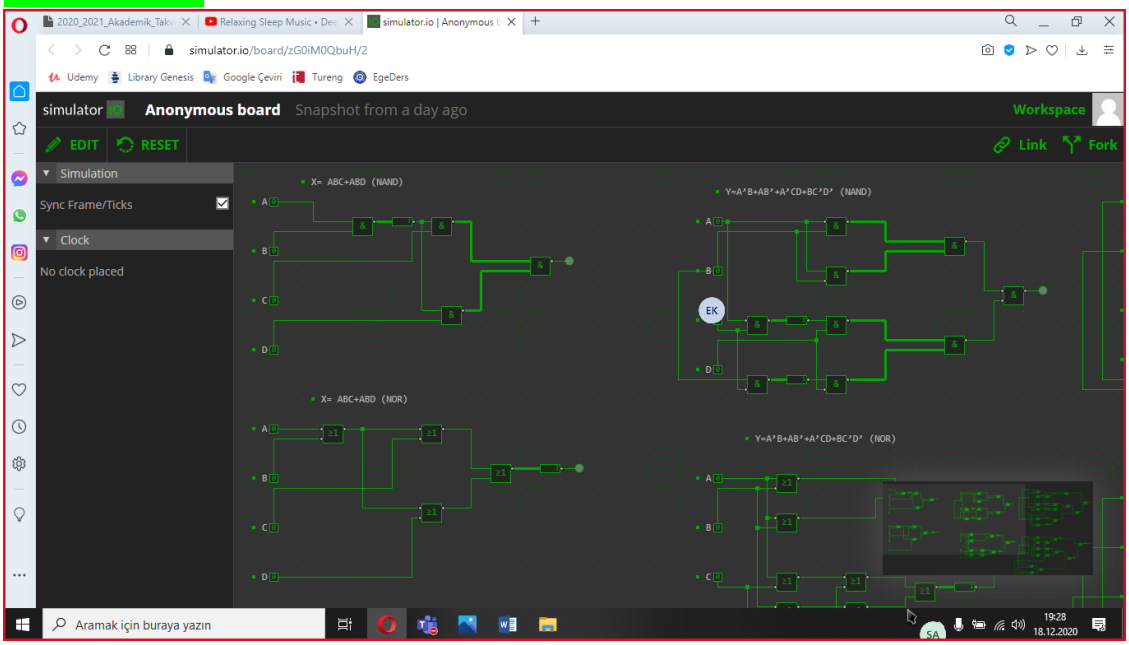
0	1	0	1
0	0	1	0
1	0	0	0
1	1	1	1

Z= AB’+AC’D’+B’C’D+B’CD’+A’BCD

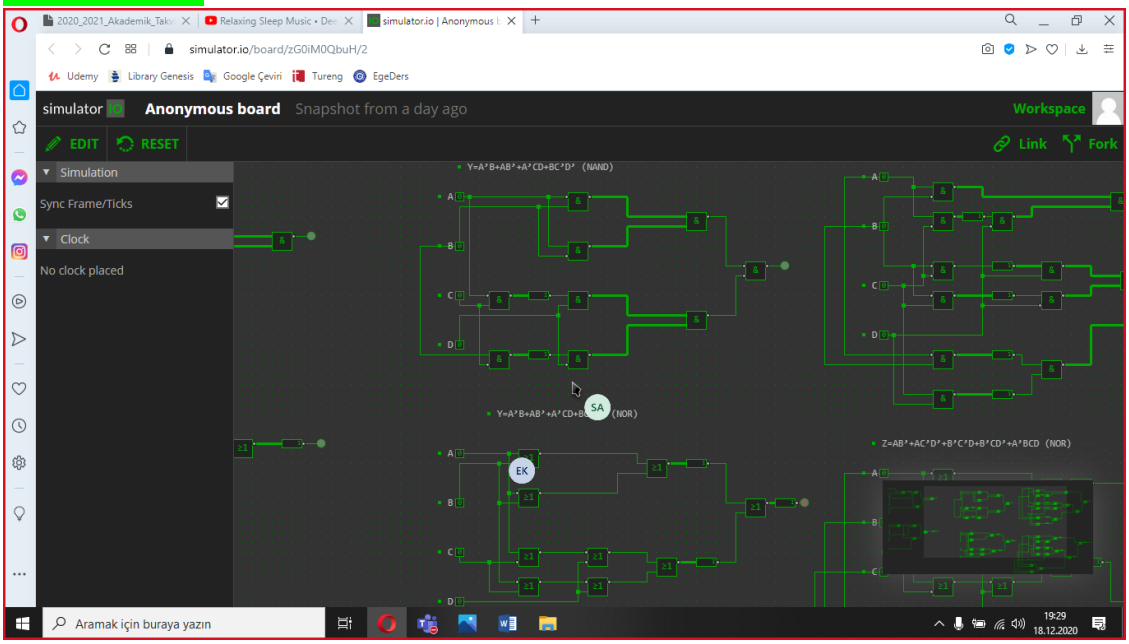
2- Draw the logic circuit diagram of the Boolean functions X, Y and Z

Link::https://simulator.io/board/zG0iM0QbuH/2

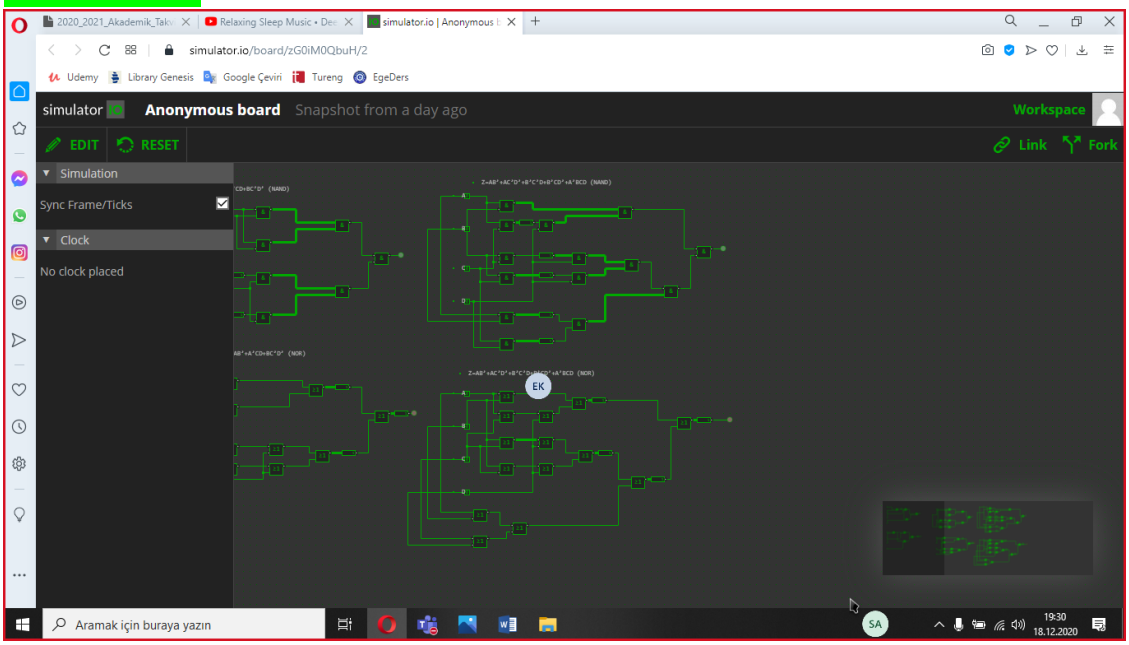
X DEVRELERİ



Y DEVRELERİ



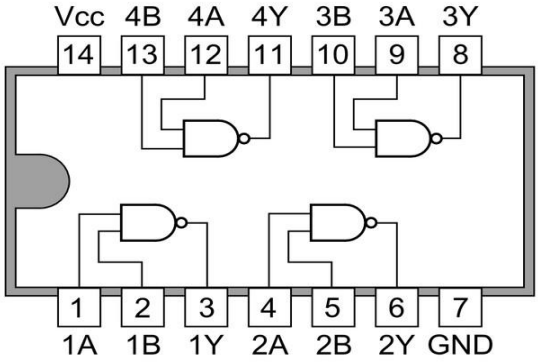
Z DEVRELERİ



Link::https://simulator.io/board/zG0iM0QbuH/2 (Yukarıdakiyle Aynı)

Video, Egerders'e eklendi.

7400 Quad 2-input NAND Gates



7402 Quad 2-input NOR Gates