Logic Design Lab 8

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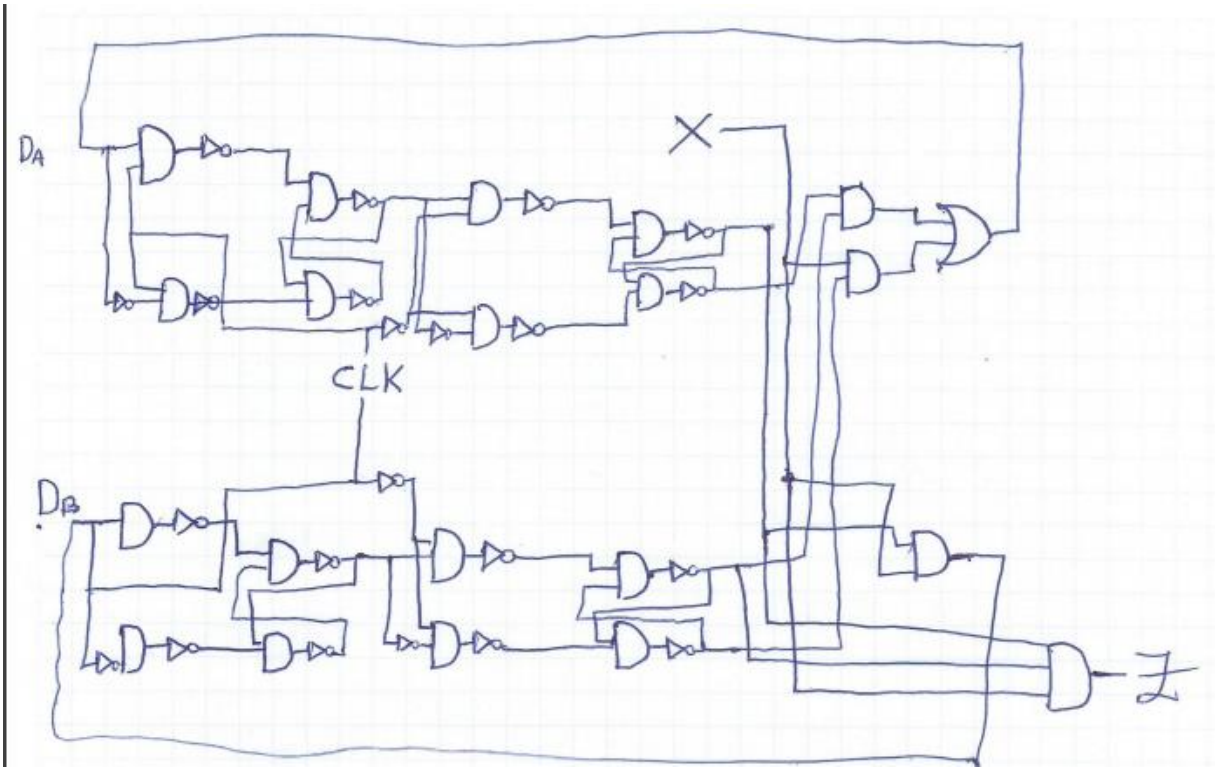
Problem description

D latch'leri uygun şekilde bağlayıp 2 flip-flop oluşturduk. Daha sonra inputları ve outputları verilen denkleme göre bağladık.

1-Logic Diagram



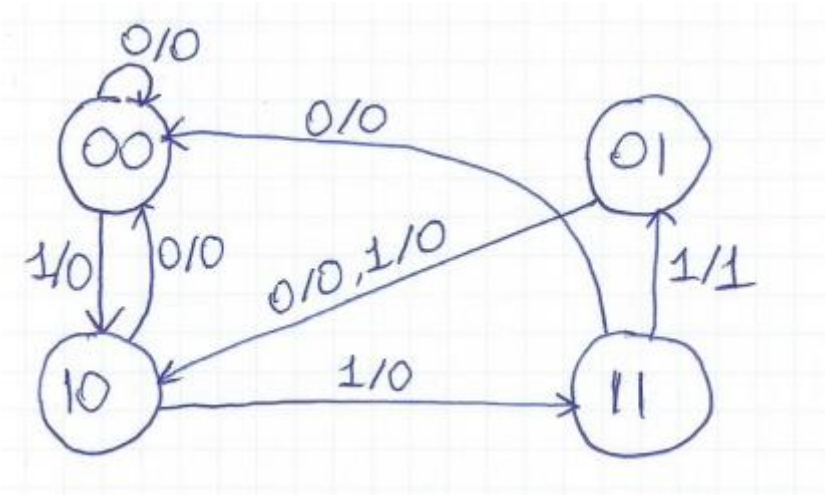
2-State Table ve State Diagram

DA=QA'QB+QB'X

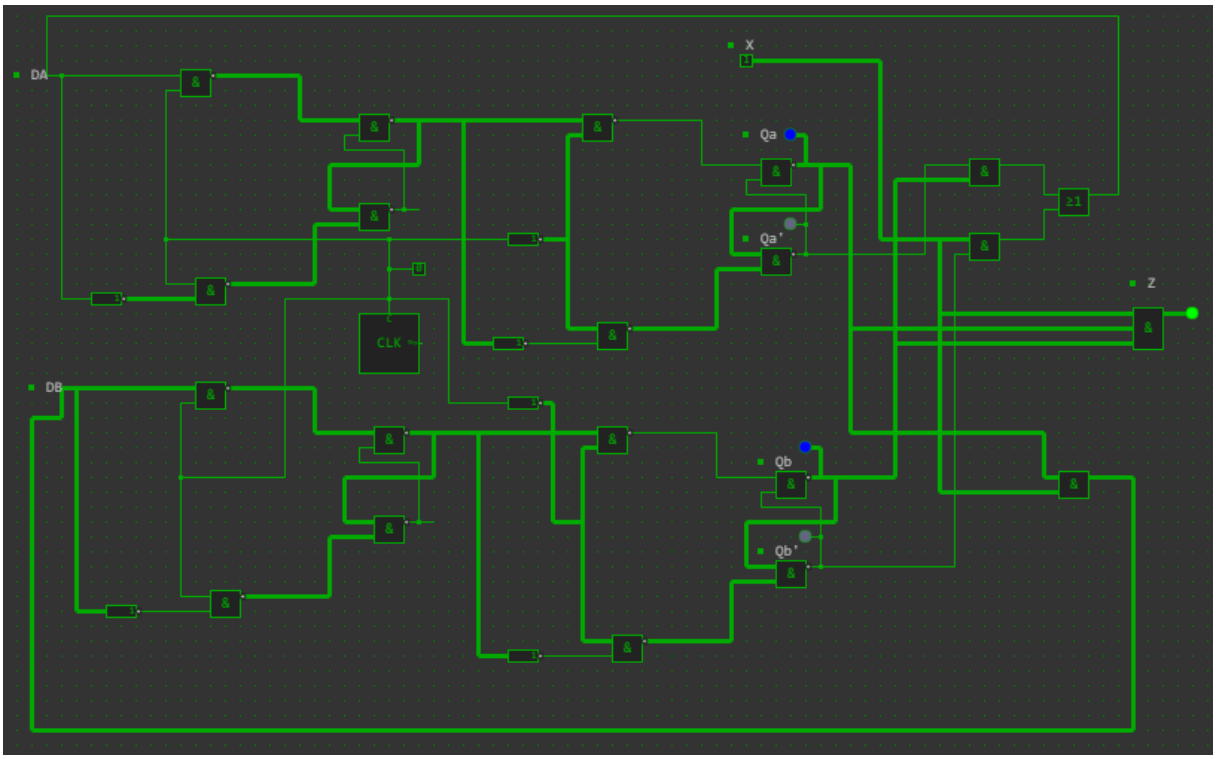
DB=QA X

Z= QA QB X

Qa	Qb	X	Qa+	Qb+	Z
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	1	1



3-Circuit Design



Link: http://simulator.io/board/yINRYqNHtq/3

Video Egeders'e eklendi.