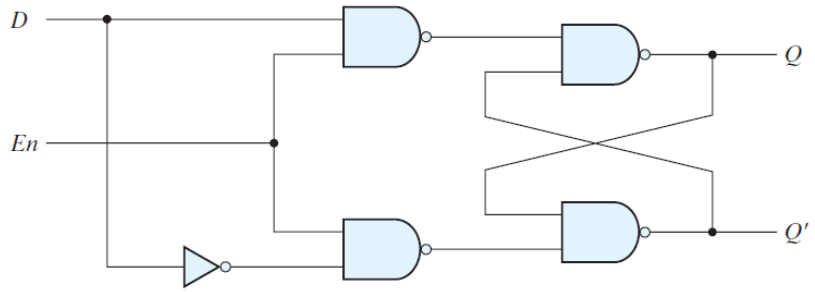
Tutorial 9: Flip-flops and counters

Q1. The D latch of Figure below is constructed with four NAND gates and an inverter. Consider the following three other ways for obtaining a D latch. In each case, draw the logic diagram and verify the circuit operation.
(a) Use NOR gates for the SR latch part and AND gates for the other two. An inverter may be needed.
(b) Use NOR gates for all four gates. Inverters may be needed.
(c) Use four NAND gates only (without an inverter). This can be done by connecting the output of the upper gate in Figure to the input of the lower gate (instead of the inverter output).



Q2. A binary ripple counter uses flip-flops that trigger on the positive-edge of the clock. What will be the count if
(a) the normal outputs of the flip-flops are connected to the clock and
(b) the complement outputs of the flip-flops are connected to the clock?

Q3. Draw the logic diagram of a four-bit binary ripple countdown counter using
(a) flip-flops that trigger on the positive-edge of the clock and
(b) flip-flops that trigger on the negative-edge of the clock.

Q4. How many flip-flops will be complemented in a 10-bit binary ripple counter to reach the next count after the following counts?
(a) 1001100111 (b) 1111000111 (c) 0000001111

Q5. A flip-flops has a 3 ns delay from the time the clock edge occurs to the time the output is complemented. What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops? What is the maximum frequency at which the counter can operate reliably?

Q6. A digital system has a clock generator that produces pulses at a frequency of 80 MHz. Design a circuit that provides a clock with a cycle time of 50 ns.