Digital Systems -Sequential Logic

Introduction

- Outputs of sequential logic depend on current *and* prior input values – it has ***memory***.
- Some definitions:
  - State: all the information about a circuit necessary to explain its future behavior
  - Latches and flip-flops: state elements that store one bit of state
  - Synchronous sequential circuits: combinational logic followed by a bank of flip-flops

Sequential Circuits

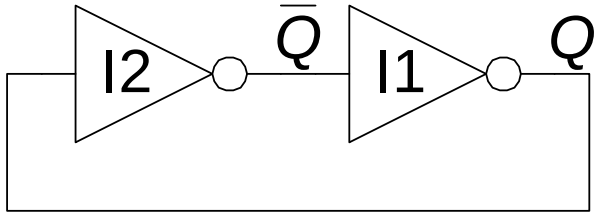
- Give sequence to events
- Have memory (short-term)
- Use feedback from output to input to store information

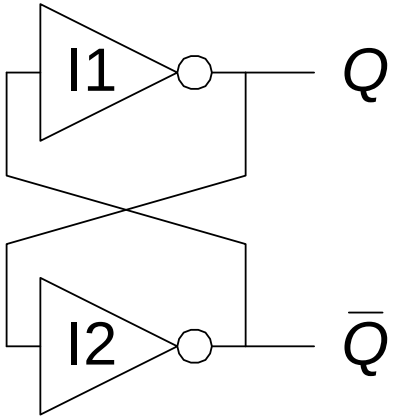
State Elements

- The state of a circuit influences its future behavior
- State elements store state
  - Bistable circuit
  - SR Latch
  - D Latch
  - D Flip-flop

Bistable Circuit

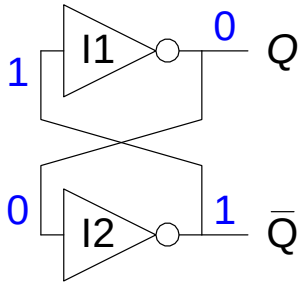
- Fundamental building block of other state elements
- Two outputs: Q, $\overline{Q}$
- No inputs



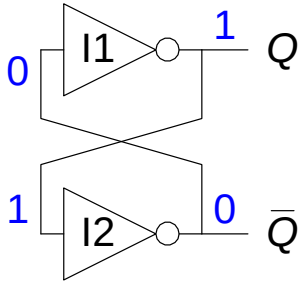


Bistable Circuit Analysis

- Consider the two possible cases:
  - $Q = 0$: then $\overline{Q} = 1$ and $Q = 0$ (consistent)



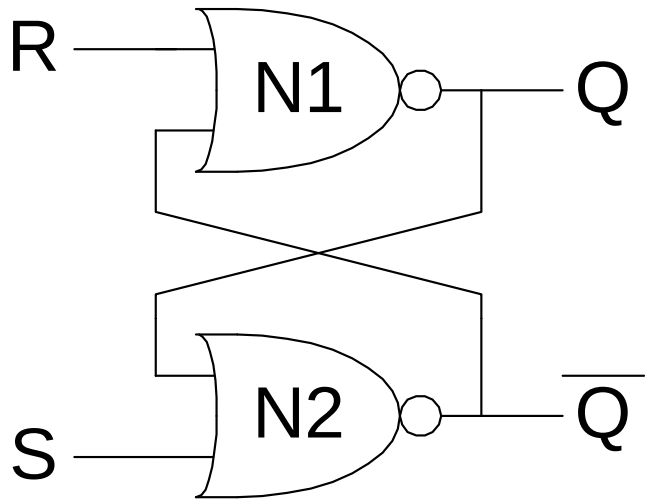
  - $Q = 1$: then $\overline{Q} = 0$ and $Q = 1$ (consistent)



- Bistable circuit stores 1 bit of state in the state variable, Q (or Q)
- But there are **no inputs to control the state**

SR (Set/Reset) Latch

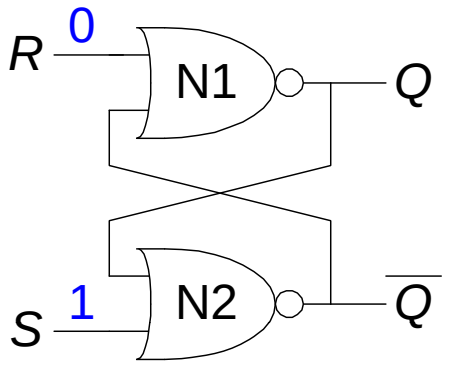
- SR Latch



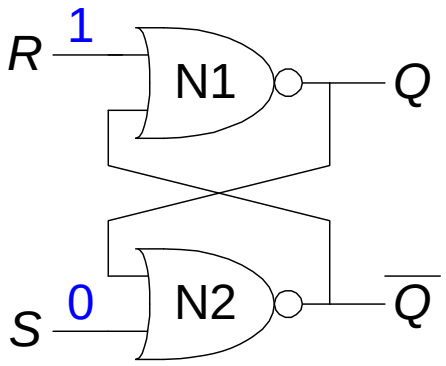
- Consider the four possible cases:
  - $S = 1, R = 0$
  - $S = 0, R = 1$
  - $S = 0, R = 0$
  - $S = 1, R = 1$

SR Latch Analysis

– $S = 1, R = 0$: then $Q = 1$ and $\overline{Q} = 0$

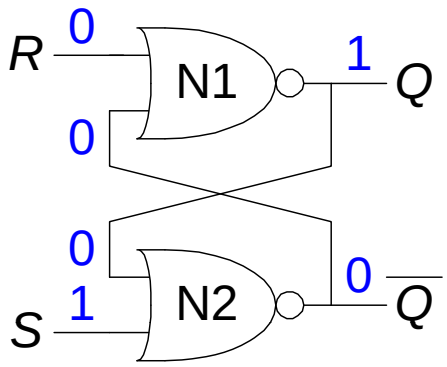


– $S = 0, R = 1$: then $Q = 0$ and $\overline{Q} = 1$

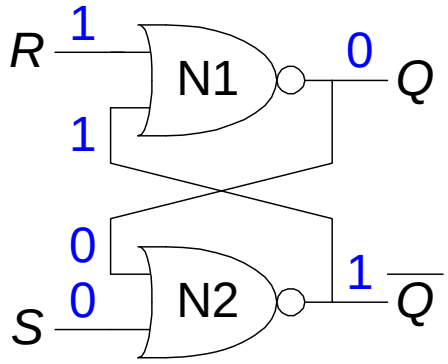


SR Latch Analysis

– $S = 1, R = 0$: then $Q = 1$ and $\overline{Q} = 0$

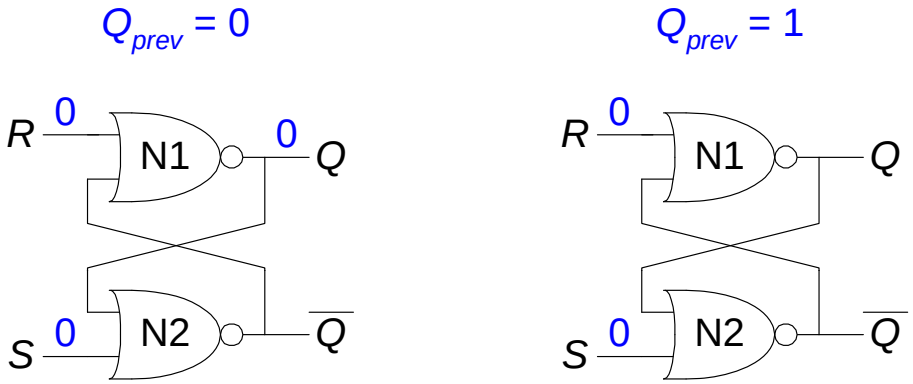


– $S = 0, R = 1$: then $Q = 0$ and $\overline{Q} = 1$

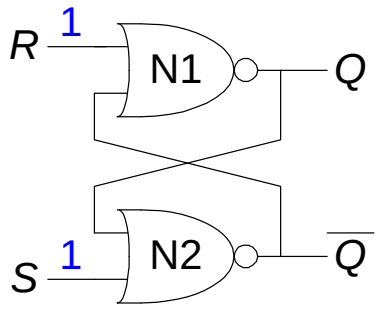


SR Latch Analysis

– $S = 0, R = 0$: then $Q = Q_{prev}$



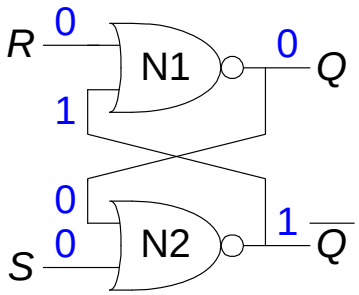
– $S = 1, R = 1$: then $Q = 0$ and $\overline{Q} = 0$



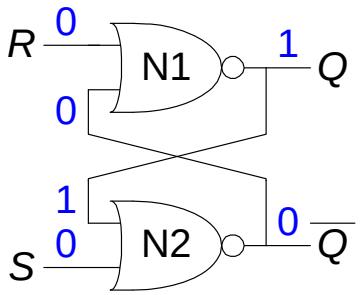
SR Latch Analysis

– $S = 0, R = 0$: then $Q = Q_{prev}$ and $\overline{Q} = \overline{Q_{prev}}$ (memory!)

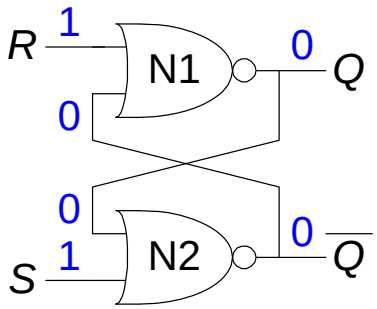
$Q_{prev} = 0$



$Q_{prev} = 1$



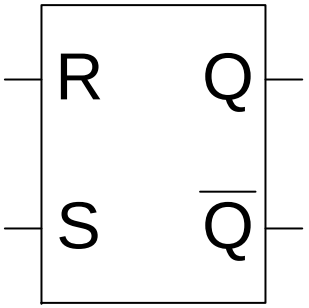
– $S = 1, R = 1$: then $Q = 0$ and $\overline{Q} = 0$ (invalid state: $\overline{Q} \neq$ NOT Q)



SR Latch Symbol

- SR stands for Set/Reset Latch
  - Stores one bit of state (Q)
- Control what value is being stored with S, R inputs
  - Set: Make the output 1 ($S = 1$, $R = 0$, $Q = \mathbf{1}$)
  - Reset: Make the output 0 ($S = 0$, $R = 1$, $Q = \mathbf{0}$)

SR Latch Symbol

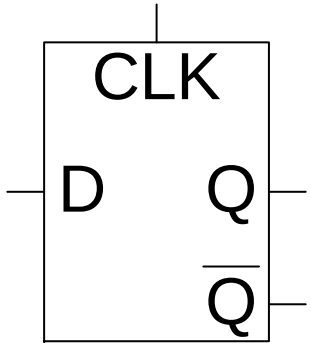


- **Must do something to avoid invalid state (when $S = R = 1$)**

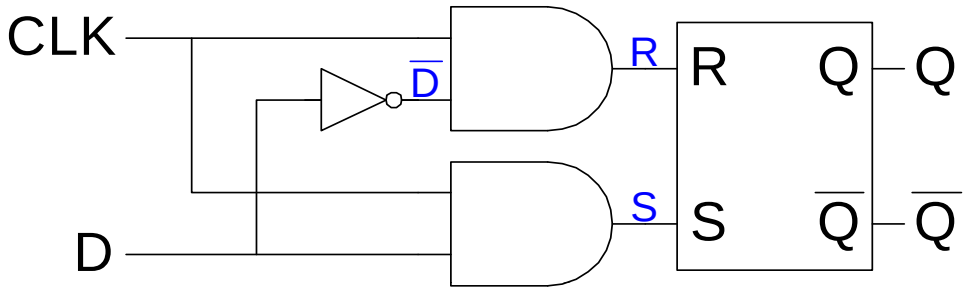
D Latch

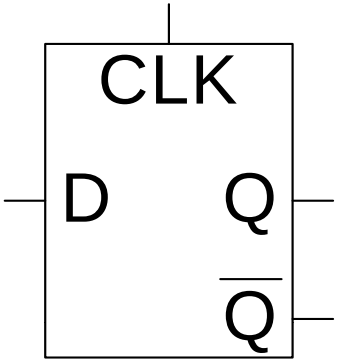
- Two inputs: *CLK*, *D*
  - *CLK*: controls *when* the output changes
  - *D* (the data input): controls *what* the output changes to
- Function
  - When *CLK* = 1, *D* passes through to *Q* (the latch is *transparent*)
  - When *CLK* = 0, *Q* holds its previous value (the latch is *opaque*)
- Avoids invalid case when $Q \neq \text{NOT } \overline{Q}$

D Latch Symbol



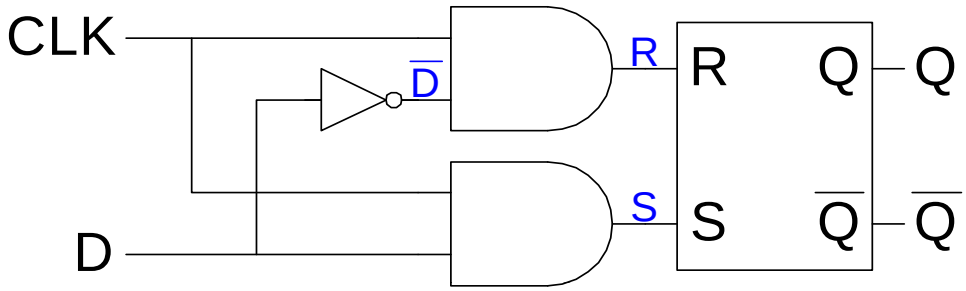
D Latch Internal Circuit

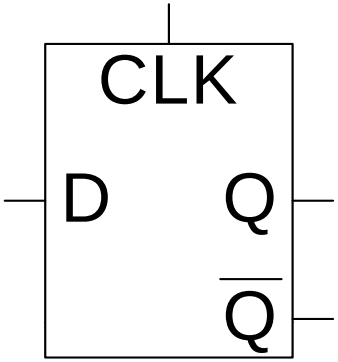




CLK	*D*	$\overline{D}$	*S*	*R*	*Q*	$\overline{Q}$
0	X					
1	0					
1	1					

D Latch Internal Circuit



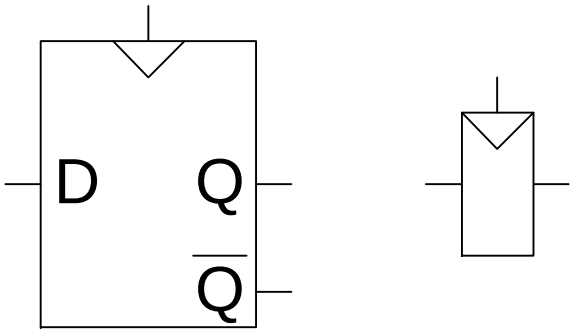


CLK	*D*	$\overline{D}$	*S*	*R*	*Q*	$\overline{Q}$
0	X	$\overline{X}$	0	0	Q_{prev}	$\overline{Q}_{prev}$
1	0	1	0	1	0	1
1	1	0	1	0	1	0

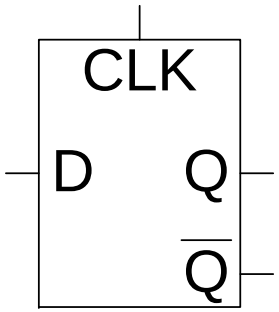
D Flip-Flop

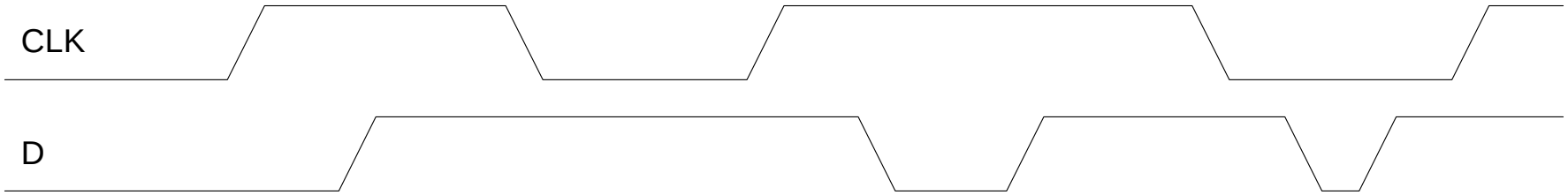
- Two inputs: *CLK*, *D*
- *Function*
  - The flip-flop "samples" *D* on the rising edge of *CLK*
    - When *CLK* rises from 0 to 1, *D* passes through to *Q*
    - Otherwise, *Q* holds its previous value
  - *Q* changes only on the rising edge of *CLK*
- A flip-flop is called an *edge-triggered* device because it is activated on the clock edge

D Flip-Flop Symbols



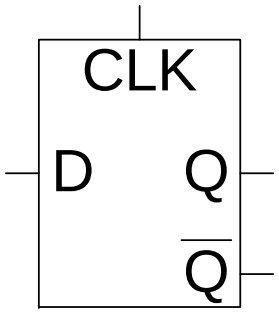
D Latch

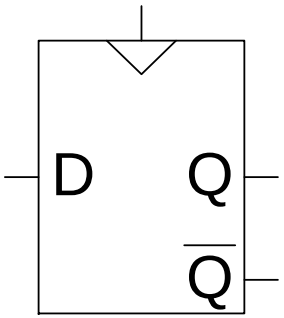


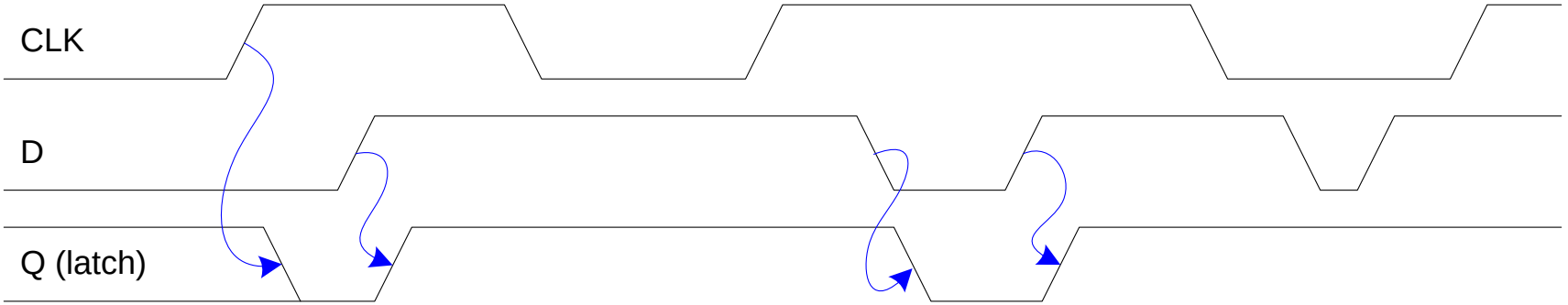


Q (latch)

D Latch

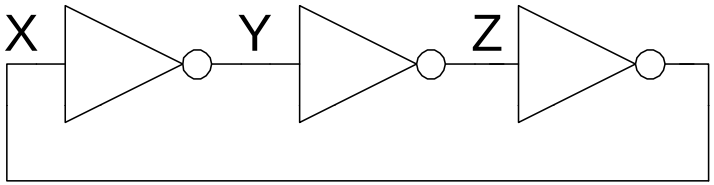


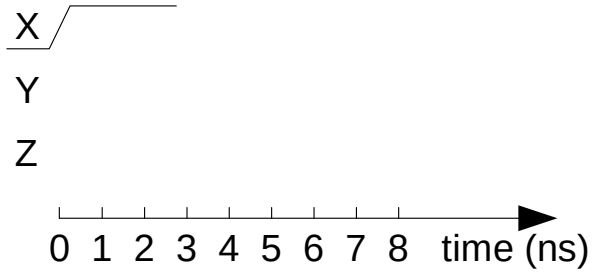




Sequential Logic

- Sequential circuits: all circuits that aren't combinational
- A problematic circuit:

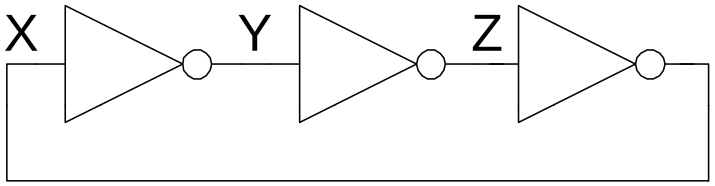


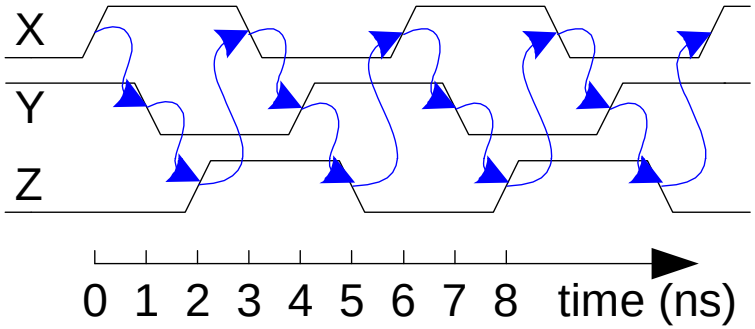


- This circuit has no inputs and 1-3 outputs

Sequential Logic

- Sequential circuits: all circuits that aren't combinational
- A problematic circuit:





- This circuit has no inputs and 1-3 outputs
- It is an astable circuit that oscillates
- Its period depends on the delay of the inverters – which depends on the manufacturing process, temperature, etc
- The circuit has a *cyclic path*: output fed back to input