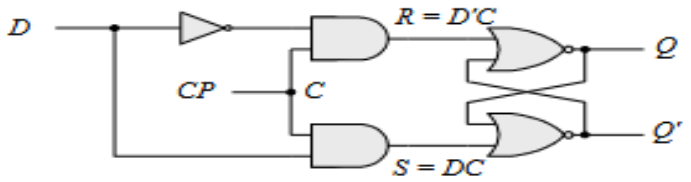
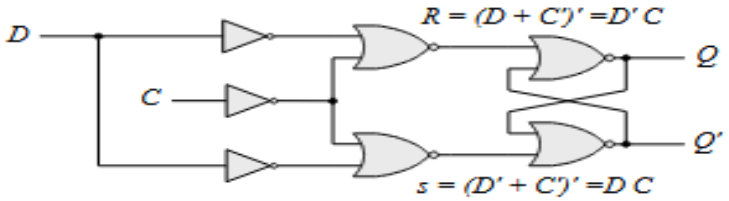
1.

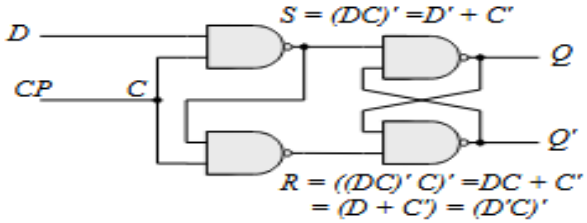
(a)



(b)



(c)

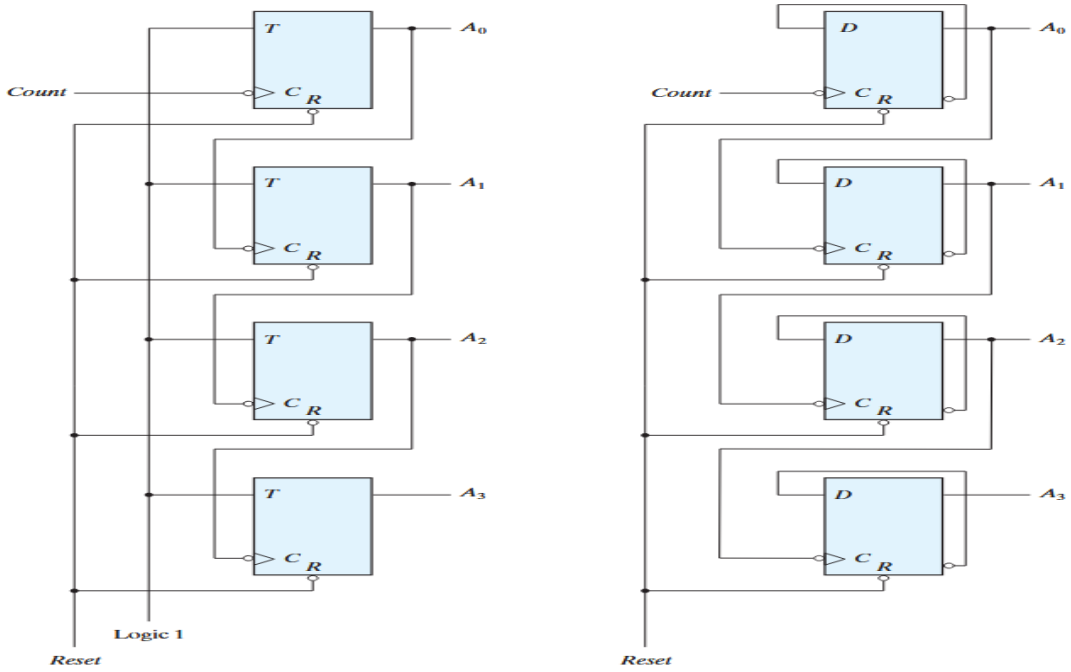


2.

(a) A count down counter.
(b) A count up counter.

3.

(a) With the bubbles in C removed (positive-edge).
(b) With complemented flip-flops connected to C.



(a) With *T* flip-flops

(b) With *D* flip-flops

4.

(a) 10_0110_0111 -> 10_011_**1000** 4;

(b) 11_1100_0111 -> 11_1100_**1000** 4;

(c) 00_0000_1111 -> 00_000**1**_**0000** 5

5. The worst case is when all 10 flip-flops are complemented. The maximum delay is 10 x 3ns = 30 ns. The maximum frequency is 10^9 /30 = 33.3 MHz.

6. The clock generator has a period of 12.5 ns. Use a 2-bit counter to count four pulses. 80/4 = 20 MHz; cycle time = 1000 x 10^{-9} /20 = 50 ns.