Digital Systems
CS227

Date: 24th Nov 2022 Endsem
Full Marks 100 Duration: 180 minutes

Question no 1 to 10 are of multiple choice type with four options and each of them carries 4 marks. Pick the correct option and justify your answer appropriately. Wrong answer will carry (-1) marks. Any answer without any option will be treated as "not attempted" and will fetch 0 marks. Justification must be provided at the same place where the option is selected. Question no 11 to 16 are subjective type and each carries 10 marks

1 A room has one light and two switches. The light is ON only when one of the switches is ON and it is OFF in all the other conditions. If this system is to be realized using two input NAND gates then the minimum number of NAND gates needed is

4 Marks

A less than equal to 3

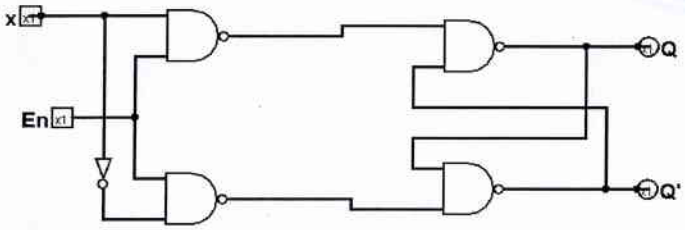
B 4

C 5

D greater than 5

2 Consider the circuit in the following figure. For inputs $En = 1$ and $x = 0$, what will be Q and Q'. Assume that when two wires are connected in a point, is marked using a small filled black circle in the figure.

4 Marks



A 00

B 01

C 10

D 11

3 What input conditions put an SR NOR latch into an indeterminate state?

4 Marks

A 00

B 01

C 10

D 11

4 The functional difference between an SR flip flop and a JK flip is that

4 Marks

A JK flip flop is faster than SR flip flop

B JK flip flop has feedback path

C JK flip flop accepts both inputs 1

D JK flip flop does not require clock pulse

5 For a flip flop with provision of preset and clear

4 Marks

A while presetting, clear is enabled

B while clearing, preset is disabled

C both of the above

D none of the above

6 The number of flip flops needed for a decade counter is

4 Marks

A 3

B 4

C 5

D 10

7 Consider the following verilog code for the *fun* module. This code module represents

```
module fun(input a,b,c, output d);
assign d = c ? a : b;
endmodule
```

4 Marks

A a 2×1 Mux with c as select input

B a 2×1 Mux with a and b as select inputs

C a syntactically wrong code

D a logically wrong code

8 Which flip flop is preferred for counting?

4 Marks

A D flip flop

B JK flip flop

C both of them

D None of them

9 Compared to asynchronous ripple counter, synchronous counters are

4 Marks

A slower

B faster

C equal in terms of propagation delay

D can't be said

10 Consider two negative edge triggered JK flip flops - FF1 and FF2. The input of FF1 are represented by J_1 and K_1, whereas the outputs of FF1 are represented by Q_1 and Q_1'. Similarly, the input of FF2 are represented by J_2 and K_2, whereas the outputs of FF2 are represented by Q_2 and Q_2'. Now, if output terminal Q_1' is connected with the clock input of FF2 and clock signal is applied in the clock input of FF1 then what sequence Q_2Q_1 will generate after each negative clock pulse, assuming that initial state was 00 and J_1, K_1, J_2 and K_2 are all connected with logic 1 input?

4 Marks

A $00, 01, 10, 11, 00, \ldots$

B $00, 11, 10, 01, 00, \ldots$

C $00, 01, 10, 00, \ldots$

D $00, 11, 00, 11, \ldots$

11 Minimize the following Boolean function using Quine-McCluskey (QM) method. Clearly identify the essential prime implicants during this minimization process

$f(A, B, C, D, E) = \sum m(0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)$

10 Marks

12 Construct one SR flip flop from a D flip flop. Show the conversion table, derive the logical expression for D input and obtain the final circuit diagram. The details of D flip flop circuit is not required to be drawn.

4+3+3=10 Marks

13 Design a 4 bit parallel in, serial out shift register using D flip flops.

10 Marks

14 A synchronous sequential circuit has two JK flip flops A and B, two inputs x and y and one output z. The flip flop input equations and circuit output equations are

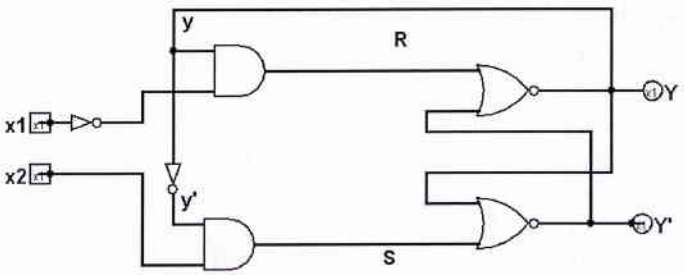
$J_A = Bx + B'y'$, $K_A = B'xy'$
$J_B = A'x$, $K_B = A + xy'$
$z = Ax'y' + Bx'y'$

i Draw the logic diagram of the circuit

ii Tabulate the state table and state diagram of the circuit

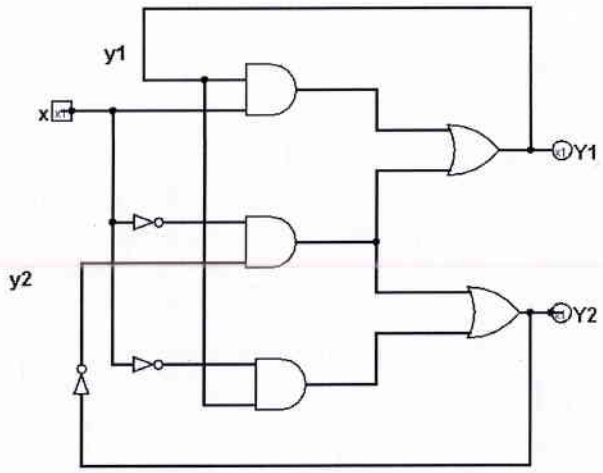
5+5= 10 Marks

15 Consider the following circuit using SR NOR latch. Obtain the transition table corresponding to this circuit. $S = 1$ and $R = 1$ must be avoided.



10 Marks

16 Consider the asynchronous sequential circuit diagram shown in the following figure.



(a) If y_1y_2x represents a total state then construct the Transition Table corresponding to this circuit.

(b) Check in this circuit whether there is any race condition. If yes then determine whether the condition is critical or non-critical.

$(5 + 5) = 10$ Marks