Tutorial 8

1. Design a combinational circuit with three inputs and one output.

a) The output is 1 when the binary value of the inputs is less than or equal to 3. The output is 0 otherwise.

b) The output is 1 when the binary value of the inputs is an odd number.

2. Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.

3. Design a combinational circuit that converts a four-bit Gray code to a four-bit binary number. Implement the circuit with exclusive-OR gates.

4. Using four half adders,

(a) Design a four-bit combinational circuit incrementer (a circuit that adds 1 to a four-bit binary number).

(b) Design a four-bit combinational circuit decrementer (a circuit that subtracts 1 from a four-bit binary number).

5. a. Design a combinational circuit that generates the 9's complement of BCD Digit.

b**.** Construct a BCD adder-subtractor circuit. Use the BCD adder of Fig. (1) and the 9's complementer of Problem 5(a). Use block diagrams for the components.

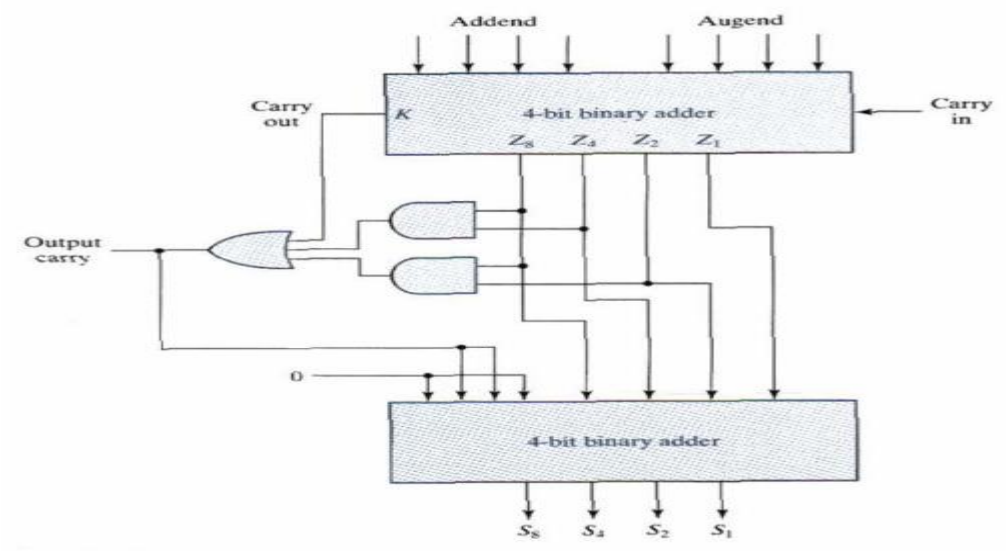

Fig. (1) Block diagram of BCD adder.

6. Draw the logic diagram of a two-to-four-line decoder using (a) NOR gates only, and (b) NAND gates only. Include an enable input. Suggest circuit changes to part (b) that produce active high outputs.

7. Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4-line decoder. Use block diagrams for the components.

8. Implement a full subtractor with a decoder and NAND gates. The subtractor inputs are A, B, and C. The subtractor produces outputs D and B0.

9. Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

(a) $F_1 = (y' + x)z$

(b) $F_2 = y'z' + xy' + yz'$

(c) $F_3 = (x' + y)z$

10. Design a four-input priority encoder with inputs as in Table given below, but with input D0 having the highest priority and input D3 the lowest priority.

Inputs				Outputs		
D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1