Design Overview

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Power Connector

General Conventions:

Signal names beginning with a '/' are active low

Directive ▼ indicates that after reviewing the design, the "No Driving Source" warning is suppressed on this pin

Unless Specified Otherwise:

All resistors are 1% metal film, 0201 (1/20W), 0402 (1/16W) or 0603 (1/10W)

All non-polarized capacitors are ceramic

All ceramic capacitors up to and including 1,000pF are NPO, 25V or higher, 5% or better

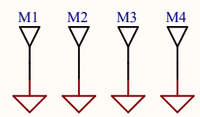
All ceramic capacitors over 1,000pF up to and including 1.0uF are X7R, 16V or higher, 10% or better

All ceramic capacitors over 1.0uF up to and including 10uF are X5R or better, 10V or higher, 20% or better

All ceramic capacitors over 10uF are of type X5R or better and the specified voltage, 20% or better

All polarized capacitors are Organic Tantalum, of the specified manufacturer/family and voltage, 20% or better

Mounting Holes



Title: *IEEE-1394/Ethernet FPGA Controller*		
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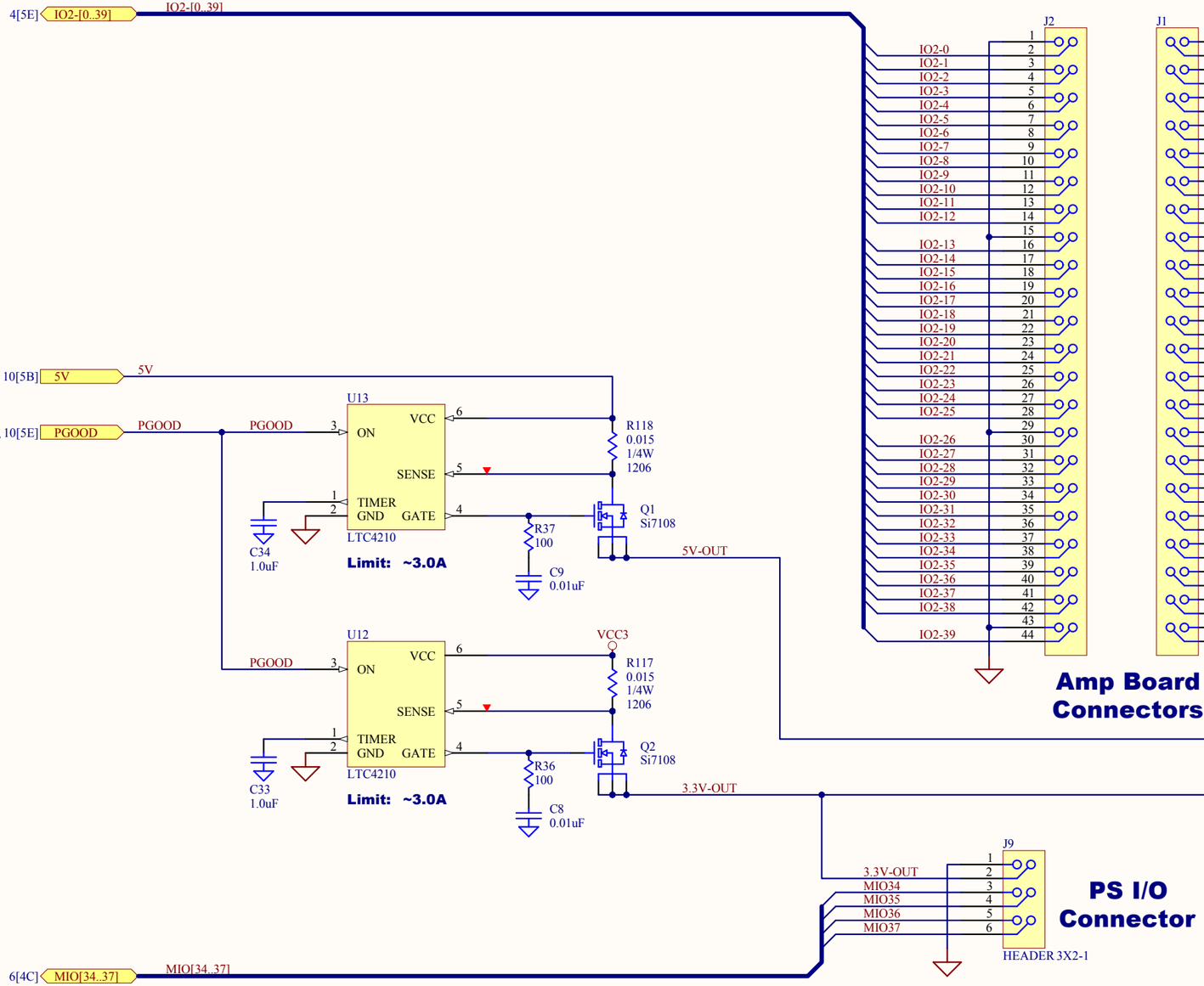
I/O Connectors

4[5E] IO1-[0..33] — IO1-[0..33]

4[5E] IO2-[0..39] — IO2-[0..39]



Amp Board Connectors

PS I/O Connector

6[4C] MIO[34..37] — MIO[34..37]

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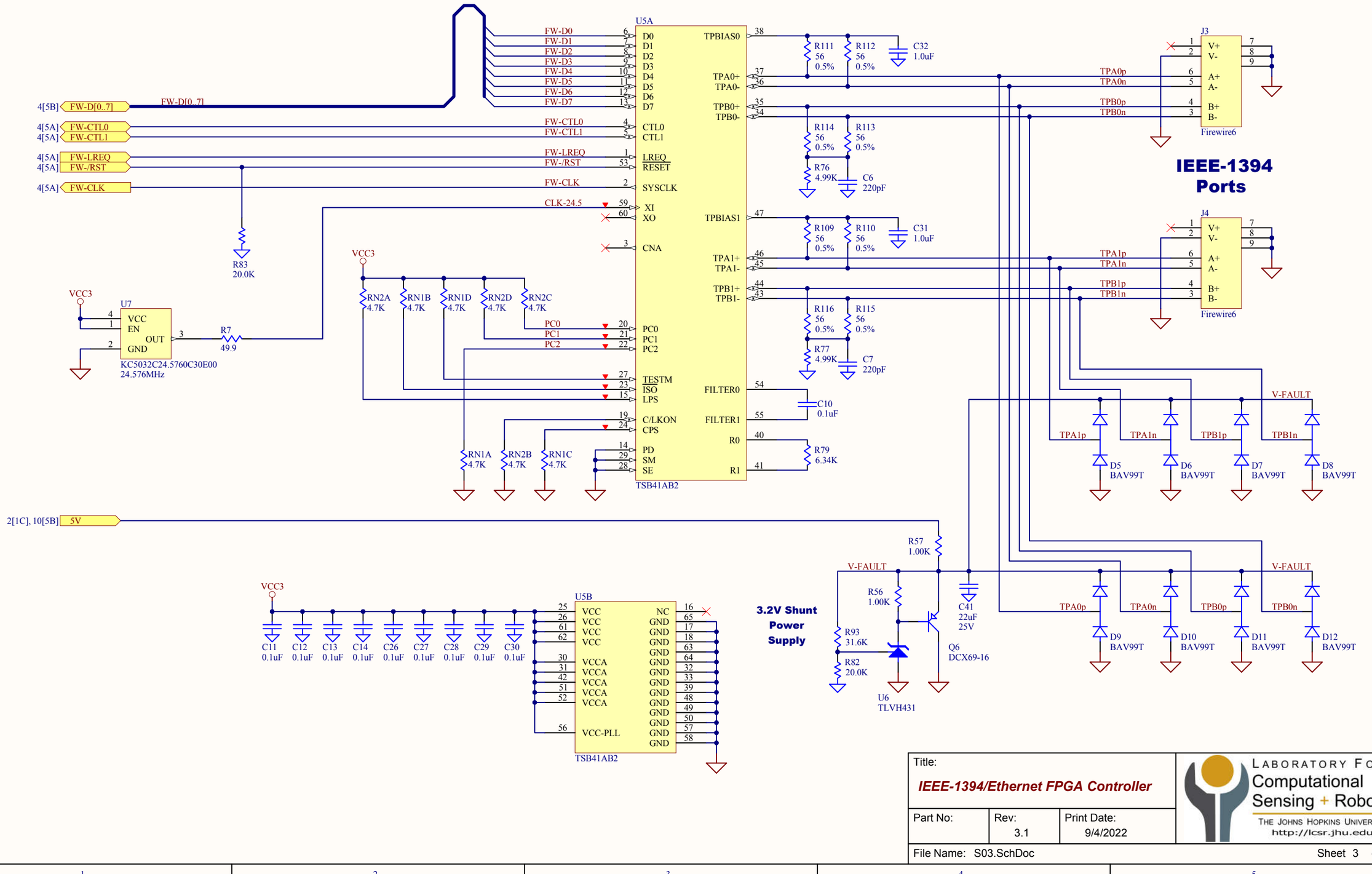
FireWire Controller & Connectors



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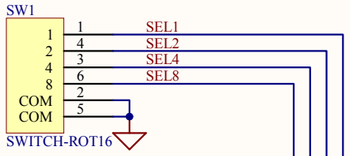
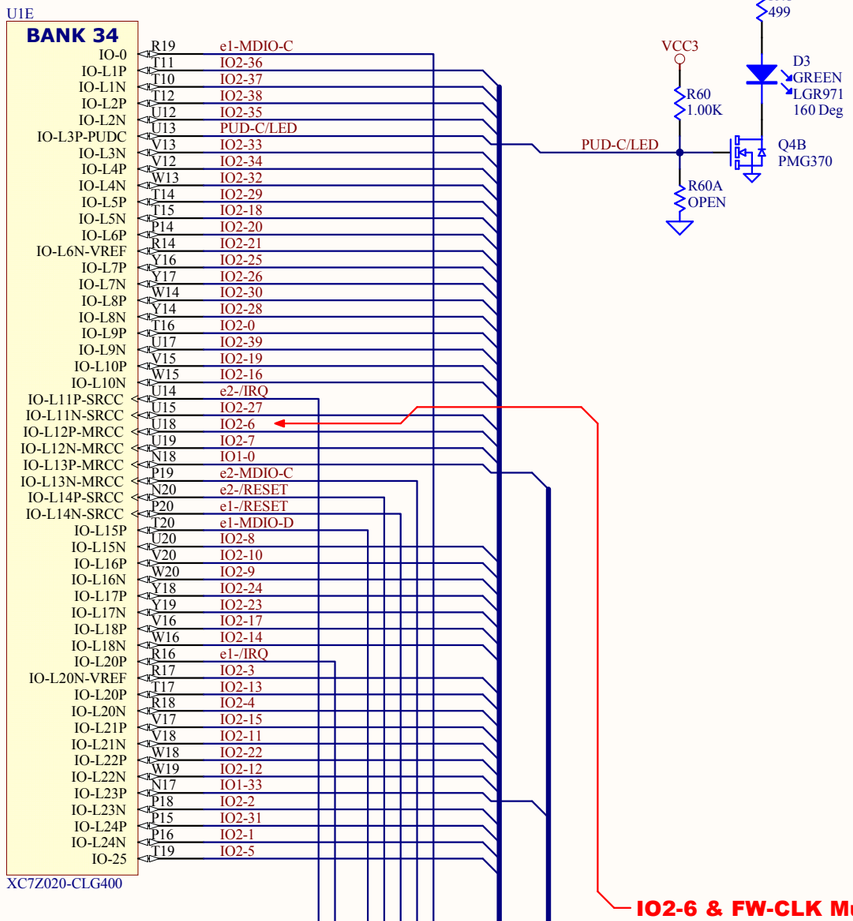
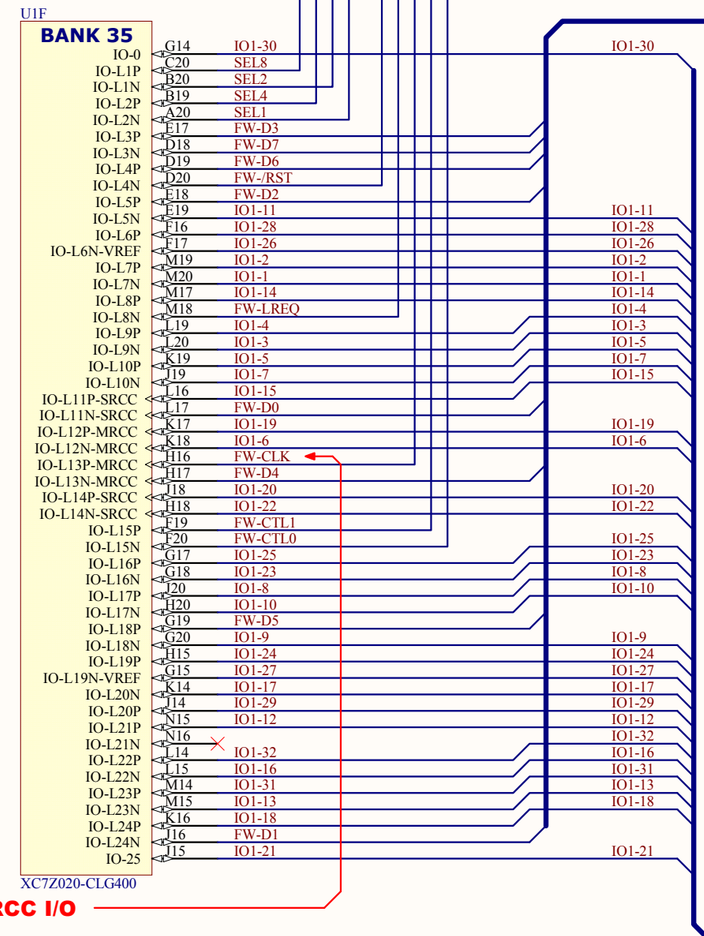
PL Generic I/O

Board ID







IO2-6 & FW-CLK Must Be On MRCC I/O

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File Name: S04.SchDoc

PL Ethernet Ports

e1-RxCLK & e2-RxCLK Must Be On MRCC I/O

U1D
BANK 13
XC7Z020-CLG400

IO-L6N-VREF	V5		e2-RxD0
IO-L11P-SRCC	U7		e2-TxEN
IO-L11N-SRCC	V7		e2-RxD3
IO-L12P-MRCC	T9		e2-RxCLK
IO-L12N-MRCC	U10		e2-TxD3
IO-L13P-MRCC	Y7		e1-RxCLK
IO-L13N-MRCC	Y6	R2 49.9	e2-TxCLK
IO-L14P-SRCC	Y9		e1-RxD2
IO-L14N-SRCC	Y8		e1-RxD0
IO-L15P	V8		e1-RxVAL
IO-L15N	W8		e1-RxD1
IO-L16P	W10		e1-TxEN
IO-L16N	W9		e1-RxD3
IO-L17P	U9		e2-TxD1
IO-L17N	U8		e2-TxD0
IO-L18P	W11		e1-TxD1
IO-L18N	Y11		e1-TxD0
IO-L19P	T5		e2-RxVAL
IO-L19N-VREF	U5		e2-RxD2
IO-L20P	Y12		e1-TxD2
IO-L20N	Y13		e1-TxD3
IO-L21P	V11	R1 49.9	e1-TxCLK
IO-L21N	V10		e2-TxD2
IO-L22P	V6		e2-RxD1
IO-L22N	W6		e2-MDIO-D/1.8

4[5E] e1-/IRQ → e1-/IRQ
4[5E] e1-/RESET → e1-/RESET

VCC3, 1.8V
U8 TXS0101
4[5E] e1-MDIO-D → e1-MDIO-D → e1-MDIO-D/1.8
CB70 0.1uF, CB71 0.1uF, CB72 0.1uF

U9 74AUP2G17
4[5E] e1-MDIO-C → e1-MDIO-C → e1-MDIO-C/1.8
4[5E] e2-MDIO-C → e2-MDIO-C → e2-MDIO-C/1.8

4[5F] e2-/IRQ → e2-/IRQ
4[5E] e2-/RESET → e2-/RESET

U19 25MHz
CB73 0.1uF
e-CLK25 → R38 100 → e1-CLK25
e-CLK25 → R39 100 → e2-CLK25

1.8V
R62 1.50K
R63 1.50K

U10A RTL8211F

e1-TxCLK	20	TX-CLK	
e1-TxD0	18	TXD0	
e1-TxD1	17	TXD1	
e1-TxD2	16	TXD2	
e1-TxD3	15	TXD3	
e1-TxEN	19	TX-EN	
e1-RxCLK R3	27	RX-CLK	
e1-RxD0 49.9	25	RXD0	
e1-RxD1	24	RXD1	
e1-RxD2	23	RXD2	
e1-RxD3	22	RXD3	
e1-RxVAL	26	RX-VALID	
e1-MDIO-D/1.8	14	MDIO	
e1-MDIO-C/1.8	13	MDC	
e1-/IRQ	31	INTR	
e1-/RESET	12	RESET	
	35	CLKOUT	
	39	RBIAS	
e1-CLK25	37	XO	
	36	XI	

Tx/Rx-A+	1	ETH1-A+
Tx/Rx-A-	2	ETH1-A-
Tx/Rx-B+	4	ETH1-B+
Tx/Rx-B-	5	ETH1-B-
Tx/Rx-C+	6	ETH1-C+
Tx/Rx-C-	7	ETH1-C-
Tx/Rx-D+	9	ETH1-D+
Tx/Rx-D-	10	ETH1-D-
LED0-10	32	
/LED1-100	33	e1-LED1
LED2-1000	34	e1-LED2

R58 1.00K, R65 2.49K, R59 1.00K, R66 2.49K

VCC3
R43 240 → e1-LED1
R42 240 → e1-LED2
R41 240 → e2-LED1
R40 240 → e2-LED2

DIFF100

J8A RJ-45-2-TRANSFORMER-PULSE

1A	10A	NC
		SHIELD
		SHIELD
2A	3A	ETH1-A+ / ETH1-A-
4A	5A	ETH1-B+ / ETH1-B-
6A	7A	ETH1-C+ / ETH1-C-
8A	9A	ETH1-D+ / ETH1-D-
11A	13A	Y / G
14A	12A	

U11A RTL8211F

e2-TxCLK	20	TX-CLK	
e2-TxD0	18	TXD0	
e2-TxD1	17	TXD1	
e2-TxD2	16	TXD2	
e2-TxD3	15	TXD3	
e2-TxEN	19	TX-EN	
e2-RxCLK R4	27	RX-CLK	
e2-RxD0 49.9	25	RXD0	
e2-RxD1	24	RXD1	
e2-RxD2	23	RXD2	
e2-RxD3	22	RXD3	
e2-RxVAL	26	RX-VALID	
e2-MDIO-D/1.8	14	MDIO	
e2-MDIO-C/1.8	13	MDC	
e2-/IRQ	31	INTR	
e2-/RESET	12	RESET	
	35	CLKOUT	
	39	RBIAS	
e2-CLK25	37	XO	
	36	XI	

Tx/Rx-A+	1	ETH2-A+
Tx/Rx-A-	2	ETH2-A-
Tx/Rx-B+	4	ETH2-B+
Tx/Rx-B-	5	ETH2-B-
Tx/Rx-C+	6	ETH2-C+
Tx/Rx-C-	7	ETH2-C-
Tx/Rx-D+	9	ETH2-D+
Tx/Rx-D-	10	ETH2-D-
LED0-10	32	
/LED1-100	33	e2-LED1
LED2-1000	34	e2-LED2

R59 1.00K, R66 2.49K

J8B RJ-45-2-TRANSFORMER-PULSE

1B	10B	NC
		SHIELD
2B	3B	ETH2-A+ / ETH2-A-
4B	5B	ETH2-B+ / ETH2-B-
6B	7B	ETH2-C+ / ETH2-C-
8B	9B	ETH2-D+ / ETH2-D-
11B	13B	Y / G
14B	12B	

R68 4.99K [34] e1-LED2
R69 4.99K [33] e1-LED1
R70 4.99K [34] e2-LED2
R71 4.99K [33] e2-LED1

Pin	Name	Default Value	Config. Value	Description
22	PHYAD0	1		001 => PHY Address 001
27	PHYAD1	0		
26	PHYAD2	0		
23	PLLOFF	0		PLL always on
24	TXDLY	0		TxC Not Delayed
25	RXDLY	1		RxC Delayed by 2ns
32	CFG-EXT	0		Internal LDO for I/O pins
33	LOD0	1	0	10 => 1.8V
34	LDO1	0	1	

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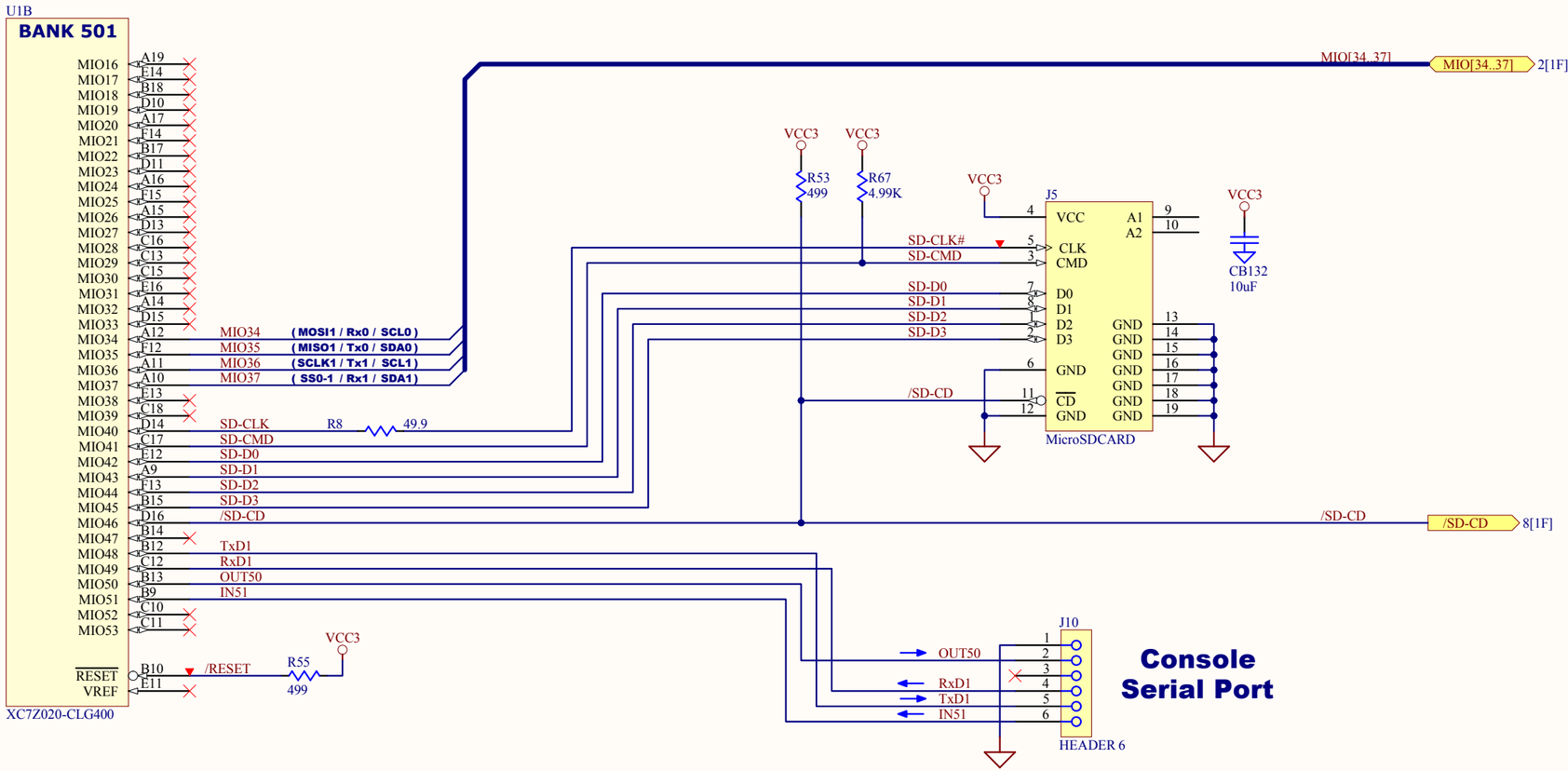
PS Micro-SD & Console



Title: *IEEE-1394/Ethernet FPGA Controller*		
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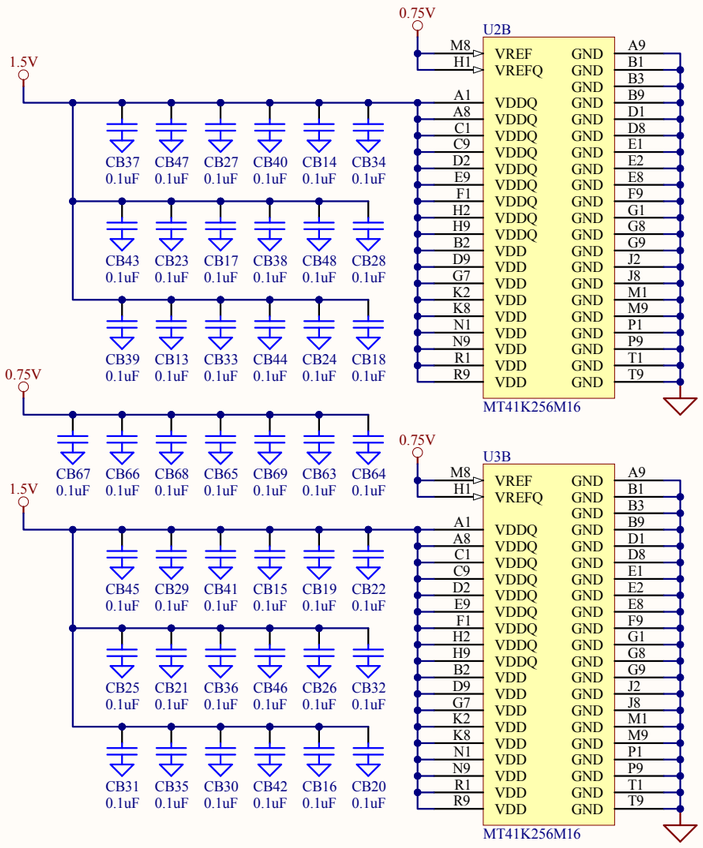
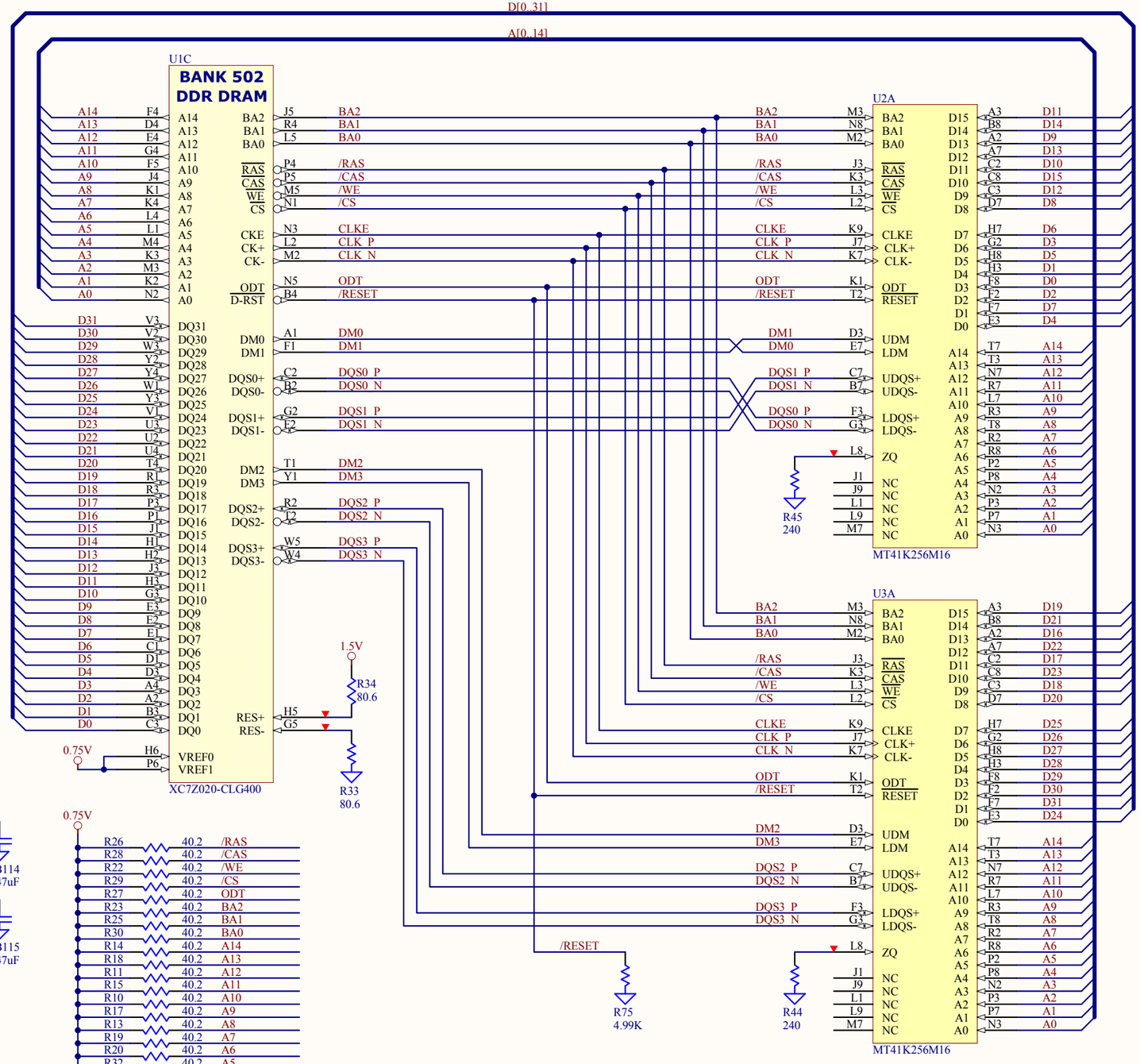
PS DRAM

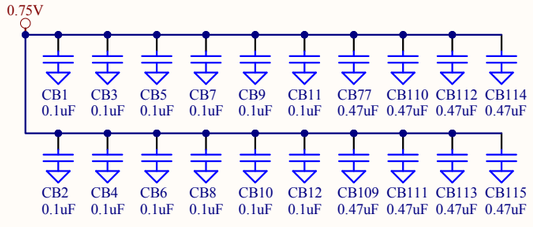


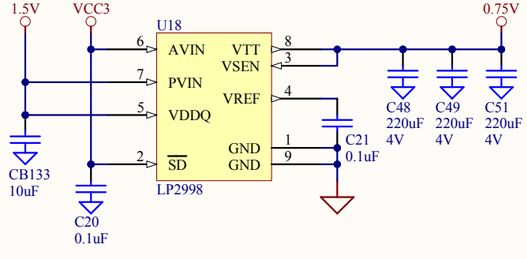


Note:

The 0.75V plane is used as a reference plane for routing DRAM signals.

The plane itself requires bypass caps to AC couple it to the ground planes.





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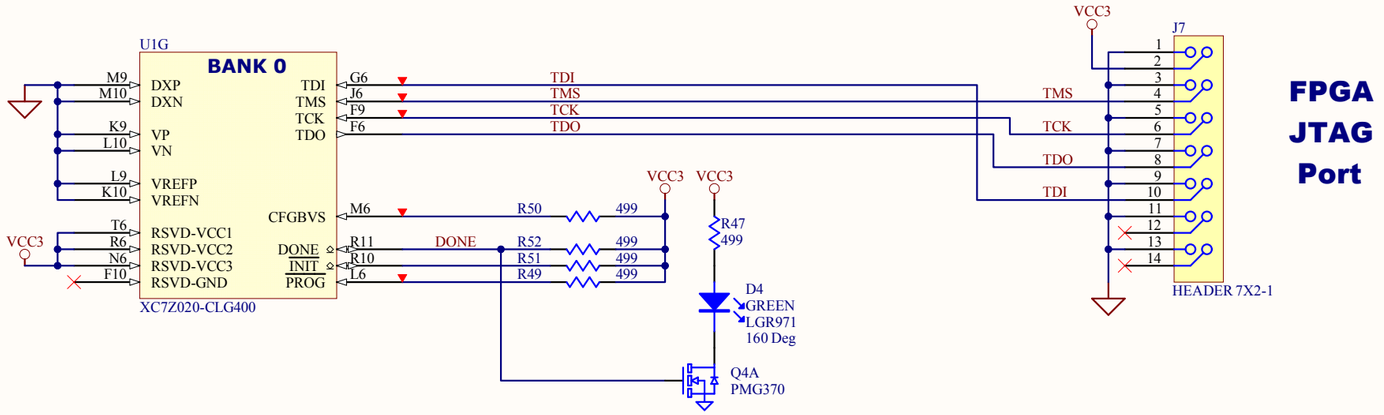
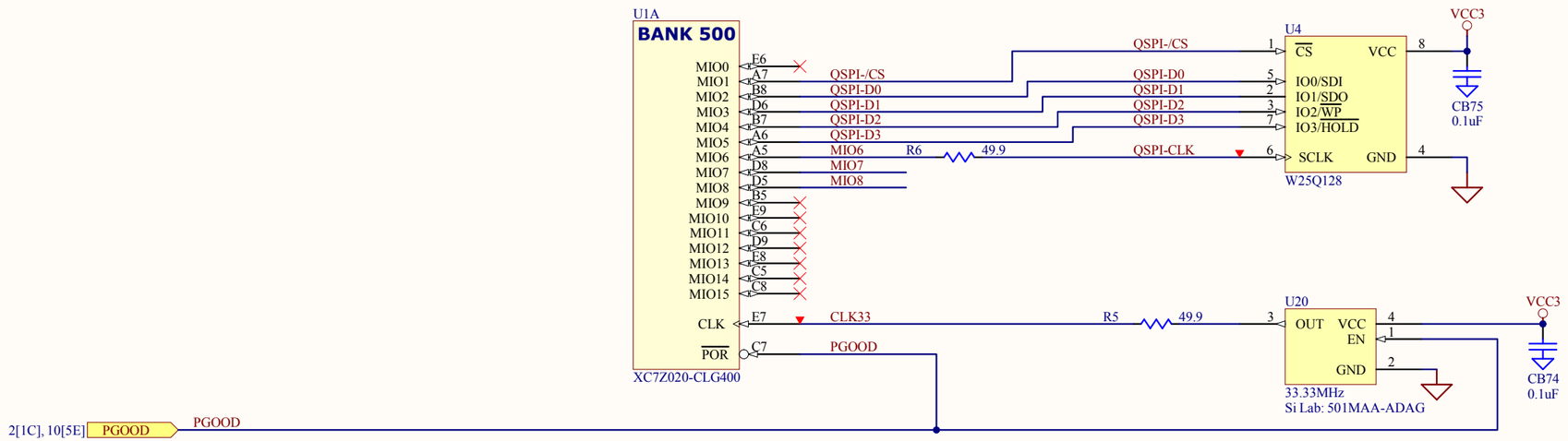
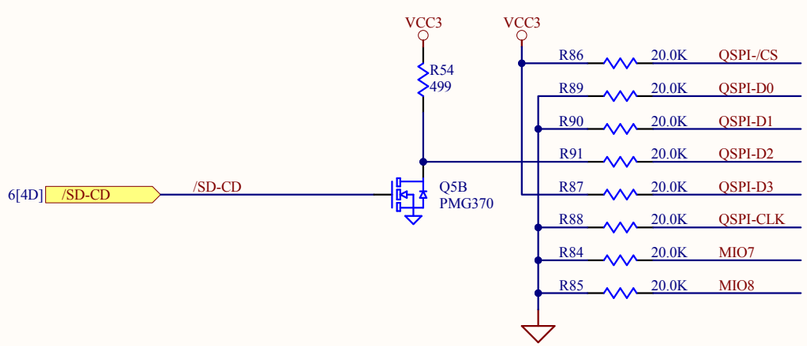
PS Boot & JTAG







Boot Options

MIO	Name	Signal	Value	Description
2	BOOT[3]	QSPI-D0	0	JTAG: Cascade Mode
3	BOOT[1]	QSPI-D1	0	000: JTAG
4	BOOT[2]	QSPI-D2	0/1	100: QSPI
5	BOOT[0]	QSPI-D3	1	110: uSD Card
6	BOOT[4]	QSPI-CLK	0	PLL Enabled
7	VMODE[0]	MIO7	0	Bank 500: 3.3V
8	VMODE[1]	MIO8	0	Bank 501: 3.3V

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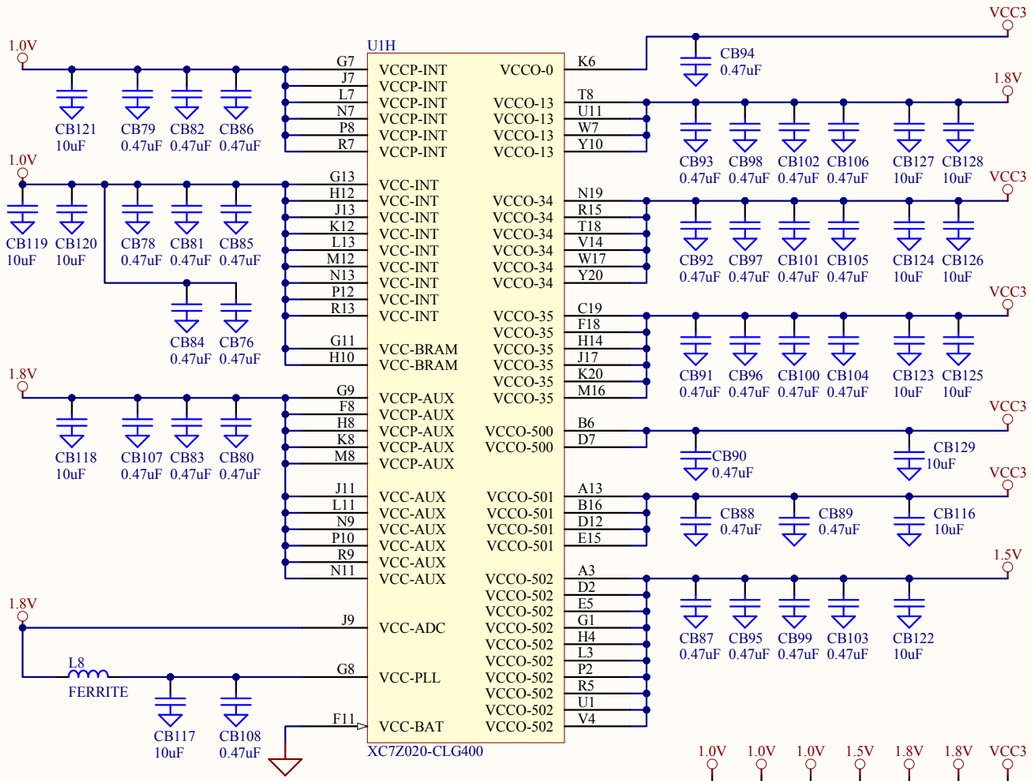
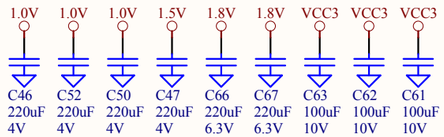
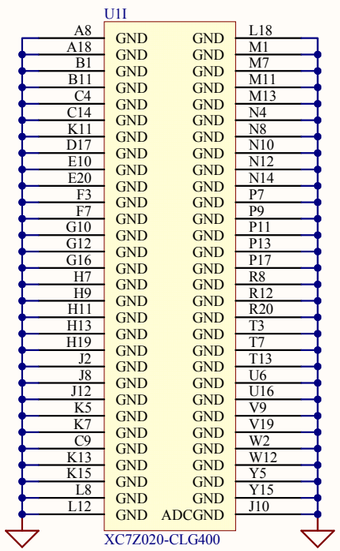
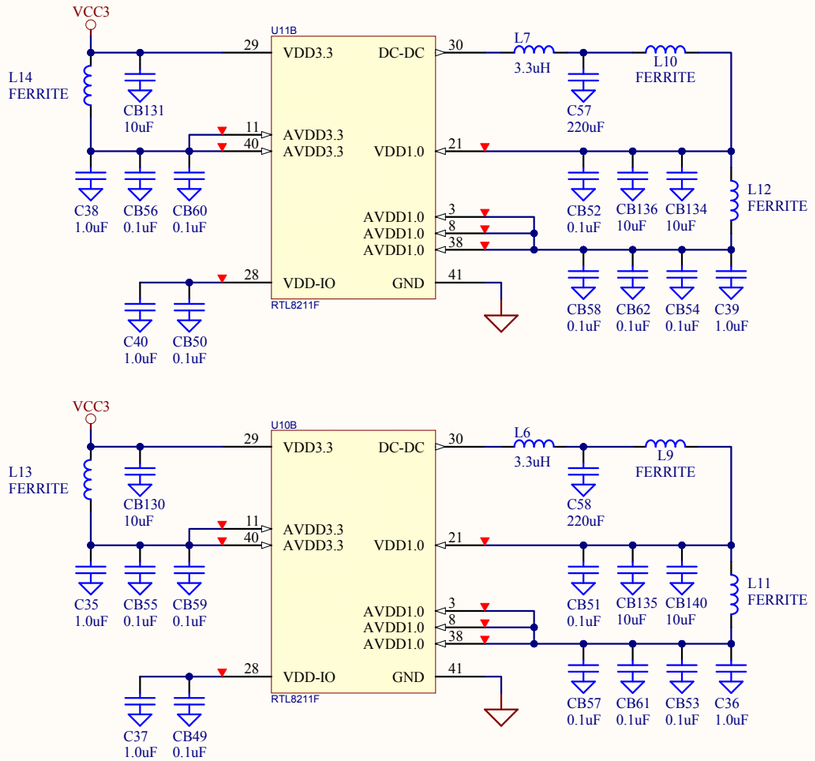
File Name: S08.SchDoc

Power Pins









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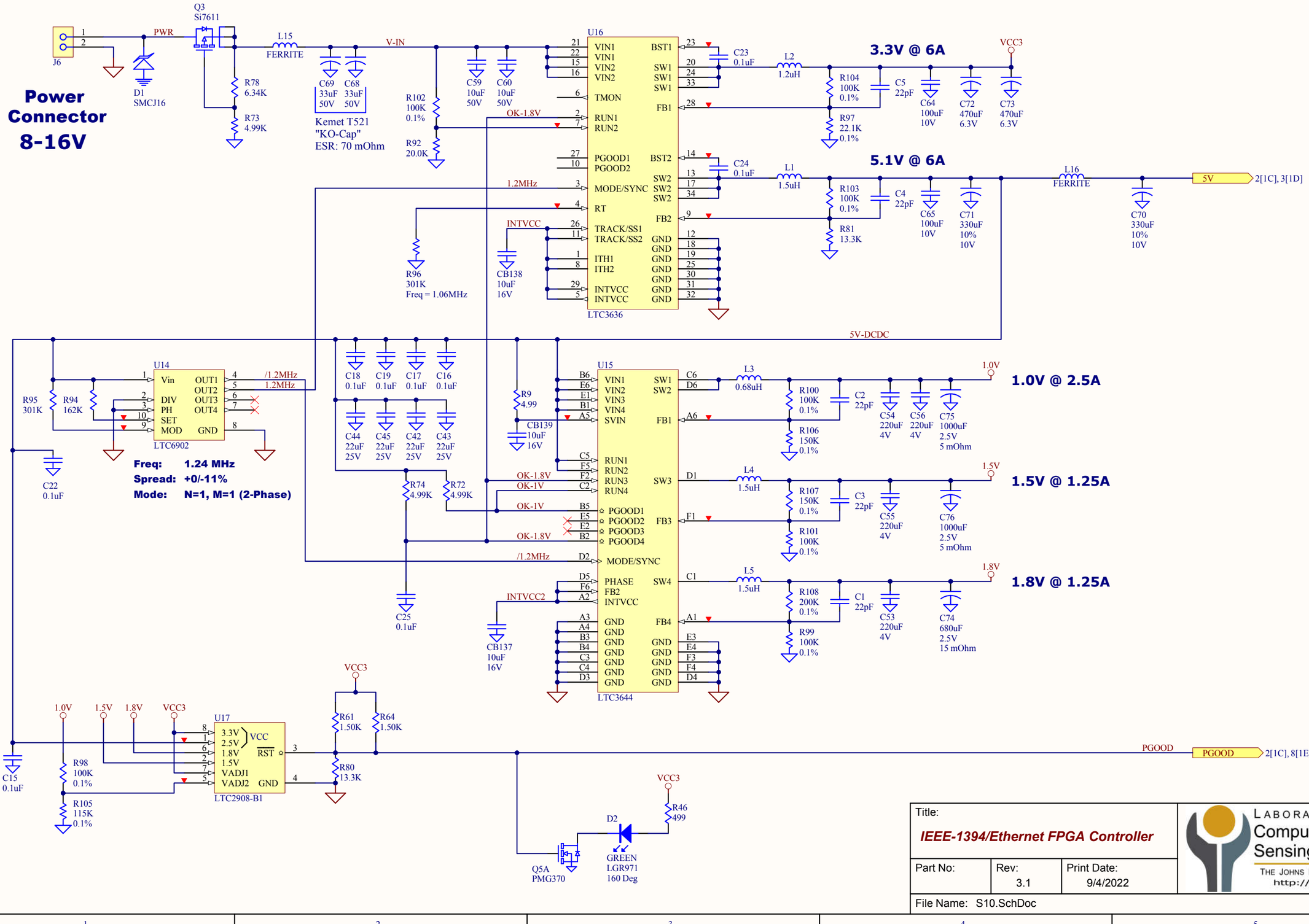
Power Supplies



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