Design Overview

General Conventions:

Signal names beginning with a '/' are active low

Directive ▼ indicates that after reviewing the design, the "No Driving Source" warning is suppressed on this pin

Unless Specified Otherwise:

All resistors are 1% metal film, 0201 (1/20W), 0402 (1/16W) or 0603 (1/10W)

All non-polarized capacitors are ceramic

All ceramic capacitors up to and including 1,000pF are NPO, 25V or higher, 5% or better

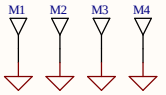
All ceramic capacitors over 1,000pF up to and including 1.0uF are X7R, 16V or higher, 10% or better

All ceramic capacitors over 1.0uF up to and including 10uF are X5R or better, 10V or higher, 20% or better

All ceramic capacitors over 10uF are of type X5R or better and the specified voltage, 20% or better

All polarized capacitors are Organic Tantalum, of the specified manufacturer/family and voltage, 20% or better

Mounting Holes



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Part No:	Rev: 3.1	Print Date: 9/4/2022	
File Name: S01.SchDoc			Sheet 1 of 10

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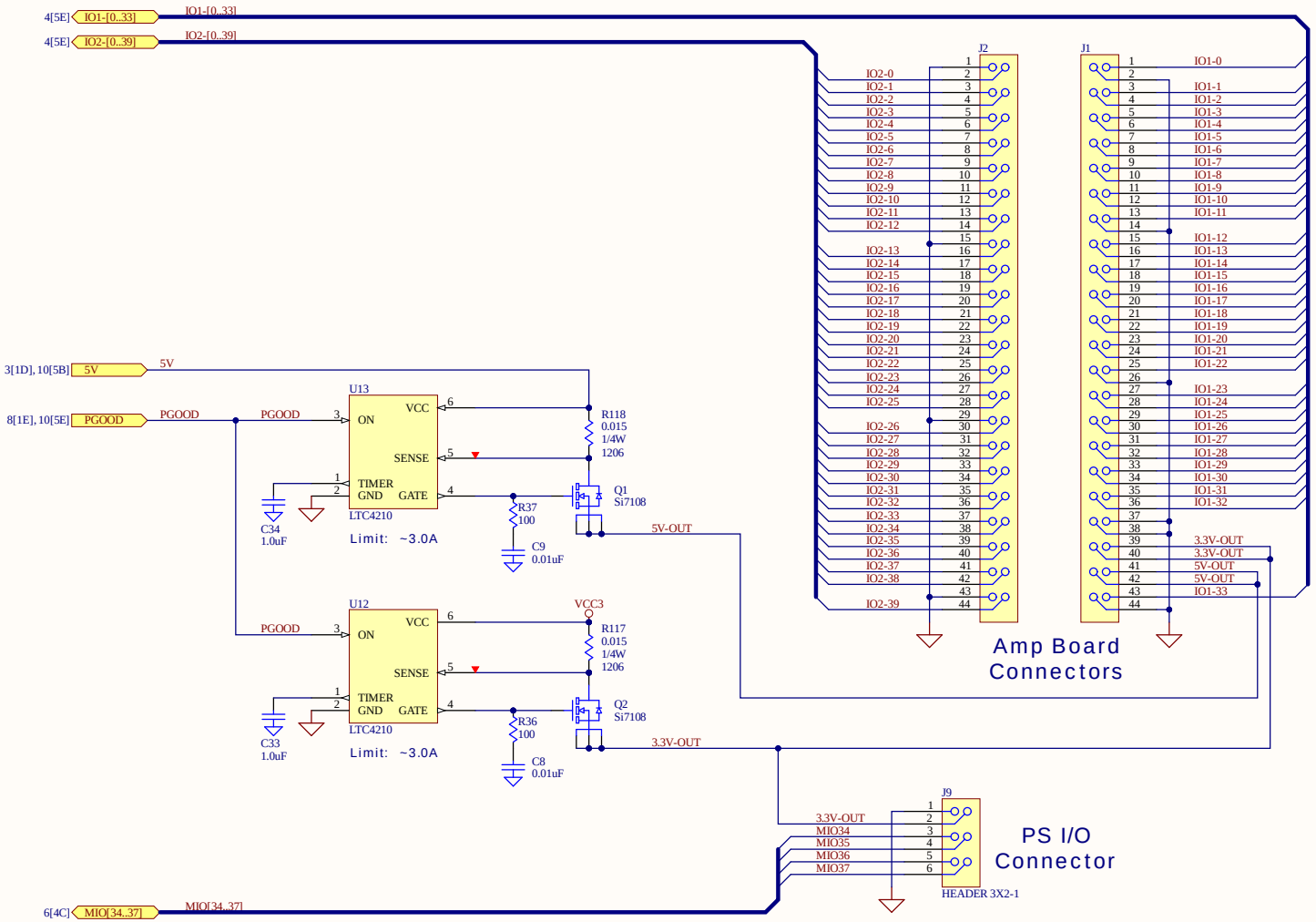
I/O Connectors



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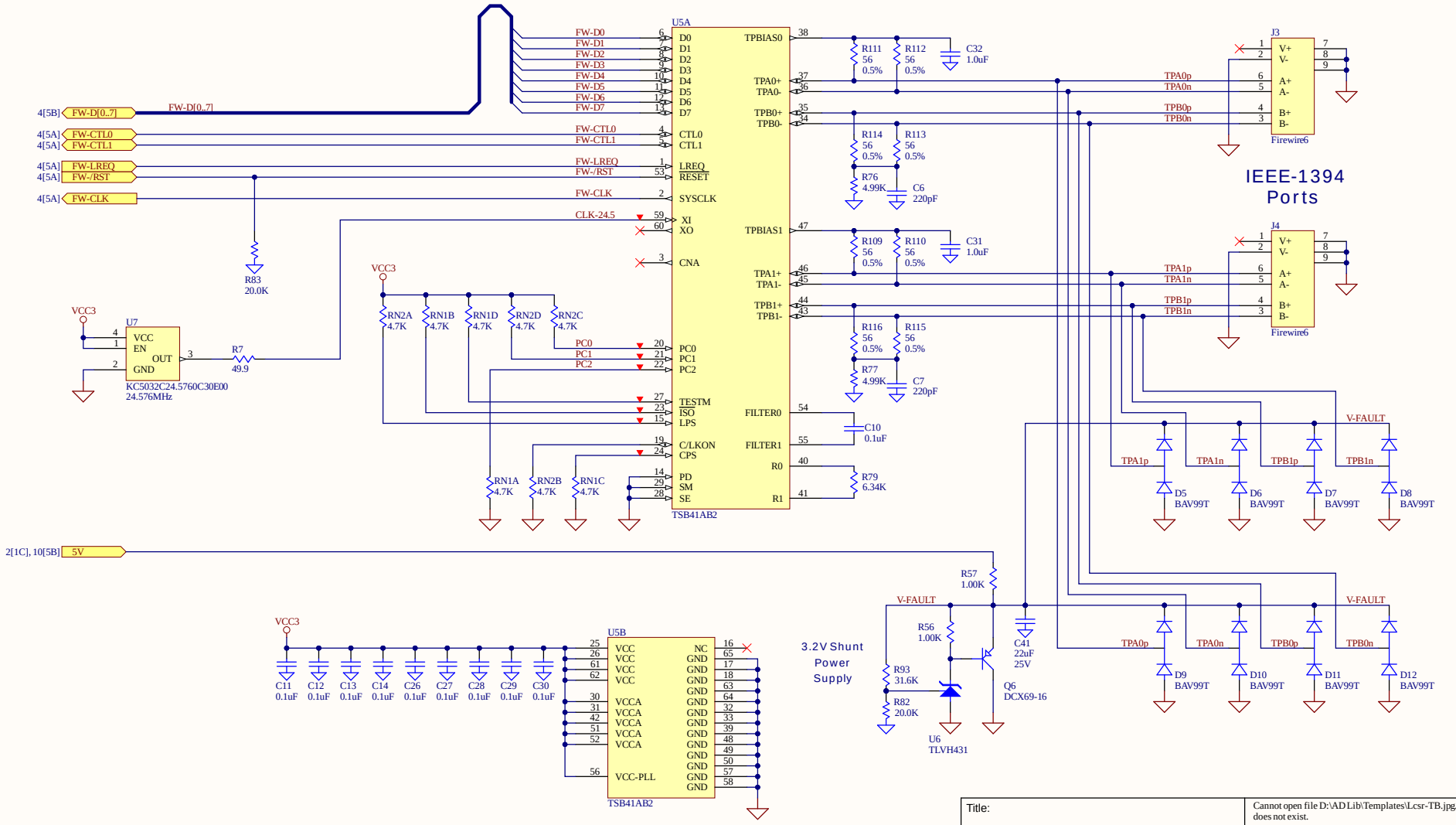
FireWire Controller & Connectors



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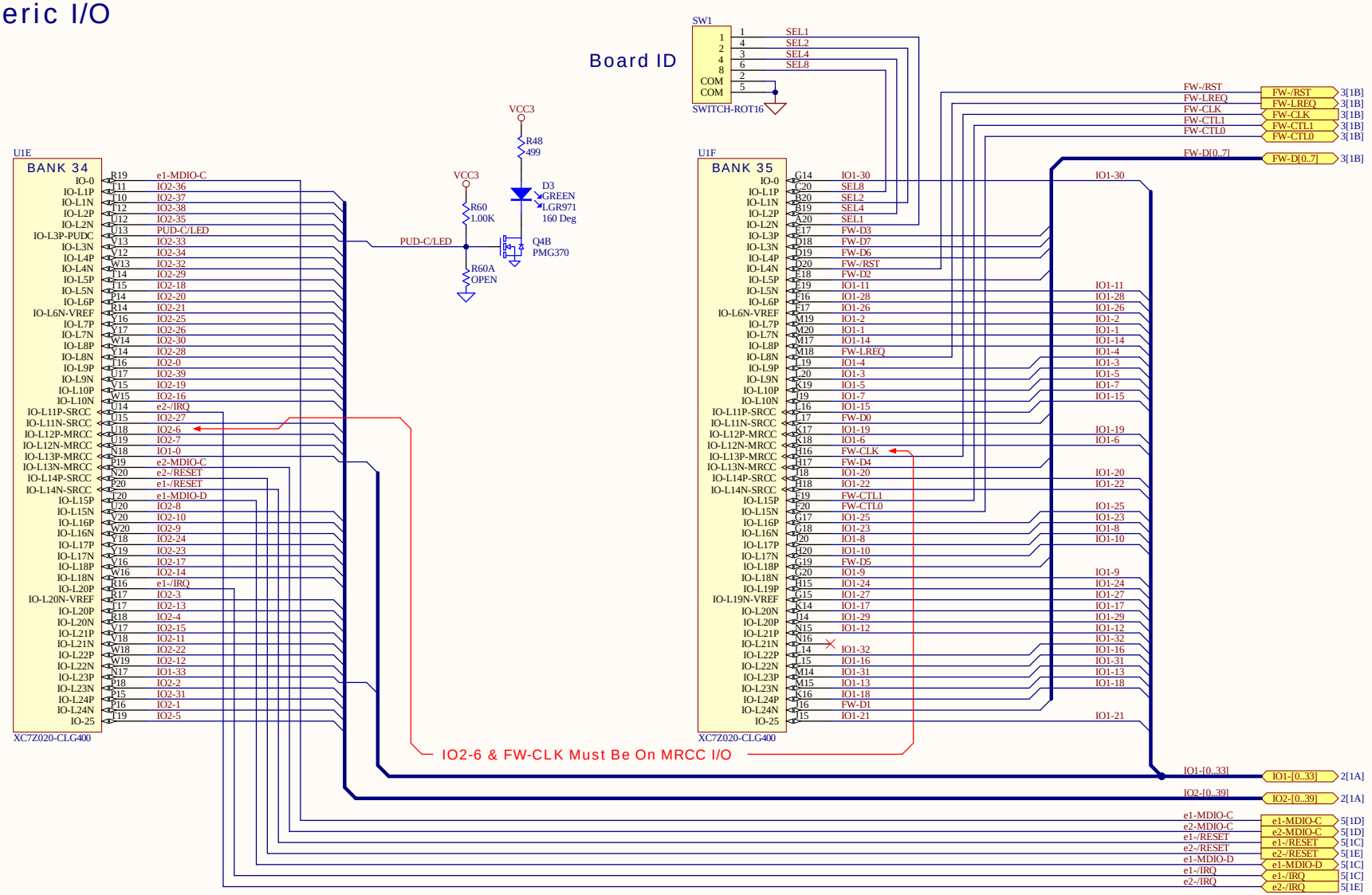
PL Generic I/O



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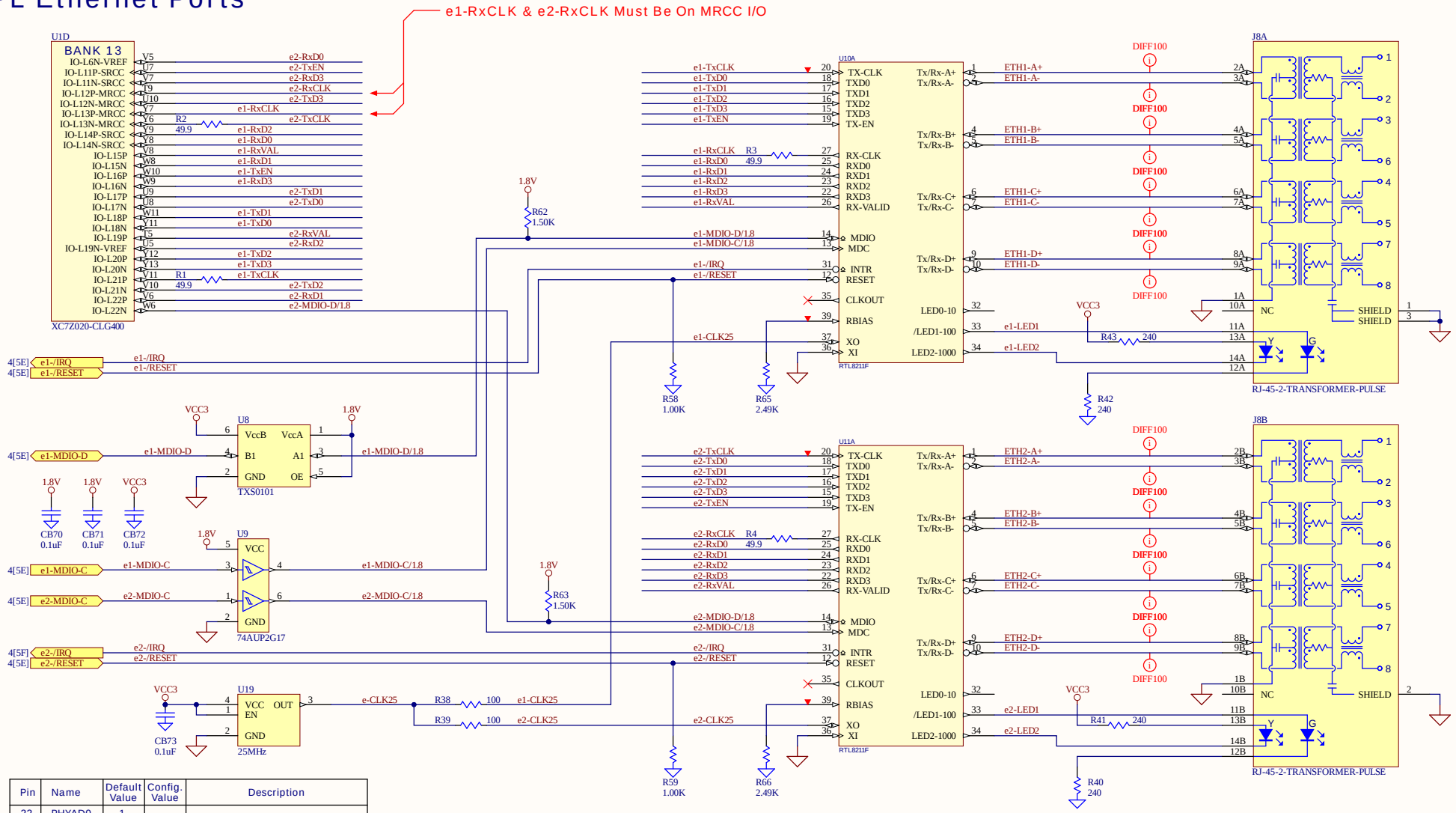
PL Ethernet Ports



Pin	Name	Default Value	Config. Value	Description
22	PHYAD0	1		001 => PHY Address 001
27	PHYAD1	0		
26	PHYAD2	0		
23	PLLOFF	0		PLL always on
24	TXDLY	0		TxC Not Delayed
25	RXDLY	1		RxC Delayed by 2ns
32	CFG-EXT	0		Internal LDO for I/O pins
33	LOD0	1	0	10 => 1.8V
34	LDO1	0	1	

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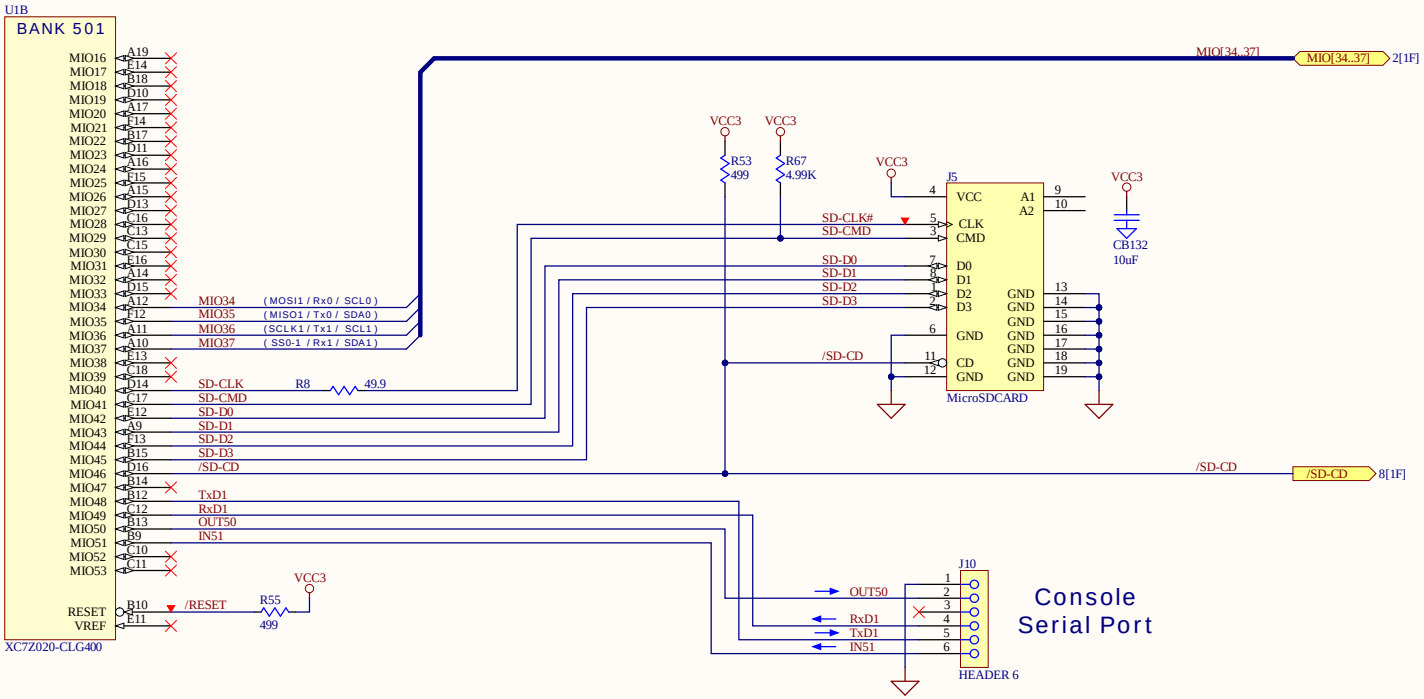
PS Micro-SD & Console



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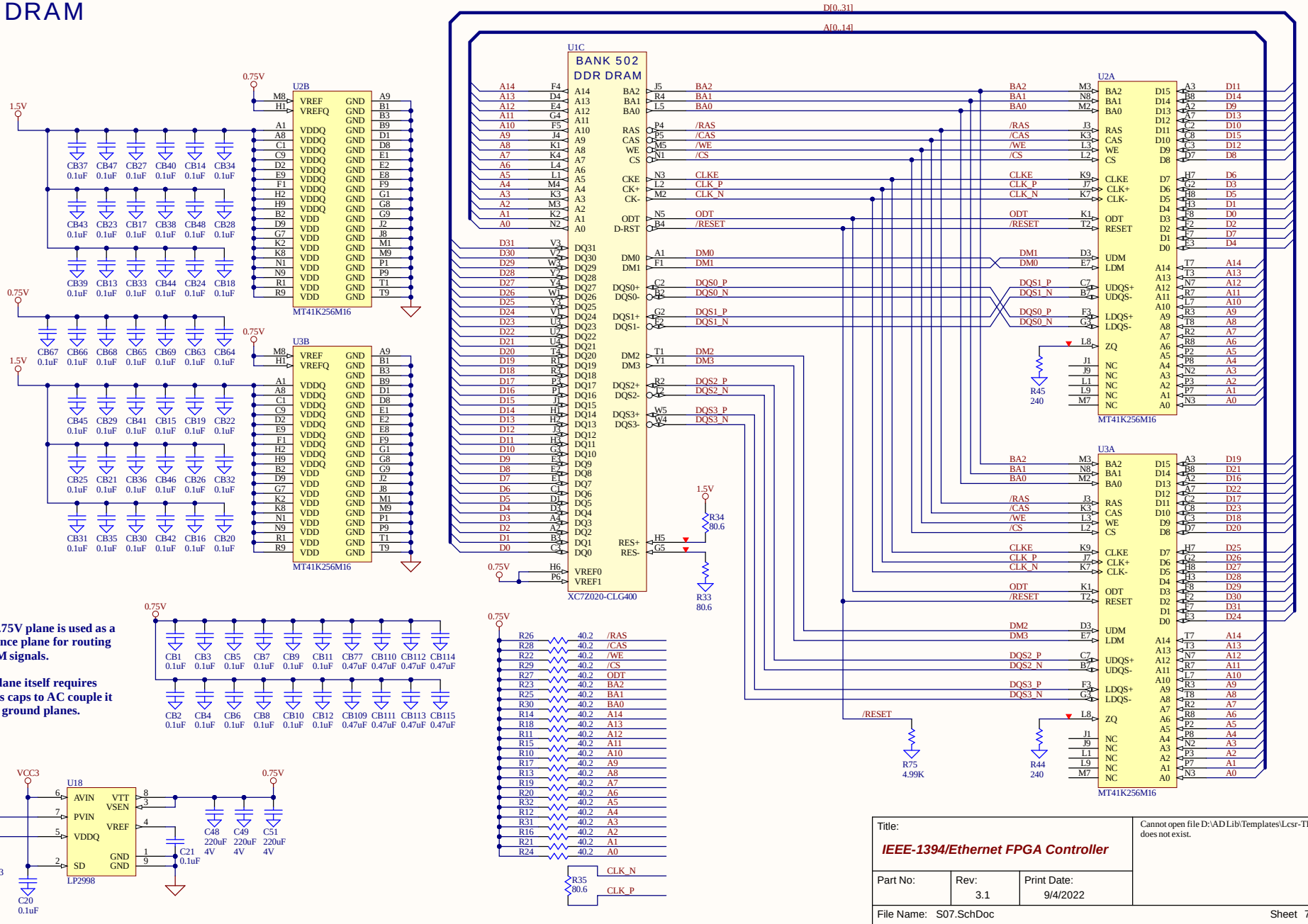
PS DRAM



Note:

The 0.75V plane is used as a reference plane for routing DRAM signals.

The plane itself requires bypass caps to AC couple it to the ground planes.

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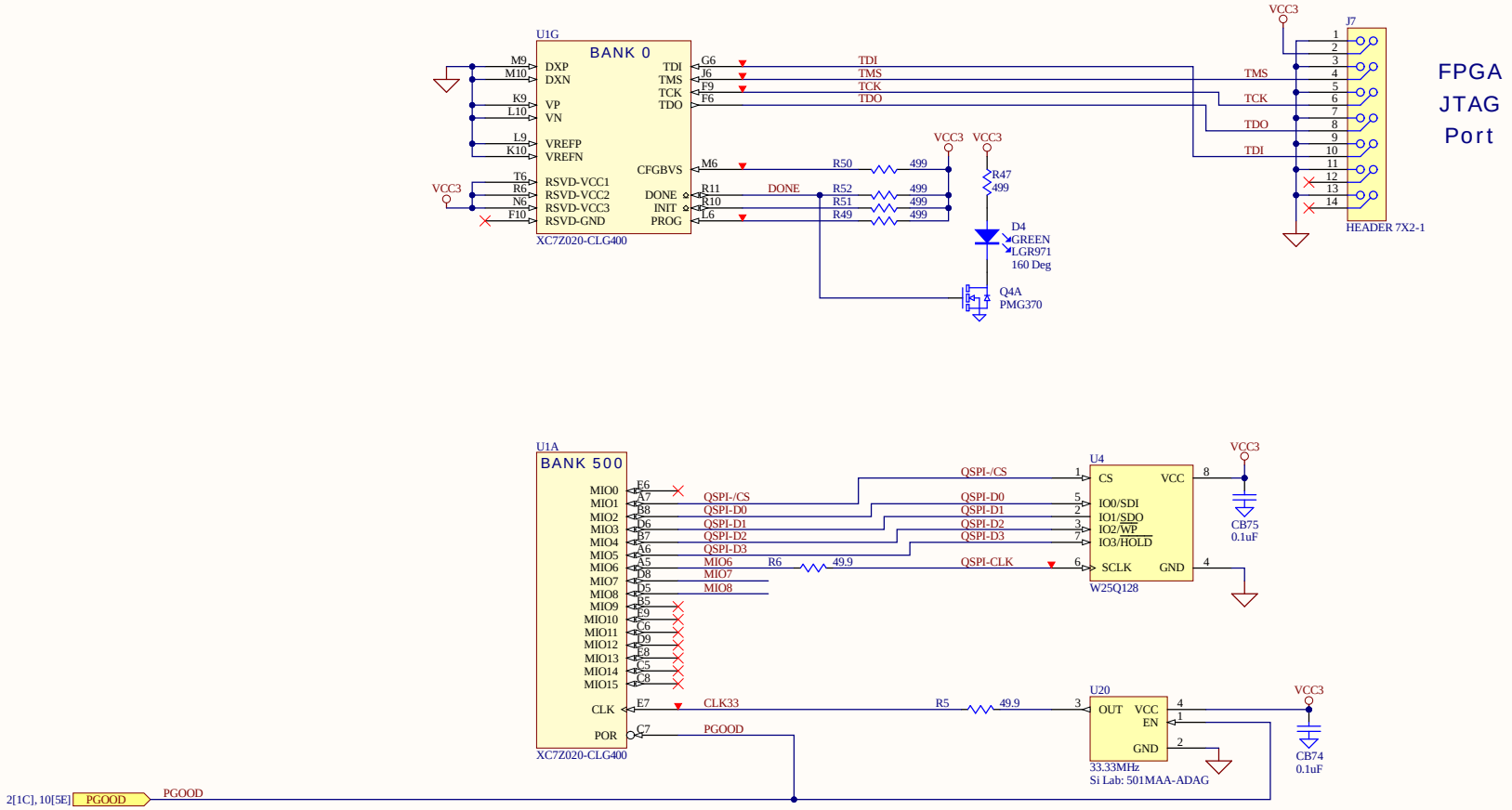
PS Boot & JTAG



Boot Options

MIO	Name	Signal	Value	Description
2	BOOT[3]	QSPI-D0	0	JTAG: Cascade Mode
3	BOOT[1]	QSPI-D1	0	000: JTAG
4	BOOT[2]	QSPI-D2	0/1	100: QSPI
5	BOOT[0]	QSPI-D3	1	110: uSD Card
6	BOOT[4]	QSPI-CLK	0	PLL Enabled
7	VMODE[0]	MIO7	0	Bank 500: 3.3V
8	VMODE[1]	MIO8	0	Bank 501: 3.3V

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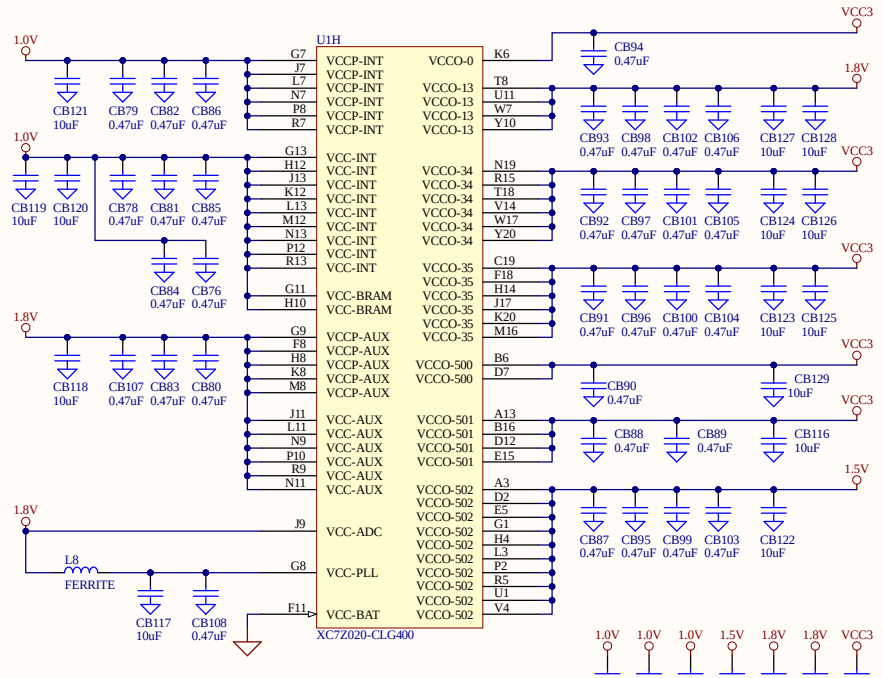
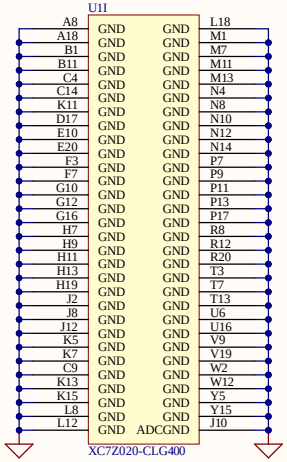
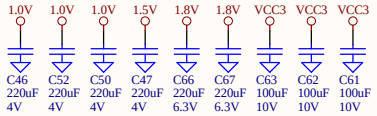
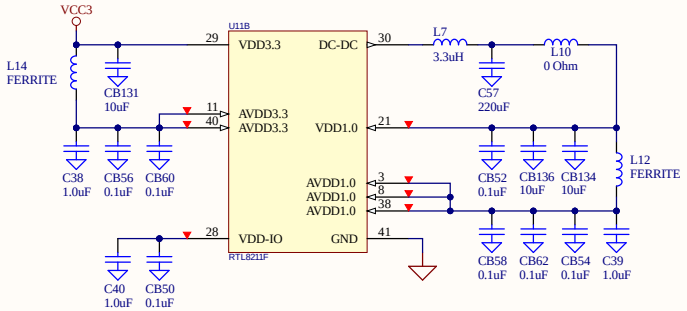
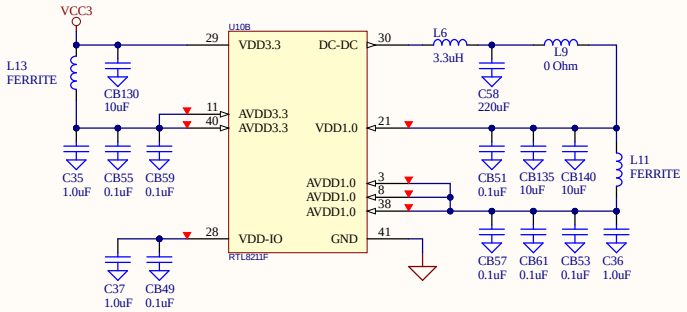
Power Pins











Drawing Title: IEEE-1394/Ethernet FPGA Controller

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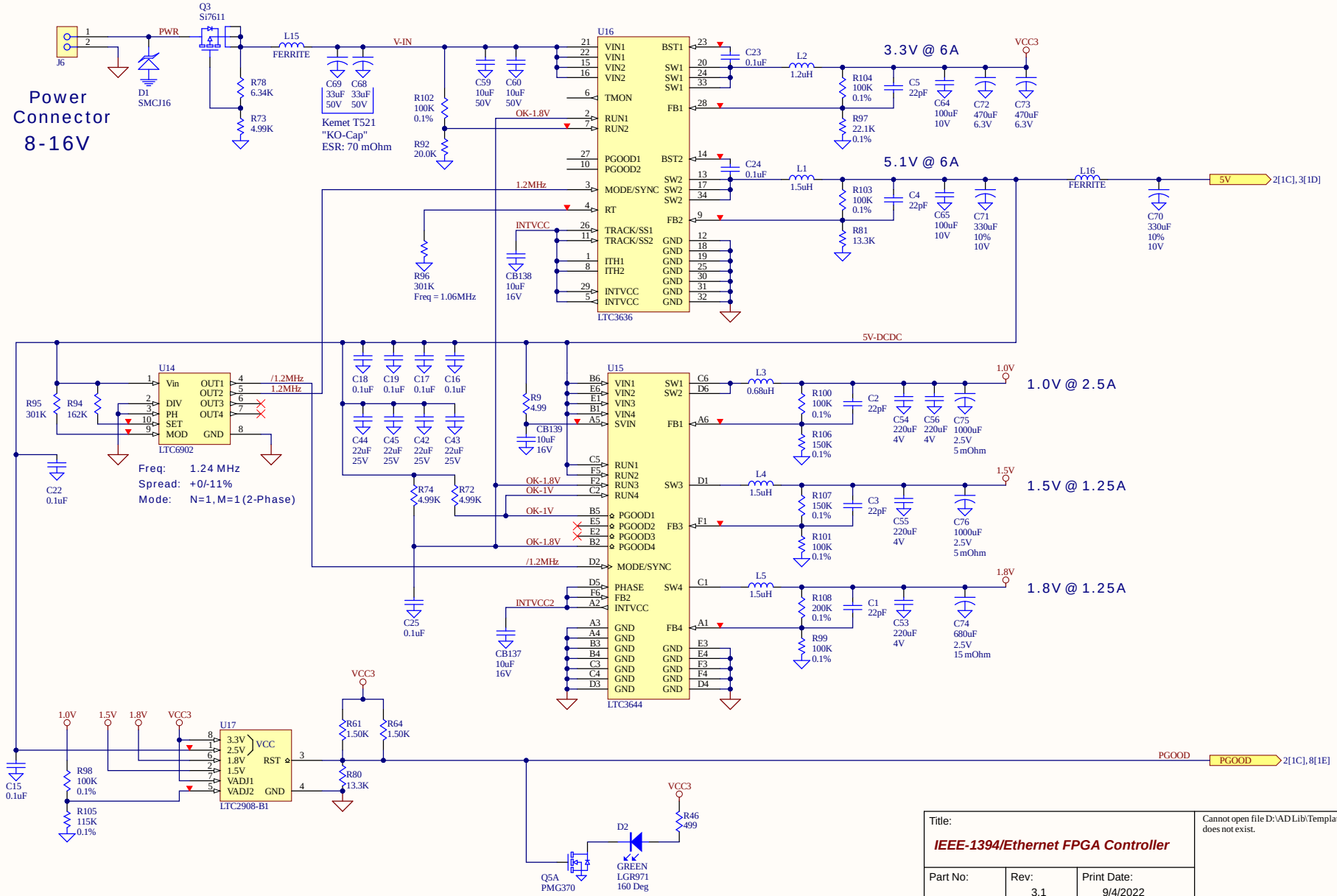
Power Supplies



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