hw4: The Memory Hierarchy Results for VARDAAN KAPOOR (He/him)

Score for this attempt: **7** out of 8
Submitted Apr 3 at 6:37pm
This attempt took 15 minutes.

Question 1

1 / 1 pts

Assume the following sequence of blocks are fetched into the *same set* of a 4-way set associative cache that is initially empty:

```
b7,b5,b1,b5,b4,b5,b7,b4,b8,b8,b7,b8,b9,b1,b1,b7,b1,b8,b1,b2,b9,b9,b5,b2
```

Assume the placement policy is increasing line order (i.e., line 0 to line 3), and the replacement policy is least-frequently used. After the sequence completes, which one below lists the resulting lines ordered from line 0 to line 3?

- `b2, b5, b9, b1`
- `b1, b5, b7, b8`
- `b7, b2, b8, b1`

Correct!

- `b1, b2, b5, b8`
- `--, b7, b2, b8`
- where -- means unused

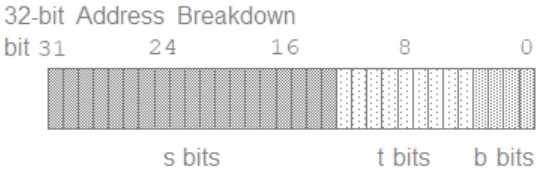
Question 2

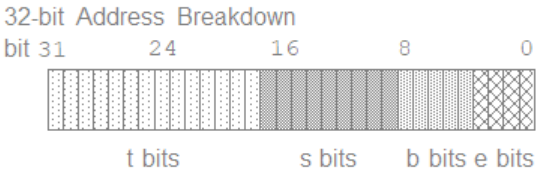
1 / 1 pts

Consider the following characteristics of a cache memory system:

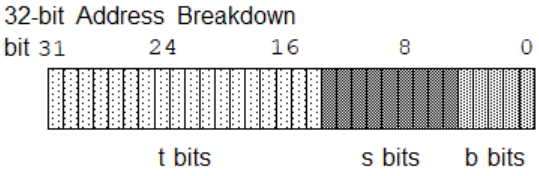
- Addresses are 32 bits.
- The memory is byte addressable.
- The CPU accesses 4-byte words.
- Blocks have 32 bytes.
- The cache is 16-way set associative with 512 sets.

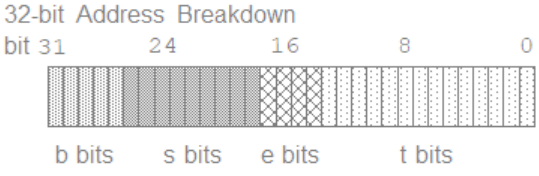
Which one of the following shows the address breakdown for an efficient cache implementation having the characteristics above?

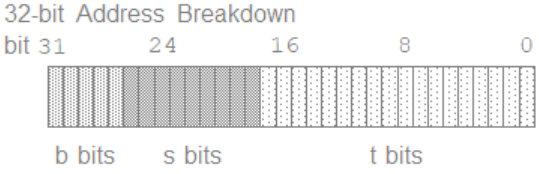




Correct!







Question 3

1 / 1 pts

Which of the following exhibit spatial locality:

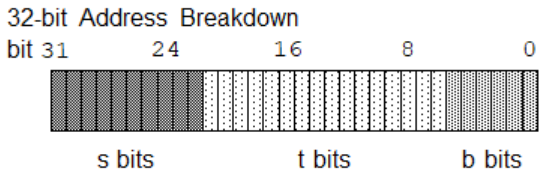
1. Sequencing control flow
2. Linear search on an array of integers
3. Accessing the first element of each row in a 2D array that is heap allocated as an array of arrays

- 1 and 3
- 3 only
- 1 and 2 (Correct!)
- 1 only
- 1, 2 and 3

Question 4

1 / 1 pts

Consider a 64KB cache that uses the following unusual address breakdown:



Assume the following code runs on this caching system:

```
int total = 0;
int *heapArray = malloc(sizeof(int) * 4096); //int is 4 bytes
for (int i = 0; i < 4096; i++)
    total += heapArray[i];
```

What is the maximum number of memory blocks for the array that are stored in the cache at any point in time?

Correct!

- (●) 1
- ( ) 256
- ( ) 2
- ( ) 4
- ( ) 512
- ( ) 1024

Question 5

0 / 1 pts

Consider the following three code fragments; assume that the stack allocated array is initialized so that all indexing is in bounds.

```
//Code Fragment 1:
for (int hour = 0; hour < 24; hour += 2) {
    for (int elev = 0; elev < 16000; elev += 1) {
        for (int count = 0; count < 200; count += 1) {
            total = array[hour][elev][count];
        }
    }
}
```

```
//Code Fragment 2:
for (int hour = 0; hour < 24; hour += 1) {
    for (int elev = 0; elev < 16000; elev += 1) {
        for (int count = 0; count < 200; count += 1) {
            total = array[hour][elev][count];
        }
    }
}
```

```
//Code Fragment 3:
for (int hour = 0; hour < 24; hour += 1) {
    for (int elev = 0; elev < 16000; elev += 1) {
        for (int count = 0; count < 200; count += 50) {
            total = array[hour][elev][count];
        }
```

```
    }
}
```

Which one of the following orders the code fragments above from best to worst use of spatial locality?

orrect Answer

- 2, 1, 3

- 1, 2, 3

- 3, 2, 1

- 3, 1, 2

ou Answered

- 2, 3, 1

- 1, 3, 2

Question 6

1 / 1 pts

Consider a cache characterized as (8, 1, 8, 14). If the contents of the cache are as follows where the Tag and byte values are given in hexadecimal.

Set Index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
0	09	0	A0	30	E0	0B	00	05	F0	DE
1	45	1	9D	43	3F	C3	A6	F5	DD	FF
2	EB	1	43	D4	84	AF	53	48	DE	B7
3	06	0	64	45	99	F1	75	B2	FB	37
4	C7	0	33	23	16	43	FA	B1	45	C2
5	71	1	FF	74	CC	AA	05	83	76	DE
6	91	1	EB	A4	E2	45	F0	72	81	EF
7	46	1	4C	A7	DD	74	23	DA	23	FE

What byte value, if any, is accessed by the address `0x0E36`?

- 81

- CC

EF

Correct! cache miss

23

Question 7

1 / 1 pts

The following table gives the parameters for a cache.

C	S	E	B	m	t	s	b
2048	128	**W**	4	32	**X**	**Y**	**Z**

Answer the following questions

1. The value of **W** is [Select]
2. The value of **X** is [Select]
3. The value of **Y** is [Select]
4. The value of **Z** is 2

Answer 1:

Correct! 4

Answer 2:

Correct! 23

Answer 3:

Correct! 7

Answer 4:

Correct! 2

Question 8

1 / 1 pts

Consider an intentionally small cache characterized by (4, 1, 8, 16) that is initially empty. Given an array of 8 integers that starts at address 0x7090, accessing the array elements in this order:

```
array[0], array[1], array[3], array[2], array[4]
```

would result in which one of the following?

- miss, hit, hit, hit, miss
- miss, miss, miss, miss
- miss, hit, miss, hit, miss

Correct!

- miss, hit, hit, miss, miss
- miss, hit, miss, miss, miss

Quiz Score: **7** out of 8