M3733

High Definition Smart Hybrid OTT Processor
High Definition Smart Hybrid DVB-C SOC Processor

Preliminary Datasheet

Version 1.3
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ALi Corporation

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Revision History

Version	Date	Revision
1.0	2014/01/21	First Release
1.1	2014/06/25	Update features (Ch. 1) and DC characteristics (Ch. 5)
1.2	2015/07/13	Add TS output & MVC (Ch.1 & Ch. 2)
1.3	2015/09/02	Update Video DAC dual inputs feature (section 1.1, page 4)

CONTENT

FIGURES

TABLES

1. Introduction

M3733 is a high performance, low power SOC for high definition hybrid OTT box, IPTV or dongle solutions. It has a dual core Cortex A9 processor, dedicated audio processor, advanced OpenGL ES 3D graphic engine, 32bit DDR3 controller, UHD 4K display engine, ALi ASE 3.0 encryption engine, DVB-C QAM annex a/b/c demodulator, four USB 2.0 host/device ports, multi-format high definition video decoder including MPEG1/2/4/H.264/VC-1/AVS+/VP8 decoding, 3D video with H.264 MVC, H.264 encoder, TV encoder and HDMI transmitter with 3D over HDMI, 48bit deep color and 4Kx2K resolution and provides one 10/100M Ethernet port with MAC and PHY or one Gbit MAC Ethernet solution.

1.1 Features

General Features

- Targeted for High Definition Smart Cable+IP hybrid OTT/STB and IPTV solutions
- 3.3V, 1.8V, 1.5V and two core power supplies

Application Processor Features

- ARM Cortex A9 Dual core
- L1 Cache with I32KB/D32KB
- L2 Cache 512KB
- NEON/vFPU supported
- Jazelle acceleration
- Built-in Interrupt Controller and timer
- Supports DVFS for power saving
- Supports ARM JTAG debugging

Security Processor Features

- RISC CPU with 32-bit bus architecture for security processing
- Internal operating frequency up to 594MHz
- Performance up to 712 DMIPS
- Built-in L1 I-cache 8K bytes, D-cache 16K bytes
- Supports JTAG for debugging

Audio Processor Features

- RISC CPU with 32-bit bus architecture
- Internal operating frequency up to 594MHz
- Performance up to 712 DMIPS
- I-cache 8K bytes, D-cache 16K bytes, two-way set-associate
- Supports JTAG for debugging

Advanced HW Security Features

- Embeds Boot ROM for Secure Boot
- Embeds OTP memory for Secret Key & ID
- Supports OTP Obfuscation for Secret Keys inside OTP
- Embeds TRNG
- Embeds SHA-1/SHA-224/SHA-256/SHA-384/SHA-512 hash engine
- Embeds Crystal Clock Speed Detector
- Embeds Voltage Level Detector
- Supports EJTAG debug interface password protection or permanently disabled
- Supports DRAM scramble
- Supports FLASH content encryption including Boot Loader code
- Supports Key Ladders
- Supports DES/3DES/AES/CSA1.1/CSA2.0/CSA3.0/Multi2/GOST/M6 Descrambler

Memory and Bus Interfaces

- 16/32-bit DDR3/DDR2 DRAM interfaces
- Dram frequency up to 1600Mhz
- Supports DRAM Size: 64MB to 2GB
- Supports Dual Channel DRAM Controller in 32-bit mode
- Supports S-FLASH size : 512KB to 32MB
- Supports S-FLASH speed up to 50M @ 1/2/4 bit

Peripherals

- 2 RS-232 serial interfaces
- 4 I2C interfaces, all supporting master, slave mode and EDDC function
- 1 IR receiver interface, 1 IR transmitter (shared with GPIO)

- Multi-bit GPIO without de-bounce
- 2 watch dog timers to prevent system lock

Transport Stream Interface

- Transport stream input @135Mbps in serial mode
- Transport stream input @400Mbps in parallel mode
- Transport stream input @270Mbps in ALi SSI mode
- 1 parallel TS input port
- 4 SSI or ALI SSI ports, shared with parallel TS port
- SSI/SPI output shared with SSI/SPI input

DEMUX

- Supports 4 sets of DEMUX
- Supports max 50 MB/s TS input
- HW auto-detect PCR packet
- 16 bit x 96 channels per filter
- Unite DMA buffer mode

CI

- Supports DVB CI/CI+ Common Interface

QAM

- Supports ETSI 300-429 Specification and ITU-T J83 Annex A, Annex B, Annex C
- Supports 16-QAM, 32-QAM, 64-QAM, 128-QAM and 256-QAM Constellations
- High Performance integrated 10-bit ADC suitable for High IF or Low IF architecture
- Supports variable symbol rate, for QAM from 1.5M to 7.0M baud-rate
- Embeds PDM AGC control loop
- Full Digital Timing recovery and carrier recovery
- Enhanced Blind Equalizer against long and strong echoes
- Robust FSM supporting timing offset and carrier offset auto-sweep function
- Fast and blind acquisition of all symbol rates and QAM Modulation Modes
- Signal quality indicator and signal strength(RF Level), SNR/BER/constellation/lock status indication
- MPEG2 transport stream output (parallel/serial interface supported)

PMU

- Supports Real Time Clock
- Supports IR/KEY/CEC standby/resume
- Supports on schedule resume
- Supports DRAM retention standby mode
- Supports System Deep Standby mode compliant with Euro Green Power Standard
- Supports embedded MCU for flexible standby mode functions

Conditional Access Interface

- 2 sets of dedicated ISO7816 smart-card reader interfaces
- ISO7816-1/2/3(Transport Protocol) compatible smart card interface
- Supports T=0, T=1 and T=14 transmission protocols
- Supports PTS (protocol type selection) procedure
- Power on sequence generation
- Programmable baud rate generating different frequencies
- Auto error signal generation on parity error detection in receive mode
- Card detection and power enable polarity selectable

Scatter/Gather DMA

- 2 sets of Scatter/Gather DMA Interfaces
- Start Code search function

Video Decoder

- ISO/IEC 11172-2 MPEG1
- ISO/IEC 13818-2 MPEG2 MP@HL
- ISO/IEC 14496 MPEG4 compliant supporting SP@L3 to ASP@L5
- H.263 (short Header)
- Xvid
- ISO/IEC 14496-10 AVC high profile@level 4.1 main profile@level 4.1
- ISO/IEC 14496-10 AVC Baseline profile@level 4.1
- MVC stereo high profile @ level 4.1
- VC-1 (Simple/Main/Advance profile, level 0~3) video decoder
- VP8 Simple/Enhance profile video decoder
- AVS Jizhun profile up to level 6.0

- AVS+
- All decoders support 2x speed
- Supports fundamental Dview function 1, 1/2, 1/4, 1/8
- Out-loop de-blocking

Display Engine
- Up to 2 video planes and 2 graphic planes (BG + Main video + Auxiliary video + Graphic 1 + Graphic 2)
- High quality scaling for UHD 4K, HD and SD outputs
- Built-in video enhancements
- High quality motion adaptive and EPEC (edge preserve and edge compensation) de-interlace
- Highly efficient solution for dual outputs applications
- Up to 32bit aRGB true color and CLUT graphic planes input
- High quality scaling with EP(edge preserve) for both graphic planes
- Advanced algorithms of anti-flicker for both graphic planes

Video Encoder
- ISO/IEC 14496-10 AVC high profile@level 4.1 main profile@level 4.1

3D GPU
- Mali-400 dual PP and up to 600 Mpixels/s
- Fully supports OpenGL ES 1.1/2.0 and OpenVG 1.1 API
- Integrates MMU based on standard ARM MMU
- Independent GPU power management and power on/off function
- Fully optimized production quality software drivers for Linux and Android

Audio Decoder
- MPEG-1/2 Layer I/II
- AAC/HEAAC v1/v2
- OGG
- ALAC
- FLAC
- APE

Programmable HW Audio Codec Engine
- Supports IMDCT and SBR module in MS11 spec or other complex audio applications
- Supports DMA mode to access DRAM

HW Audio Engine
- One I2S output supporting internal/external DAC for playing audio
- One I2S input supporting external CODEC for recording audio or microphone in
- Supports S/PDIF output
- Supports DDPLUS S/PDIF output (out to HDMI directly in chip core)
- Supports one PCM(also can be programmed to I2S) input and output for VOIP
- One embedded Audio DAC for stereo outputs supporting 8-192kHz sample rate
- EQ, 4 bands EQ for all channels except center and subwoofer channel
- Volume control, supporting 1/256 step from mute to max volume control
- Fade In/Out for preventing pop noise
- H/W AV sync supported by PTS (Presentation Time Stamp) and SCR(System Clock Reference) check

Network
- Gb Ethernet MAC supports Reduced GMII interface
- Full Duplex/Half Duplex capability for 10M/100M MAC
- Full Duplex capability for Gb MAC
- Supports IEEE 802.3x full Duplex Flow Control
- Supports IEEE 802.1Q VLAN tagging(Tagged MAC frame)
- Supports wake-on-LAN remote wake-up
- Integrates two large independent transmit (2KB) and receive (16KB) FIFO devices
- Supports a 28-bit general-purpose timer with the MAC clock as the clock source to generate timer-interrupt
- Supports TCP/UDP Checksum for Transmitter and Receiver
- Supports Individual IPv4/IPv6 Check Sum Format
- Separated RX COE & TX COE Function
- Supports Back pressure Flow Control in half-duplex Mode
- Supports 9Kbyte Jumbo Frame Receiver
- Supports Interrupt Coalescence for Receiver
- Supports Scatter/Gather I/O Function for Linux OS
- Supports TSO Function for Linux OS

- Supports UFO Function for Linux OS
- Supports 65536 TX Descriptors and 65536 Rx Descriptors maximum
- RX Supports Remove VLAN TAG Function
- TX Supports Insert VLAN TAG Function

10/100M Ethernet PHY

- Fully compliant with the IEEE 802.3 / 802.3u 10BASE-T, 100BASE-TX
- Interface available to 100Base-FX Fiber-PMD (transceiver), compliant with TP-PMD standard: ANSI X3.263-1995, compliant with FDDI-PMD standard: ISO/IEC 9314-3: 1990 and ANSI X3.166-1990
- Supports RMII / MII interface to the MAC controller
- Serial management interface compliant with IEEE 802.3u
- Supports Full-Duplex or Half-Duplex Operation
- Supports Auto-Negotiation/Parallel Detection function compliant with IEEE 802.3u, and manual configuration is also supported
- Automatic Polarity Correction
- Supports auto MDI/MDIX crossover function for 10BASE-T / 100BASE-TX
- Supports Power Down / Power reduced work Mode
- High performance baseline wander correction (BLW) Circuit
- High Performance Digital Clock recovery algorithm
- High performance Digital Blind Equalizer for ISI mitigation
- LED Driver for Link, Activity, Duplex, Collision, and Speed Status
- Supports 803.2az standard-2010 (EEE)

NAND Flash

- Supports ECC Types: no ECC, CRC16/512B, 1bit/512B ECC, 16bit/1024B ECC, 24bit/1024B ECC, 40bit/1024B ECC, 48bit/1024B ECC, 60bit/1024B ECC
- Supports NF Interface Types: Legacy(Asynchronous) , Toggle and Synchronous, 8bit data bus access

HDMI

- Fully compliant with HDMI specification
- Supports 3D display over HDMI
- Supports Deep Color up to 16bits
- Supports xvYCC
- Supports resolutions SDTV, HDTV, and VGA
- Scalable bandwidth: 25–297 Mega pixels per second (Mpps)
- Programmable clock, data timing (deskew)
- Supports hot plug detection
- Power down mode
- High bandwidth supporting HDTV formats including 4K, 1080p, 1080i and 720p

Video DAC

- 4 x 10bit DAC for SD/HD dual outputs, not including OSD separate display function
- Analog HD output YPbPr or RGB, RGsB, RGBHV
- Analog SD output YCbCr, YC or CVBS

USB

- Two sets of USB 2.0 host controllers compatible with EHCI/OHCI
- Supports USB specification revision 2.0 High-Speed (HS)/ Full-Speed (FS)/ Low-Speed (LS) compliant with on-chip USB transceiver
- Supports up to 4 host ports or 2 host ports + 1 device port
- Supports configurable HS/FS mode on device port
- Supports 5-layer hub device extension
- Supports USB suspend/resume/remote wakeup protocol
- Supports power-down/power-up control to reduce power consumption

SDIO

- Supports SD/SDIO cards
- Supports eMMC and MMC cards
- Supports PIO interface for DATA read/write
- Supports DMA interface for DATA read/write
- Supports half-duplex serial and parallel data transfer for SD/SDIO cards, i.e. 1 bit, 4 bits
- Supports half-duplex serial and parallel data transfer for eMMC/MMC cards, i.e. 1 bit, 4 bits, 8 bits

Package

- FBGA 462 balls

2. System Block Diagrams

2.1 Architecture Block Diagram

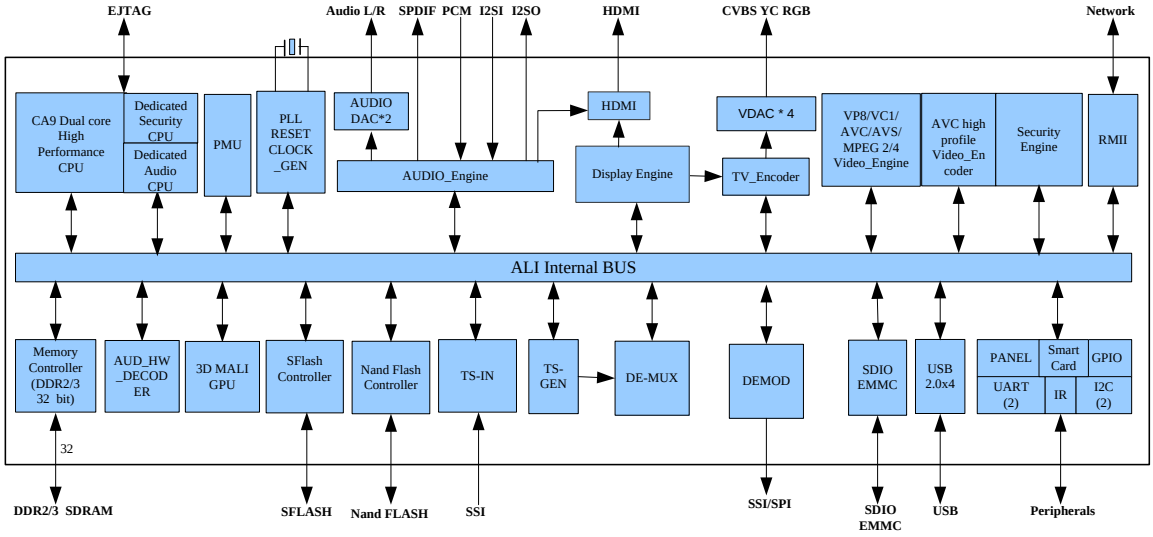


Figure 2-1. M3733 Block Diagram

2.2 Application Diagram

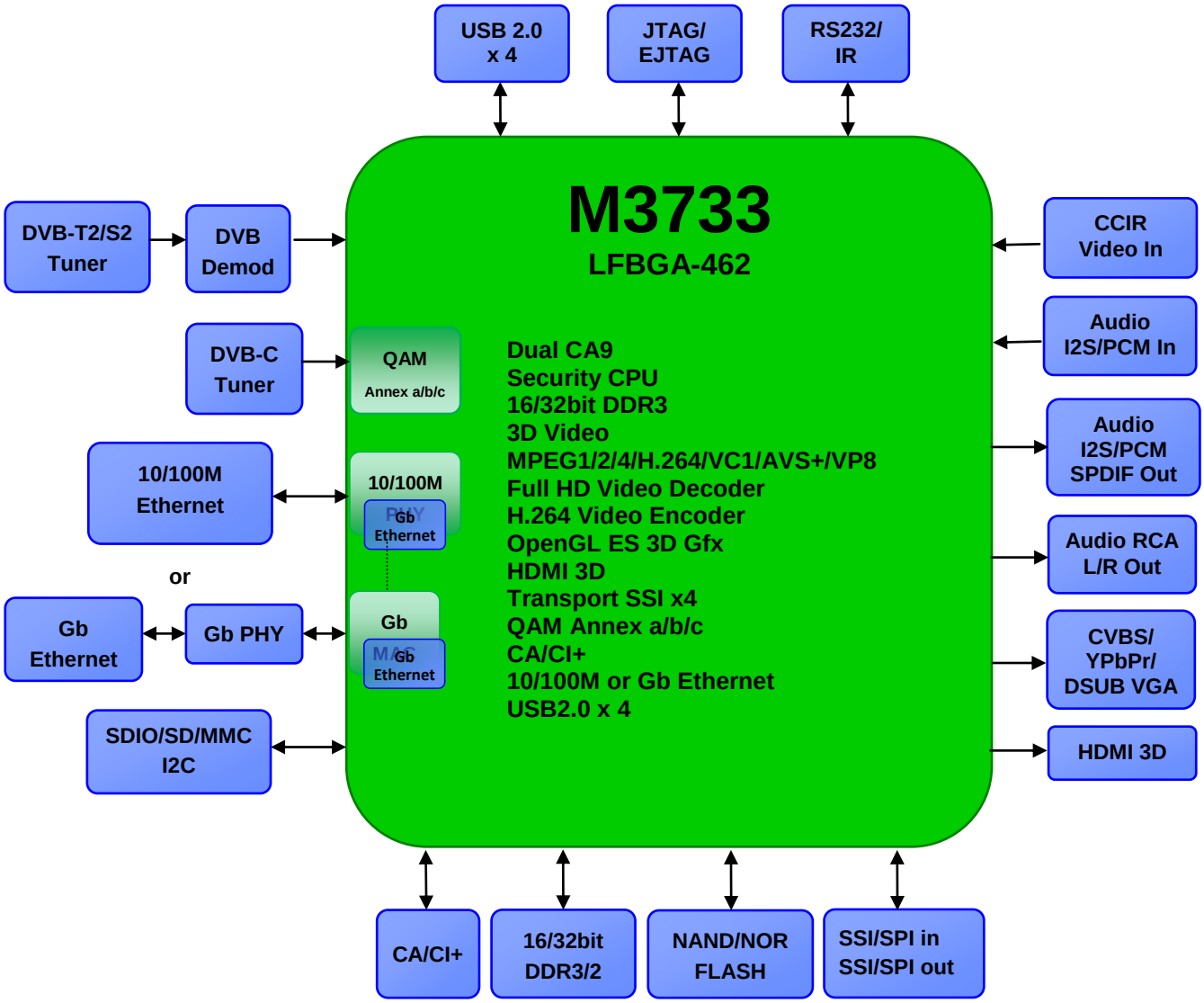
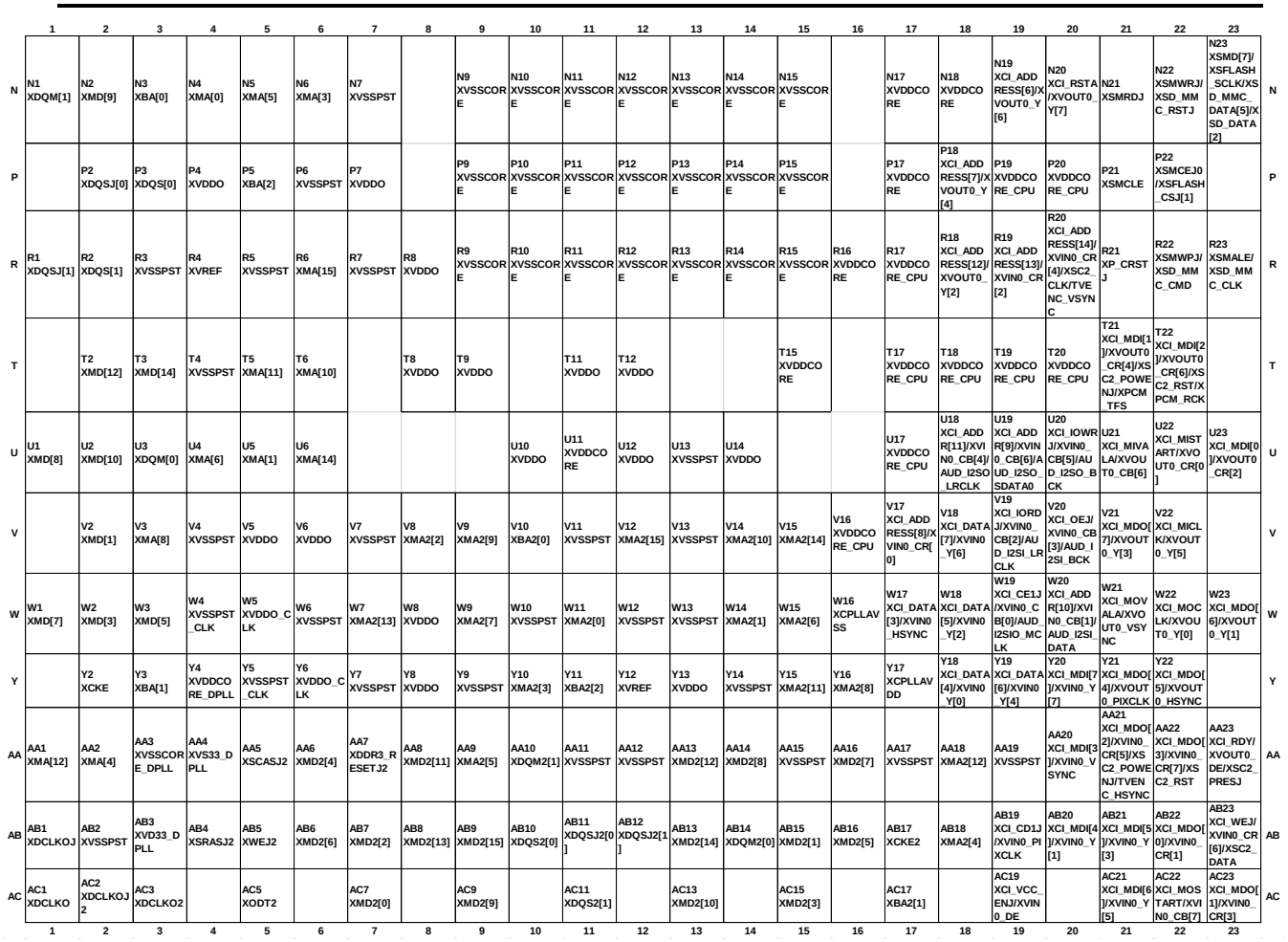


Figure 2-2. M3733 Application Diagram

3. Pin Configuration

Table 3-1. Pin Arrangement

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	A1 XDP[1]	A2 XDM[1]	A3 XDM[0]	A4 XENET_TXN	A5 XENET_RXN	A6 TMDSDATAN[2]	A7 TMDSDATAN[1]	A8 TMDSDATAN[0]	A9 TMDSCLKN	A10 XGPIO[4]	A11 XSCL_3/MCU_DOCD_DATAO		A13 XVDAC_OUT3		A15 XSDA_1/XPCM_PCM_DO/AUD_XEJ_TDI		A17 XSCL_2/XUART2_RX		A19 XRXADC_IP		A21 XPMU_VSSIO	A22 XP_X27IN	A23 XPMU_VDDIO	A
B	B1 XDP[2]	B2 XDM[2]	B3 XDP[0]	B4 XENET_TXP	B5 XENET_RXP	B6 TMDSDATAP[2]	B7 TMDSDATAP[1]	B8 TMDSDATAP[0]	B9 TMDSCLKP	B10 XGPIO[5]	B11 XSDA_3/MCU_DOCD_DATAI	B12 XVDAC_OUT1	B13 XVDAC_OUT4	B14 XADAC_OL_P	B15 XGPIO_PCM1/XPCM_RFS/AUD_XEJ_TDO	B16 XGPIO_PCM2/XPCM_PCM_DI/AUD_XEJ_TCLK	B17 XSDA_2/XUART2_TX	B18 XIF_AGC_PDM/XSC1_DATA/ALISSI4_DATA1	B19 XRXADC_IN	B20 XPMU_GPIO[7]/AUD_I2SO_BCK/ALISSI4_CLK	B21 XP_X27OUT	B22 XIR_RX	B23 XTSPI_DATA[0]/ALISSI2_DATA1/QAM_SPI_DATA[0]	B
C	C1 XDP[3]	C2 XDM[3]	C3 XRGMII_MDIO	C4 XENET_VSSA1	C5 XENET_PLL_VSSA	C6 XHDMI_GD	C7 XHDMI_GD	C8 XHDMI_GD	C9 XHDMI_GD	C10 XHDMI_DDCCEC	C11 XCEC	C12 XVDAC_OUT2	C13 XGPIO_127/XTUN_AGC_PDM/XIR_TX/AUD_XEJ_TRST/TVENC_VSYNC	C14 XADAC_OR_P	C15 XSCL_1/XPCM_RCK/AUD_XEJ_TMS	C16 XSPDIF/MCU_DOCD_CLK	C17 XUART_RX	C18 XRXADC_AVS	C19 XPMU_GPIO[8]/ALISSI4_DATA0	C20 XPMU_GPIO[6]/XSC1_PRESJ/AUD_I2SO_LRCLK/ALISSI4_VALID	C21 XTSPI_DATA[1]/ALISSI2_DATA0/QAM_SPI_DATA[1]	C22 XTSPI_DATA[3]/ALISSI2_VALID/QAM_SPI_DATA[3]	C23 XTSPI_DATA[2]/ALISSI2_CLK/QAM_SPI_DATA[2]	C
D		D2 XRGMII_TXD[3]	D3 XRGMII_MDC	D4 XRGMII_TXD[2]	D5 XAVDDUSBTX	D6 XENET_VDDA1	D7 XENET_PLL_VDCORE	D8 XVDDIO	D9 XHDMI_GD	D10 XGPIO[6]	D11 XHDMI_VP	D12 XVDDIO	D13 XVSSCORE	D14 XVDAC_VDDA	D15 XADAC_VREF	D16 XVDD_ADAC_3	D17 XRXADC_DVS	D18 XRXADC_AVD	D19 XMPLLAVDD	D20 XRXPLLAVDD	D21 XTSPI_DATA[4]/ALISSI2_SYNC/QAM_SPI_DATA[4]	D22 XTSPI_DATA[5]/ALISSI2_ERROR/QAM_SPI_DATA[5]		D
E	E1 XRGMII_TX_CTL	E2 XRGMII_RXC	E3 XRGMII_TXC	E4 XRGMII_TXD[0]	E5 XAVDDUSBTX	E6 XRREF	E7 XENET_REXTA	E8 XVDDIO		E10 XHDMI_AVDD33	E11 XHDMI_VP	E12 XVDDIO	E13 XVDDCORE	E14 XVDAC_VSSA	E15 XVSS_ADAC_3	E16 XEJ_TMS/TVENC_VSYNC/ALISSI_SYNC/QAM_SSI_SYNC	E17 XVSSCORE	E18 XRXADC_DVD	E19 XPMU_GPIO[5]/XSC1_RST/AUD_I2SI_BCK/ALISSI_DATA1	E20 XRXPLLAVSS	E21 XTSPI_DATA[6]/ALISSI3_DATA1/QAM_SPI_DATA[6]	E22 XTSPI_CLK/ALISSI3_CLK/QAM_SPI_CLK/QAM_SSI_CLK	E23 XTSPI_DATA[7]/ALISSI3_DATA0/QAM_SPI_DATA[7]/QAM_SSI_DATA[0]	E
F		F2 XPHY_INT	F3 XRGMII_REF_CLK	F4 XRGMII_RXD[0]	F5 XRGMII_TXD[1]	F6 XAVSSUSBTX	F7 XAVSSUSBTX	F8 XVDDIO	F9 XGPIO[1]/XSPDIF/MCU_UART_TXD	F10 XHDMI_REXT	F11 XVSSIO	F12 XEJ_SELECT/TVENC_HSYNC/ALISSI_DATA1	F13 XHDMI_HPD	F14 XEJ_TDI/AUD_I2SO_SDATA2/ALISSI_CLK/QAM_SSI_CLK	F15 XEJ_TDO/AUD_I2SO_SDATA1/ALISSI_VALID/QAM_SSI_VALID	F16 XEJ_TCLK/ALISSI_ERROR/QAM_SSI_ERROR	F17 XUART_TX	F18 XPMU_GPIO[4]/AUD_I2SI_LRCLK/ALISSI_DATA0/QAM_SSI_DATA[0]	F19 XPMU_GPIO[3]/AUD_I2SI_DATA/ALISSI_CLK/QAM_SSI_CLK	F20 XTSPI_VALID/ALISSI3_VALID/QAM_SPI_VALID/QAM_SSI_VALID	F21 XTSPI_ERROR/ALISSI3_ERROR/QAM_SPI_ERROR/QAM_SSI_ERROR	F22 XTSPI_SYNC/ALISSI3_SYNC/QAM_SPI_SYNC/QAM_SSI_SYNC		F
G	G1 XSRASJ	G2 XSCASJ	G3 XVSSPST	G4 XRGMII_RXD[2]	G5 XRGMII_RX_CTL	G6 XGPIO[2]/DIGITAL_PLL_FOUT2/MCU_UART_RXDI				G10 XVDDIO	G11 XVDDIO	G12 XVSSIO	G13 XVSSIO	G14 XEJ_TRST/AUD_I2SO_SDATA3/ALISSI_DATA0/QAM_SSI_DATA[0]				G18 XPMU_GPIO[2]/AUD_I2SIO_MCLK/ALISSI_VALID/QAM_SSI_VALID	G19 XPMU_GPIO[1]/XUART2_RX/TVENC_HSYNC/ALISSI_SYNC/QAM_SSI_SYNC	G20 XPMU_GPIO[0]/XUART2_TX/ALISSI_ERROR/QAM_SSI_ERROR	G21 XPCM_RFS/AUD_I2SO_SDATA2/AUD_I2SO_LRCLK_2/ALISSI3_DATA0	G22 XPCM_DI/AUD_I2SO_SDATA3/AUD_I2SO_BCK_2/ALISSI3_DATA1	G23 XGPIO[0]/XSC1_POWENJ/AUD_I2SO_SDATA0/ALISSI4_SYNC/AUD_I2SO_SDATA_2/XSMDQS	G
H		H2 XWEJ	H3 XSC1_CLK	H4 XRGMII_RXD[3]	H5 XRGMII_RXD[1]	H6 XSC1_POWENJ		H8 XVDDIO	H9 XVDDCORE						H15 XVDDCORE	H16 XVDDCORE		H18 XPMU_DOWN	H19 XVDDCORE	H20 XVDDCORE	H21 XPCM_TFS/AUD_I2SI_DATA_2/ALISSI3_SYNC	H22 XPCM_TCK/AUD_I2SIO_MCLK_2/ALISSI3_ERROR		H
J	J1 XMD[4]	J2 XODT	J3 XVSSPST	J4 XSC1_DATA	J5 XSC1_RST	J6 XSC1_PRESJ		J8 XVDDIO	J9 XVDDCORE	J10 XVDDCORE	J11 XVSSIO	J12 XVSSIO	J13 XVSSIO	J14 XVSSIO	J15 XVSSIO	J16 XVDDCORE		J18 XDFTTM	J19 XGPIO[3]/XSC1_CLK/ALISSI4_ERROR	J20 XCI_CD2J/XPCM_PCM_DI	J21 XSMCEJ1/XSFLASH_CSJ[0]	J22 XPCM_DO/AUD_I2SI_LRCLK_2/ALISSI3_VALID	J23 XPCM_RCK/AUD_I2SO_SDATA1/AUD_I2SI_BCK_2/ALISSI3_CLK	J
K		K2 XMD[2]	K3 XMD[6]	K4 XDDR3_RESETJ	K5 XVSSPST	K6 XMA[9]	K7 XVSSCORE		K9 XVSSCORE	K10 XVSSCORE	K11 XVSSCORE	K12 XVSSCORE	K13 XVSSCORE	K14 XVSSCORE	K15 XVSSIO		K17 XCI_ADDRESS[0]/XVOUT0_CR[1]	K18 XCI_DATA[0]/XVOUT0_CR[3]/XSC2_CLK/XPCM_TCK	K19 XCI_DATA[2]/XVOUT0_CR[7]/XSC2_PRESJ/XPCM_RFS	K20 XCI_DATA[1]/XVOUT0_CR[5]/XSC2_DATA/XPCM_PCM_DO	K21 XSMD[1]/XSD_MMC_DATA[6]	K22 XSMD[0]/XSD_MMC_DATA[7]		K
L	L1 XMD[11]	L2 XMD[0]	L3 XVSSPST	L4 XMA[2]	L5 XVSSPST	L6 XMA[13]	L7 XVDDO		L9 XVSSCORE	L10 XVSSCORE	L11 XVSSCORE	L12 XVSSCORE	L13 XVSSCORE	L14 XVSSCORE	L15 XVSSIO		L17 XVDDCORE	L18 XCI_REGJ/XVOUT0_CB[4]	L19 XCI_ADDRESS[3]/XVOUT0_CB[3]	L20 XCI_ADDRESS[2]/XVOUT0_CB[5]	L21 XSMD[4]/XSFLASH_WJ/XSD_MMC_DATA[0]/XSD_CLK	L22 XSMD[3]/XSFLASH_HOLDJ/XSD_MMC_DATA[1]/XSD_DATA[0]	L23 XSMD[2]/XSD_MMC_DATA[2]/XSD_DATA[1]	L
M		M2 XMD[15]	M3 XMD[13]	M4 XVSSPST	M5 XMA[7]	M6 XVSSPST	M7 XVDDO		M9 XVSSCORE	M10 XVSSCORE	M11 XVSSCORE	M12 XVSSCORE	M13 XVSSCORE	M14 XVSSCORE	M15 XVSSIO	M16 XVDDCORE	M17 XCI_WAITJ/XVOUT0_CB[2]	M18 XCI_ADDRESS[1]/XVOUT0_CB[7]	M19 XCI_ADDRESS[5]/XVOUT0_CB[0]	M20 XCI_ADDRESS[4]/XVOUT0_CB[1]	M21 XSMD[6]/XSFLASH_MOSI/XSD_MMC_DATA[3]/XSD_DATA[3]	M22 XSMD[5]/XSFLASH_MISO/XSD_MMC_DATA[4]/XSD_CMD		M
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
N	N1 XDQM[1]	N2 XMD[9]	N3 XBA[0]	N4 XMA[0]	N5 XMA[5]	N6 XMA[3]	N7 XVSSPST		N9 XVSSCORE	N10 XVSSCORE	N11 XVSSCORE	N12 XVSSCORE	N13 XVSSCORE	N14 XVSSCORE	N15 XVSSCORE		N17 XVDDCORE	N18 XVDDCORE	N19 XCI_ADDRESS[6]/XVOUT0_Y[6]	N20 XCI_RSTA/XVOUT0_Y[7]	N21 XSMRDJ	N22 XSMWRJ/XSD_MMC_RSTJ	N23 XSMD[7]/XSFLASH_SCLK/XSD_MMC_DATA[5]/XSD_DATA[2]	N
P		P2 XDQSJ[0]	P3 XDQS[0]	P4 XVDDO	P5 XBA[2]	P6 XVSSPST	P7 XVDDO		P9 XVSSCORE	P10 XVSSCORE	P11 XVSSCORE	P12 XVSSCORE	P13 XVSSCORE	P14 XVSSCORE	P15 XVSSCORE		P17 XVDDCORE	P18 XCI_ADDRESS[7]/XVOUT0_Y[4]	P19 XVDDCORE_CPU	P20 XVDDCORE_CPU	P21 XSMCLE	P22 XSMCEJ0/XSFLASH_CSJ[1]		P
R	R1 XDQSJ[1]	R2 XDQS[1]	R3 XVSSPST	R4 XVREF	R5 XVSSPST	R6 XMA[15]	R7 XVSSPST	R8 XVDDO	R9 XVSSCORE	R10 XVSSCORE	R11 XVSSCORE	R12 XVSSCORE	R13 XVSSCORE	R14 XVSSCORE	R15 XVSSCORE	R16 XVDDCORE	R17 XVDDCORE_CPU	R18 XCI_ADDRESS[12]/XVOUT0_Y[2]	R19 XCI_ADDRESS[13]/XVIN0_CR[2]	R20 XCI_ADDRESS[14]/XVIN0_CR[4]/XSC2_CLK/TVENC_VSYNC	R21 XP_CRSTJ	R22 XSMWPJ/XSD_MMC_CMD	R23 XSMALE/XSD_MMC_CLK	R
T		T2 XMD[12]	T3 XMD[14]	T4 XVSSPST	T5 XMA[11]	T6 XMA[10]		T8 XVDDO	T9 XVDDO		T11 XVDDO	T12 XVDDO			T15 XVDDCORE		T17 XVDDCORE_CPU	T18 XVDDCORE_CPU	T19 XVDDCORE_CPU	T20 XVDDCORE_CPU	T21 XCI_MDI[1]/XVOUT0_CR[4]/XSC2_POWENJ/XPCM_TFS	T22 XCI_MDI[2]/XVOUT0_CR[6]/XSC2_RST/XPCM_RCK		T
U	U1 XMD[8]	U2 XMD[10]	U3 XDQM[0]	U4 XMA[6]	U5 XMA[1]	U6 XMA[14]				U10 XVDDO	U11 XVDDCORE	U12 XVDDO	U13 XVSSPST	U14 XVDDO			U17 XVDDCORE_CPU	U18 XCI_ADDR[11]/XVIN0_CB[4]/AUD_I2SO_LRCLK	U19 XCI_ADDR[9]/XVIN0_CB[6]/AUD_I2SO_SDATA0	U20 XCI_IOWRJ/XVIN0_CB[5]/AUD_I2SO_BCK	U21 XCI_MIVAL/XVOUT0_CB[6]	U22 XCI_MISTART/XVOUT0_CR[0]	U23 XCI_MDI[0]/XVOUT0_CR[2]	U
V		V2 XMD[1]	V3 XMA[8]	V4 XVSSPST	V5 XVDDO	V6 XVDDO	V7 XVSSPST	V8 XMA2[2]	V9 XMA2[9]	V10 XBA2[0]	V11 XVSSPST	V12 XMA2[15]	V13 XVSSPST	V14 XMA2[10]	V15 XMA2[14]	V16 XVDDCORE_CPU	V17 XCI_ADDRESS[8]/XVIN0_CR[0]	V18 XCI_DATA[7]/XVIN0_Y[6]	V19 XCI_IORDJ/XVIN0_CB[2]/AUD_I2SI_LRCLK	V20 XCI_OEJ/XVIN0_CB[3]/AUD_I2SI_BCK	V21 XCI_MDO[7]/XVOUT0_Y[3]	V22 XCI_MICLK/XVOUT0_Y[5]		V
W	W1 XMD[7]	W2 XMD[3]	W3 XMD[5]	W4 XVSSPST_CLK	W5 XVDDO_CLK	W6 XVSSPST	W7 XMA2[13]	W8 XVDDO	W9 XMA2[7]	W10 XVSSPST	W11 XMA2[0]	W12 XVSSPST	W13 XVSSPST	W14 XMA2[1]	W15 XMA2[6]	W16 XCPLLAVSS	W17 XCI_DATA[3]/XVIN0_HSYNC	W18 XCI_DATA[5]/XVIN0_Y[2]	W19 XCI_CE1J/XVIN0_CB[0]/AUD_I2SIO_MCLK	W20 XCI_ADDR[10]/XVIN0_CB[1]/AUD_I2SI_DATA	W21 XCI_MOVALA/XVOUT0_VSYNC	W22 XCI_MOCLK/XVOUT0_Y[0]	W23 XCI_MDO[6]/XVOUT0_Y[1]	W
Y		Y2 XCKE	Y3 XBA[1]	Y4 XVDDCORE_DPLL	Y5 XVSSPST_CLK	Y6 XVDDO_CLK	Y7 XVSSPST	Y8 XVDDO	Y9 XVSSPST	Y10 XMA2[3]	Y11 XBA2[2]	Y12 XVREF	Y13 XVDDO	Y14 XVSSPST	Y15 XMA2[11]	Y16 XMA2[8]	Y17 XCPLLAVDD	Y18 XCI_DATA[4]/XVIN0_Y[0]	Y19 XCI_DATA[6]/XVIN0_Y[4]	Y20 XCI_MDI[7]/XVIN0_Y[7]	Y21 XCI_MDO[4]/XVOUT0_PIXCLK	Y22 XCI_MDO[5]/XVOUT0_HSYNC		Y
AA	AA1 XMA[12]	AA2 XMA[4]	AA3 XVSSCORE_DPLL	AA4 XVS33_DPLL	AA5 XSCASJ2	AA6 XMD2[4]	AA7 XDDR3_RESETJ2	AA8 XMD2[11]	AA9 XMA2[5]	AA10 XDQM2[1]	AA11 XVSSPST	AA12 XVSSPST	AA13 XMD2[12]	AA14 XMD2[8]	AA15 XVSSPST	AA16 XMD2[7]	AA17 XVSSPST	AA18 XMA2[12]	AA19 XVSSPST	AA20 XCI_MDI[3]/XVIN0_VSYNC	AA21 XCI_MDO[2]/XVIN0_CR[5]/XSC2_POWENJ/TVENC_HSYNC	AA22 XCI_MDO[3]/XVIN0_CR[7]/XSC2_RST	AA23 XCI_RDY/XVOUT0_DE/XSC2_PRESJ	AA
AB	AB1 XDCLKOJ	AB2 XVSSPST	AB3 XVD33_DPLL	AB4 XSRASJ2	AB5 XWEJ2	AB6 XMD2[6]	AB7 XMD2[2]	AB8 XMD2[13]	AB9 XMD2[15]	AB10 XDQS2[0]	AB11 XDQSJ2[0]	AB12 XDQSJ2[1]	AB13 XMD2[14]	AB14 XDQM2[0]	AB15 XMD2[1]	AB16 XMD2[5]	AB17 XCKE2	AB18 XMA2[4]	AB19 XCI_CD1J/XVIN0_PIXCLK	AB20 XCI_MDI[4]/XVIN0_Y[1]	AB21 XCI_MDI[5]/XVIN0_Y[3]	AB22 XCI_MDO[0]/XVIN0_CR[1]	AB23 XCI_WEJ/XVIN0_CR[6]/XSC2_DATA	AB
AC	AC1 XDCLKO	AC2 XDCLKOJ2	AC3 XDCLKO2		AC5 XODT2		AC7 XMD2[0]		AC9 XMD2[9]		AC11 XDQS2[1]		AC13 XMD2[10]		AC15 XMD2[3]		AC17 XBA2[1]		AC19 XCI_VCC_ENJ/XVIN0_DE		AC21 XCI_MDI[6]/XVIN0_Y[5]	AC22 XCI_MOSTART/XVIN0_CB[7]	AC23 XCI_MDO[1]/XVIN0_CR[3]	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

Table 3-2. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	XDP[1]	F11	XVSSIO	M15	XVSSIO	V13	XVSSPST
A2	XDM[1]	F12	XEJ_SELECT/TVENC_HSYNC/ALISSI_DATA1	M16	XVDDCORE	V14	XMA2[10]
A3	XDM[0]	F13	XHDMI_HPD	M17	XCI_WAITJ/XVOUT0_CB[2]	V15	XMA2[14]
A4	XENET_TXN	F14	XEJ_TDI/AUD_I2SO_SDATA2/ALISSI_CLK/QAM_SSI_CLK	M18	XCI_ADDRESS[1]/XVOUT0_CB[7]	V16	XVDDCORE_CPU
A5	XENET_RXN	F15	XEJ_TDO/AUD_I2SO_SDATA1/ALISSI_VALID/QAM_SSI_VALID	M19	XCI_ADDRESS[5]/XVOUT0_CB[0]	V17	XCI_ADDRESS[8]/XVIN0_CR[0]
A6	TMDSDATAN[2]	F16	XEJ_TCLK/ALISSI_ERROR/QAM_SSI_ERROR	M20	XCI_ADDRESS[4]/XVOUT0_CB[1]	V18	XCI_DATA[7]/XVIN0_Y[6]
A7	TMDSDATAN[1]	F17	XUART_TX	M21	XSMD[6]/XSFLASH_MOSI/XSD_MMC_DATA[3]/XSD_DATA[3]	V19	XCI_IORDJ/XVIN0_CB[2]/AUD_I2SI_LRCLK
A8	TMDSDATAN[0]	F18	XPMU_GPIO[4]/AUD_I2SI_LRCLK/ALISSI_DATA0/QAM_SSI_DATA[0]	M22	XSMD[5]/XSFLASH_MISO/XSD_MMC_DATA[4]/XSD_CMD	V20	XCI_OEJ/XVIN0_CB[3]/AUD_I2SI_BCK
A9	TMDSCLKN	F19	XPMU_GPIO[3]/AUD_I2SI_DATA/ALISSI_CLK/QAM_SSI_CLK	N1	XDQM[1]	V21	XCI_MDO[7]/XVOUT0_Y[3]

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A10	XGPIO[4]	F20	XTSPI_VALID/ALISSI3_VALID/QAM_SPI_VALID/QAM_SSI_VALID	N2	XMD[9]	V22	XCI_MICLK/XVOUT0_Y[5]
A11	XSCL_3/MCU_DOCD_DATAO	F21	XTSPI_ERROR/ALISSI3_ERROR/QAM_SPI_ERROR/QAM_SSI_ERROR	N3	XBA[0]	W1	XMD[7]
A13	XVDAC_OUT3	F22	XTSPI_SYNC/ALISSI3_SYNC/QAM_SPI_SYNC/QAM_SSI_SYNC	N4	XMA[0]	W2	XMD[3]
A15	XSDA_1/XPCM_PCM_DO/AUD_XEJ_TDI	G1	XSRASJ	N5	XMA[5]	W3	XMD[5]
A17	XSCL_2/XUART2_RX	G2	XSCASJ	N6	XMA[3]	W4	XVSSPST_CLK
A19	XRXADC_IP	G3	XVSSPST	N7	XVSSPST	W5	XVDDO_CLK
A21	XPMU_VSSIO	G4	XRGMII_RXD[2]	N9	XVSSCORE	W6	XVSSPST
A22	XP_X27IN	G5	XRGMII_RX_CTL	N10	XVSSCORE	W7	XMA2[13]
A23	XPMU_VDDIO	G6	XGPIO[2]/DIGITAL_PLL_FOUT2/MCU_UART_RXDI	N11	XVSSCORE	W8	XVDDO
B1	XDP[2]	G10	XVDDIO	N12	XVSSCORE	W9	XMA2[7]
B2	XDM[2]	G11	XVDDIO	N13	XVSSCORE	W10	XVSSPST
B3	XDP[0]	G12	XVSSIO	N14	XVSSCORE	W11	XMA2[0]
B4	XENET_TXP	G13	XVSSIO	N15	XVSSCORE	W12	XVSSPST
B5	XENET_RXP	G14	XEJ_TRST/AUD_I2SO_SDATA3/ALISSI_DATA0/QAM_SSI_DATA[0]	N17	XVDDCORE	W13	XVSSPST
B6	TMDSDATAP[2]	G18	XPMU_GPIO[2]/AUD_I2SIO_MCLK/ALISSI_VALID/QAM_SSI_VALID	N18	XVDDCORE	W14	XMA2[1]
B7	TMDSDATAP[1]	G19	XPMU_GPIO[1]/XUART2_RX/TVENC_HSYNC/ALISSI_SYNC/QAM_SSI_SYNC	N19	XCI_ADDRESS[6]/XVOUT0_Y[6]	W15	XMA2[6]
B8	TMDSDATAP[0]	G20	XPMU_GPIO[0]/XUART2_TX/ALISSI_ERROR/QAM_SSI_ERROR	N20	XCI_RSTA/XVOUT0_Y[7]	W16	XCPLLAVSS
B9	TMDSCLKP	G21	XPCM_RFS/AUD_I2SO_SDATA2/AUD_I2SO_LRCLK_2/ALISSI3_DATA0	N21	XSMRDJ	W17	XCI_DATA[3]/XVIN0_HSYNC
B10	XGPIO[5]	G22	XPCM_DI/AUD_I2SO_SDATA3/AUD_I2SO_BCK_2/ALISSI3_DATA1	N22	XSMWRJ/XSD_MMC_RSTJ	W18	XCI_DATA[5]/XVIN0_Y[2]
B11	XSDA_3/MCU_DOCD_DATAI	G23	XGPIO[0]/XSC1_POWENJ/AUD_I2SO_SDATA0/ALISSI4_SYNC/AUD_I2SO_SDATA_2/XSMDQS	N23	XSMD[7]/XSFLASH_SCLK/XSD_MMC_DATA[5]/XSD_DATA[2]	W19	W19 XCI_CE1J/XVIN0_CB[0]/AUD_I2SIO_MCLK
B12	XVDAC_OUT1	H2	XWEJ	P2	XDQSJ[0]	W20	XCI_ADDR[10]/XVIN0_CB[1]/AUD_I2SI_DATA
B13	XVDAC_OUT4	H3	XSC1_CLK	P3	XDQS[0]	W21	XCI_MOVALA/XVOUT0_VSYNC
B14	XADAC_OL_P	H4	XRGMII_RXD[3]	P4	XVDDO	W22	XCI_MOCLK/XVOUT0_Y[0]
B15	XGPIO_PCM1/XPCM_RFS/AUD_XEJ_TDO	H5	XRGMII_RXD[1]	P5	XBA[2]	W23	XCI_MDO[6]/XVOUT0_Y[1]
B16	XGPIO_PCM2/XPCM	H6	XSC1_POWENJ	P6	XVSSPST	Y2	XCKE

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
	_PCM_DI/AUD_XEJ_TCLK						
B17	XSDA_2/XUART2_TX	H8	XVDDIO	P7	XVDDO	Y3	XBA[1]
B18	XIF_AGC_PDM/XSC1_DATA/ALISSI4_DATA1	H9	XVDDCORE	P9	XVSSCORE	Y4	XVDDCORE_DPLL
B19	XRXADC_IN	H15	XVDDCORE	P10	XVSSCORE	Y5	XVSSPST_CLK
B20	XPMU_GPIO[7]/AUD_I2SO_BCK/ALISSI4_CLK	H16	XVDDCORE	P11	XVSSCORE	Y6	XVDDO_CLK
B21	XP_X27OUT	H18	XPMU_DOWN	P12	XVSSCORE	Y7	XVSSPST
B22	XIR_RX	H19	XVDDCORE	P13	XVSSCORE	Y8	XVDDO
B23	XTSPI_DATA[0]/ALISSI2_DATA1/QAM_SPI_DATA[0]	H20	XVDDCORE	P14	XVSSCORE	Y9	XVSSPST
C1	XDP[3]	H21	XPCM_TFS/AUD_I2SI_DATA_2/ALISSI3_SYNC	P15	XVSSCORE	Y10	XMA2[3]
C2	XDM[3]	H22	XPCM_TCK/AUD_I2SIO_MCLK_2/ALISSI3_ERROR	P17	XVDDCORE	Y11	XBA2[2]
C3	XRGMII_MDIO	J1	XMD[4]	P18	XCI_ADDRESS[7]/XVOUT0_Y[4]	Y12	XVREF
C4	XENET_VSSA1	J2	XODT	P19	XVDDCORE_CPU	Y13	XVDDO
C5	XENET_PLL_VSSA	J3	XVSSPST	P20	XVDDCORE_CPU	Y14	XVSSPST
C6	XHDMI_GD	J4	XSC1_DATA	P21	XSMCLE	Y15	XMA2[11]
C7	XHDMI_GD	J5	XSC1_RST	P22	XSMCEJ0/XSFLASH_CSJ[1]	Y16	XMA2[8]
C8	XHDMI_GD	J6	XSC1_PRESJ	R1	XDQSJ[1]	Y17	XCPLLAVDD
C9	XHDMI_GD	J8	XVDDIO	R2	XDQS[1]	Y18	XCI_DATA[4]/XVIN0_Y[0]
C10	XHDMI_DDCCEC	J9	XVDDCORE	R3	XVSSPST	Y19	XCI_DATA[6]/XVIN0_Y[4]
C11	XCEC	J10	XVDDCORE	R4	XVREF	Y20	XCI_MDI[7]/XVIN0_Y[7]
C12	XVDAC_OUT2	J11	XVSSIO	R5	XVSSPST	Y21	XCI_MDO[4]/XVOUT0_PIXCLK
C13	XGPIO_127/XTUN_AGC_PDM/XIR_TX/AUD_XEJ_TRST/TVENC_VSYNC	J12	XVSSIO	R6	XMA[15]	Y22	XCI_MDO[5]/XVOUT0_HSYNC
C14	XADAC_OR_P	J13	XVSSIO	R7	XVSSPST	AA1	XMA[12]
C15	XSCL_1/XPCM_RCK/AUD_XEJ_TMS	J14	XVSSIO	R8	XVDDO	AA2	XMA[4]
C16	XSPDIF/MCU_DOCD_CLK	J15	XVSSIO	R9	XVSSCORE	AA3	XVSSCORE_DPLL
C17	XUART_RX	J16	XVDDCORE	R10	XVSSCORE	AA4	XVS33_DPLL
C18	XRXADC_AVS	J18	XDFTTM	R11	XVSSCORE	AA5	XSCASJ2
C19	XPMU_GPIO[8]/ALISSI4_DATA0	J19	XGPIO[3]/XSC1_CLK/ALISSI4_ERROR	R12	XVSSCORE	AA6	XMD2[4]
C20	XPMU_GPIO[6]/XSC1_PRESJ/AUD_I2SO_LRCLK/ALISSI4_VALID	J20	XCI_CD2J/XPCM_PCM_DI	R13	XVSSCORE	AA7	XDDR3_RESETJ2
C21	XTSPI_DATA[1]/ALISSI2_DATA0/QAM_SPI_DATA[1]	J21	XSMCEJ1/XSFLASH_CSJ[0]	R14	XVSSCORE	AA8	XMD2[11]
C22	XTSPI_DATA[3]/ALISSI2_VALID/QAM_SPI_DATA[3]	J22	XPCM_DO/AUD_I2SI_LRCLK_2/ALISSI3_VALID	R15	XVSSCORE	AA9	XMA2[5]
C23	XTSPI_DATA[2]/ALISSI2_CLK/QAM_SPI_DATA[2]	J23	XPCM_RCK/AUD_I2SO_SDATA1/AUD_I2SI_BCK_2/ALISSI3_CLK	R16	XVDDCORE	AA10	XDQM2[1]

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
D2	XRGMII_TXD[3]	K2	XMD[2]	R17	XVDDCORE_CPU	AA11	XVSSPST
D3	XRGMII_MDC	K3	XMD[6]	R18	XCI_ADDRESS[12]/XVOUT0_Y[2]	AA12	XVSSPST
D4	XRGMII_TXD[2]	K4	XDDR3_RESETJ	R19	XCI_ADDRESS[13]/XVIN0_CR[2]	AA13	XMD2[12]
D5	XAVDDUSBTX	K5	XVSSPST	R20	XCI_ADDRESS[14]/XVIN0_CR[4]/XSC2_CLK/TVENC_VSYNC	AA14	XMD2[8]
D6	XENET_VDDA1	K6	XMA[9]	R21	XP_CRSTJ	AA15	XVSSPST
D7	XENET_PLL_VDCORE	K7	XVSSCORE	R22	XSMWPJ/XSD_MMC_CMD	AA16	XMD2[7]
D8	XVDDIO	K9	XVSSCORE	R23	XSMALE/XSD_MMC_CLK	AA17	XVSSPST
D9	XHDMI_GD	K10	XVSSCORE	T2	XMD[12]	AA18	XMA2[12]
D10	XGPIO[6]	K11	XVSSCORE	T3	XMD[14]	AA19	XVSSPST
D11	XHDMI_VP	K12	XVSSCORE	T4	XVSSPST	AA20	XCI_MDI[3]/XVIN0_VSYNC
D12	XVDDIO	K13	XVSSCORE	T5	XMA[11]	AA21	XCI_MDO[2]/XVIN0_CR[5]/XSC2_POWENJ/TVENC_HSYNC
D13	XVSSCORE	K14	XVSSCORE	T6	XMA[10]	AA22	XCI_MDO[3]/XVIN0_CR[7]/XSC2_RST
D14	XVDAC_VDDA	K15	XVSSIO	T8	XVDDO	AA23	XCI_RDY/XVOUT0_DE/XSC2_PRESJ
D15	XADAC_VREF	K17	XCI_ADDRESS[0]/XVOUT0_CR[1]	T9	XVDDO	AB1	XDCLKOJ
D16	XVDD_ADAC_3	K18	XCI_DATA[0]/XVOUT0_CR[3]/XSC2_CLK/XPCM_TCK	T11	XVDDO	AB2	XVSSPST
D17	XRXADC_DVS	K19	K19 XCI_DATA[2]/XVOUT0_CR[7]/XSC2_PRESJ/XPCM_RFS	T12	XVDDO	AB3	XVD33_DPLL
D18	XRXADC_AVD	K20	XCI_DATA[1]/XVOUT0_CR[5]/XSC2_DATA/XPCM_PCM_DO	T15	XVDDCORE	AB4	XSRASJ2
D19	XMPLLAVDD	K21	XSMD[1]/XSD_MMC_DATA[6]	T17	XVDDCORE_CPU	AB5	XWEJ2
D20	XRXPLLAVDD	K22	XSMD[0]/XSD_MMC_DATA[7]	T18	XVDDCORE_CPU	AB6	XMD2[6]
D21	XTSPI_DATA[4]/ALISSI2_SYNC/QAM_SPI_DATA[4]	L1	XMD[11]	T19	XVDDCORE_CPU	AB7	XMD2[2]
D22	XTSPI_DATA[5]/ALISSI2_ERROR/QAM_SPI_DATA[5]	L2	XMD[0]	T20	XVDDCORE_CPU	AB8	XMD2[13]
E1	XRGMII_TX_CTL	L3	XVSSPST	T21	XCI_MDI[1]/XVOUT0_CR[4]/XSC2_POWENJ/XPCM_TFS	AB9	XMD2[15]
E2	XRGMII_RXC	L4	XMA[2]	T22	XCI_MDI[2]/XVOUT0_CR[6]/XSC2_RST/XPCM_RCK	AB10	XDQS2[0]
E3	XRGMII_TXC	L5	XVSSPST	U1	XMD[8]	AB11	XDQSJ2[0]
E4	XRGMII_TXD[0]	L6	XMA[13]	U2	XMD[10]	AB12	XDQSJ2[1]
E5	XAVDDUSBTX	L7	XVDDO	U3	XDQM[0]	AB13	XMD2[14]
E6	XRREF	L9	XVSSCORE	U4	XMA[6]	AB14	XDQM2[0]
E7	XENET_REXTA	L10	XVSSCORE	U5	XMA[1]	AB15	XMD2[1]
E8	XVDDIO	L11	XVSSCORE	U6	XMA[14]	AB16	XMD2[5]
E10	XHDMI_AVDD33	L12	XVSSCORE	U10	XVDDO	AB17	XCKE2
E11	XHDMI_VP	L13	XVSSCORE	U11	XVDDCORE	AB18	XMA2[4]
E12	XVDDIO	L14	XVSSCORE	U12	XVDDO	AB19	XCI_CD1J/XVIN0_PIXCLK
E13	XVDDCORE	L15	XVSSIO	U13	XVSSPST	AB20	XCI_MDI[4]/XVIN0_

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
							Y[1]
E14	XVDAC_VSSA	L17	XVDDCORE	U14	XVDDO	AB21	XCI_MDI[5]/XVIN0_Y[3]
E15	XVSS_ADAC_3	L18	XCI_REGJ/XVOUT0_CB[4]	U17	XVDDCORE_CPU	AB22	XCI_MDO[0]/XVIN0_CR[1]
E16	XEJ_TMS/TVENC_VSYNC/ALISSI_SYNC/QAM_SSI_SYNC	L19	XCI_ADDRESS[3]/XVOUT0_CB[3]	U18	XCI_ADDR[11]/XVIN0_CB[4]/AUD_I2SO_LRCLK	AB23	XCI_WEJ/XVIN0_CR[6]/XSC2_DATA
E17	XVSSCORE	L20	XCI_ADDRESS[2]/XVOUT0_CB[5]	U19	XCI_ADDR[9]/XVIN0_CB[6]/AUD_I2SO_SDATA0	AC1	XDCLKO
E18	XRXADC_DVD	L21	XSMD[4]/XSFLASH_WJ/XSD_MMC_DATA[0]/XSD_CLK	U20	XCI_IOWRJ/XVIN0_CB[5]/AUD_I2SO_BCK	AC2	XDCLKOJ2
E19	XPMU_GPIO[5]/XSC1_RST/AUD_I2SI_BCK/ALISSI_DATA1	L22	XSMD[3]/XSFLASH_HOLDJ/XSD_MMC_DATA[1]/XSD_DATA[0]	U21	XCI_MIVALA/XVOUT0_CB[6]	AC3	XDCLKO2
E20	XRXPLLAVSS	L23	XSMD[2]/XSD_MMC_DATA[2]/XSD_DATA[1]	U22	XCI_MISTART/XVOUT0_CR[0]	AC5	XODT2
E21	XTSPI_DATA[6]/ALISSI3_DATA1/QAM_SPI_DATA[6]	M2	XMD[15]	U23	XCI_MDI[0]/XVOUT0_CR[2]	AC7	XMD2[0]
E22	XTSPI_CLK/ALISSI3_CLK/QAM_SPI_CLK/QAM_SSI_CLK	M3	XMD[13]	V2	XMD[1]	AC9	XMD2[9]
E23	XTSPI_DATA[7]/ALISSI3_DATA0/QAM_SPI_DATA[7]/QAM_SSI_DATA[0]	M4	XVSSPST	V3	XMA[8]	AC11	XDQS2[1]
F2	XPHY_INT	M5	XMA[7]	V4	XVSSPST	AC13	XMD2[10]
F3	XRGMII_REF_CLK	M6	XVSSPST	V5	XVDDO	AC15	XMD2[3]
F4	XRGMII_RXD[0]	M7	XVDDO	V6	XVDDO	AC17	XBA2[1]
F5	XRGMII_TXD[1]	M9	XVSSCORE	V7	XVSSPST	AC19	XCI_VCC_ENJ/XVIN0_DE
F6	XAVSSUSBTX	M10	XVSSCORE	V8	XMA2[2]	AC21	XCI_MDI[6]/XVIN0_Y[5]
F7	XAVSSUSBTX	M11	XVSSCORE	V9	XMA2[9]	AC22	XCI_MOSTART/XVIN0_CB[7]
F8	XVDDIO	M12	XVSSCORE	V10	XBA2[0]	AC23	XCI_MDO[1]/XVIN0_CR[3]
F9	XGPIO[1]/XSPDIF/MCU_UART_TXD	M13	XVSSCORE	V11	XVSSPST		
F10	XHDMI_REXT	M14	XVSSCORE	V12	XMA2[15]		

4. Signal Description

Table 4-1. DDR3 SDRAM Interface

Name	Number	Type	Description
XMD[15:0]	16	B	DDR2/3 SDRAM data
XMA[15:0]	14	O	DDR2/3 SDRAM address
XDQM[1:0]	2	O	DDR2/3 SDRAM data mask
XDQS[1:0]	2	B	DDR2/3 SDRAM differential data strobe
XDQSJ[1:0]	2	B	DDR2/3 SDRAM differential data strobe
XCKE	1	O	DDR2/3 SDRAM clock enable
XSRASJ	1	O	DDR2/3 SDRAM row address strobe
XSCASJ	1	O	DDR2/3 SDRAM column address strobe
XWEJ	1	O	DDR2/3 SDRAM write enable
XCSJ	1	O	DDR2/3 SDRAM chip select
XODT	1	I	DDR2/3 SDRAM On die termination
XDCLK_O	1	O	DDR2/3 SDRAM differential clock
XDCLKJ_O	1	O	DDR2/3 SDRAM differential clock
XBA[2:0]	3	O	DDR2/3 SDRAM bank address
XVREF	1	I	DDR2/3 SDRAM reference voltage
XRESET	1	O	DDR3 SDRAM Reset

Table 4-2. 2nd Channel DDR2/3 SDRAM Interface

Name	Number	Type	Description
XMD2[15:0]	16	B	DDR2/3 SDRAM data
XMA2[15:0]	14	O	DDR2/3 SDRAM address
XDQM2[1:0]	2	O	DDR2/3 SDRAM data mask
XDQS2[1:0]	2	B	DDR2/3 SDRAM differential data strobe
XDQS2J[1:0]	2	B	DDR2/3 SDRAM differential data strobe
XCKE2	1	O	DDR2/3 SDRAM clock enable
XSRAS2J	1	O	DDR2/3 SDRAM row address strobe
XSCAS2J	1	O	DDR2/3 SDRAM column address strobe
XWE2J	1	O	DDR2/3 SDRAM write enable
XCS2J	1	O	DDR2/3 SDRAM chip select
XODT2	1	I	DDR2/3 SDRAM On die termination
XDCLK2_O	1	O	DDR2/3 SDRAM differential clock
XDCLK2J_O	1	O	DDR2/3 SDRAM differential clock
XBA2[2:0]	3	O	DDR2/3 SDRAM bank address
XVREF2	1	I	DDR2/3 SDRAM reference voltage
XRESET2	1	O	DDR3 SDRAM Reset

Table 4-3. DDR2/3 SDRAM Power/Ground

Name	Number	Type	Description
XVSSPST	1	G	DDR2 SDRAM IO Ground
XVDDO	1	P	DDR2/3 SDRAM IO Power (1.8V/1.5V)
XVDDCORE	1	P	DDR2/3 SDRAM Core Power (1.0V)
XVSSCORE	1	G	DDR2/3 SDRAM Core Ground

Table 4-4. Serial Flash Interface

Name	Number	Type	Description
XSFLASH_CSJ	1	O	Serial flash chip selection
XSFLASH_SCLK	1	O	Serial flash serial clock
XSFLASH_WJ	1	B	Serial flash write enable/SQI SIO2
XSFLASH_MISO	1	B	Serial flash master in slave out/SQI SIO1
XSFLASH_MOSI	1	B	Serial flash master out slave in/SQI SIO0
XSFLASH_HOLDJ	1	B	Serial flash hold enable/SQI SIO3

Table 4-5. Audio I2S OUT Interface

Name	Number	Type	Description
XI2SO_DATA0	1	O	I2S data0 output
XI2SO_DATA1	1	O	I2S data0 output
XI2SO_BCK	1	O	Bit clock for I2S output
XI2SO_LRCK	1	O	Channel clock for I2S output(fs)
XI2SO_MCLK	1	O	Over sample clock for I2S DAC(for delta-sigma modulator and digital filter)

Table 4-6. Serial Communication Bus Interface (1)

Name	Number	Type	Description
XSPDIF	1	O	Spdif data

Table 4-7. Serial Communication Bus Interface, total 2 sets

Name	Number	Type	Description
XSDA	1	B	Serial bus data
XSCL	1	B	Serial bus clock

Table 4-8. Consumer IR RX Interface

Name	Number	Type	Description
XIR_RX	1	I	Consumer Infra-red remote controller / wireless keyboard

Table 4-9. RS-232 UART, total 2 set

Name	Number	Type	Description
XUART_TX	1	O	Transmitted Data (TD) Outgoing Data to a DCE
XUART_RX	1	I	Received Data (RD) Incoming Data from a DCE

Table 4-10. ISO7816 Interface, total 2 sets

Name	Number	Type	Description
XSC_POWENJ	1	O	Smart card output power enable, low active
XSC_PRESJ	1	I	Smart card detect input
XSC_RST	1	O	Smart card output reset
XSC_DATA	1	B	Smart card data line, bi-direction
XSC_CLK	1	O	Smart card output clock

Table 4-11. EJTAG Interface (5)

Name	Number	Type	Description
XEJ_TDI	1	O	Serial Test Data Input
XEJ_TMS	1	O	Test Mode Select

Name	Number	Type	Description
XEJ_TCLK	1	O	Test Clock
XEJ_TRSTJ	1	O	Test Reset
XEJ_TDI	1	O	Serial Test Data Input

Table 4-12. External TS Stream Interface

Name	Number	Type	Description
XTSPI_CLK	1	I	External MPEG TS CLOCK INPUT
XTSPI_VALID	1	I	External MPEG TS PACKET START INPUT
XTSPI_ERROR	1	I	External MPEG TS VALID DATA INPUT
XTSPI_SYNC	1	I	External MPEG TS DATA INPUT
XTSPI_DATA[7:0]	8	I	External MPEG TS ERROR INPUT

Table 4-13. External Serial TS Stream Interface (5), total 4 sets

Name	Number	Type	Description
XTSSI_CLK	1	I	External Serial TS CLOCK INPUT
XTSSI_VALID	1	I	External Serial TS PACKET START INPUT
XTSSI_ERROR	1	I	External Serial TS ERROR INPUT
XTSSI_SYNC	1	I	External Serial TS VALID DATA INPUT
XTSSI_DATA[1:0]	2	I	External Serial TS DATA INPUT

Table 4-14. MPEG SPI Output Interface

Name	Number	Type	Description
QAM_SPI_CLK	1	O	MPEG TS CLOCK output
QAM_SPI_VALID	1	O	MPEG TS PACKET START output
QAM_SPI_ERROR	1	O	MPEG TS VALID DATA output
QAM_SPI_SYNC	1	O	MPEG TS DATA output
QAM_SPI_DATA[7:0]	8	O	MPEG TS ERROR output

Table 4-15. MPEG SSI Output Interface

Name	Number	Type	Description
QAM_SSI_CLK	1	O	MPEG Serial TS CLOCK output
QAM_SSI_VALID	1	O	MPEG Serial TS PACKET START output
QAM_SSI_ERROR	1	O	MPEG Serial TS ERROR output
QAM_SSI_SYNC	1	O	MPEG Serial TS VALID DATA output
QAM_SSI_DATA[1:0]	2	O	MPEG Serial TS DATA output

Table 4-16. RMII Interface

Name	Number	Type	Description
XRMII_REF_CLK	1	O	RMII reference clock
XRMII_CRS_DV	1	I	RMII receive data valid
XRMII_RXD[1:0]	2	I	RMII rx data
XRMII_TX_EN	1	O	RMII tx transmit enable
XRMII_TXD[1:0]	2	O	RMII tx data
XRMII_RX_ER	1	I	RMII receive error notice
XRMII_MDIO	1	B	RMII management data input/output
XRMII_MDC	1	O	RMII management clock

Name	Number	Type	Description
XRMII_INT	1	I	RMII interrupt

Table 4-17. Nand FLASH Interface

Name	Number	Type	Description
XNF_WPJ	1	O	Nand flash write protect
XNF_CLE	1	O	Nand flash command latch enable
XNF_ALE	1	O	Nand flash address latch enable
XNF_WEJ	1	O	Nand flash write enable
XNF_CEJ	1	O	Nand flash chip select
XNF_REJ	1	O	Nand flash read enable
XNF_DATA[7:0]	8	B	Nand flash data

Table 4-18. System Interface (3)

Name	Number	Type	Description
XDFT_SE	1	I	DFT test mode signal
XDFT_TM	1	I	DFT test enable signal
XP_CRSTJ	1	I	Chip cold reset signal

Table 4-19. USB2.0 Controller

Name	Number	Type	Description
XUSB_DM	4	B	USB signal DM
XUSB_DP	4	B	USB signal DP
XUSB_REXT	1	B	USB IO reference current source pin
XUSB_AVSS33	0	G	USB analog ground (Down Bond)
XUSB_AVDD33	1	P	USB 3.3v analog power

Table 4-20. Power/Ground (4)

Name	Number	Type	Description
XVDDCORE	1	P	Digital Core Power
XVSSCORE	1	G	Digital Core Ground
XVDDIO	1	P	Digital IO Power 3.3v
XVSSIO	1	G	Digital IO Ground

Table 4-21. General Purpose IO (7)

Name	Number	Type	Description
XGPIO[6:0]	7	B	General Purpose IO

Table 4-22. RXADC/AGCADC

Name	Number	Type	Description
XRXADC_AVD	1	P	ADC Analog 3.3V Power
XRXADC_DVD	1	P	ADC Digital 3.3V Power
XAGCADC_VSS	1	G	AGCADC Core Power Ground
XRXADC_AVS	1	G	ADC Analog Ground
XRXADC_DVS	1	G	ADC Digital Ground
XRXADC_IP	1	AI	I channel ADC positive input
XRXADC_IN	1	AI	I channel ADC negative input
XRXADC_QP	1	AI	Q channel ADC positive input

Name	Number	Type	Description
XRXADC_QN	1	AI	Q channel ADC negative input
XAGCADC_IP	1	AI	AGCADC Analog Input

Table 4-23. Audio DAC

Name	Number	Type	Description
XVDD_ADAC	1	P	Audio DAC Analog 3.3V Power
XVSS_ADAC	1	P	Audio DAC Analog Ground
XADAC_OR_P	1	AO	Audio DAC Right Channel output
XADAC_OL_P	1	AO	Audio DAC Left Channel output
XADAC_VREF	1	AB	Audio DAC Reference Voltage

Table 4-24. Video DAC

Name	Number	Type	Description
XVDAC_VDDA	1	P	Video DAC Analog 3.3V Power
XVDAC_VSSA	1	G	Video DAC Analog Ground
XVDAC_REXT	1	AO	Video DAC Reference node for bias circuits
XVDAC_OUT1	1	AO	Video DAC Analog output
XVDAC_OUT2	1	AO	Video DAC Analog output
XVDAC_OUT3	1	AO	Video DAC Analog output
XVDAC_OUT4	1	AO	Video DAC Analog output

Table 4-25. PLL

Name	Number	Type	Description
XRXPLLAVDD	1	P	PLL Anal
XDVDD	1	P	PLL Analog 3.3 Power
XPLLAVSS	1	AO	PLL Analog Ground
XPLLAVDD	1	AO	RXPLL Analog 3.3 Power
XRXPLLAVSS	1	AO	RXPLL Analog Ground
XP_X27IN	1	AI	Crystal Pad Input
XP_X27OUT	1	AO	Crystal Pad Output

Table 4-26. HDMI PHY Interface, EDDC function implemented by I2C

Name	Number	Type	Description
XHDMI0_N	1	A	TMDS Data0-
XHDMI0_P	1	A	TMDS Data0+
XHDMI1_N	1	A	TMDS Data1-
XHDMI1_P	1	A	TMDS Data1+
XHDMI2_N	1	A	TMDS Data2-
XHDMI2_P	1	A	TMDS Data2+
XHDMI_CLK_N	1	A	TMDS Clock-
XHDMI_CLK_P	1	A	TMDS Clock+
XHDMI_VD33	1	P	Power (3.3V)
XEDDC_CLK	1	B	Enhanced Display Data Channel(Clock),XSCL2
XEDDC_DATA	1	B	Enhanced Display Data Channel(Data),XSDA2
XHTPG	1	I	Hot Plug Detect Signal
XCEC	1	B	Consumer Electronics Control Signal

5. DC Characteristics

Table 5-1. DC Characteristics

VDDP-VSSP = 3.3V ±10%, Ta = 25°C, Crystal frequency is XP_X27IN = 27MHz.

Symbol	Parameter	Test Condition	Min.	Typical	Max.	Unit	Note
XSPLLAVDD	Analog power for SPLL		2.97	3.3	3.63	V	
XRXPLLAVDD	Analog power for RXPLL		2.97	3.3	3.63	V	
XCPLLAVDD	PLL power for CA9		2.97	3.3	3.63	V	
XPMU_VDDIO	Analog Power for PMU		2.97	3.3	3.63	V	
XVDD_ADAC	Analog Power for Audio DAC		2.97	3.3	3.63	V	
XVDAC_VDDA	Analog power for Video DAC		2.97	3.3	3.63	V	
XRXADC_AVD	Analog power for RXADC		2.97	3.3	3.63	V	
XRXADC_DVD	Digital power for RXADC		2.97	3.3	3.63	V	
XENET_VDDA1	Analog power for ENET		2.97	3.3	3.63	V	
XENET_PLL_VDCORE	PLL power for ENET		1.02	1.06	1.09	V	
XAVDDUSBTX	Analog power for USB		2.97	3.3	3.63	V	
XHDMI_AVDD33	Analog Power for HDMI PHY		2.97	3.3	3.63	V	
XHDMI_VP	Analog Core Power for HDMI		1.02	1.06	1.09	V	
XVDDO	Digital power for DDR		1.425	1.5	1.575	V	
XVD33_DPLL	PLL power for DDR		2.97	3.3	3.63	V	
XVDDO_CLK	Digital power for DDR CLK I/O		1.425	1.5	1.575	V	
XVDDCORE_DPLL	Digital core power for DDR CLK I/O		1.02	1.06	1.09	V	
XVDDIO	Digital power supply for I/O		2.97	3.3	3.63	V	
XVDDCORE	Digital power supply for core		1.02	1.06	1.09	V	
XVDDCORE_CPU	Digital core power supply for CA9		1.27	1.31	1.34	V	
I_VDDCORE	Operating Supply Current, for all VDD=1.06V			TBD	TBD	mA	
I_VDDCORE_CPU	Operating Supply Current for CA9, for all VDD=1.31V			TBD	TBD	mA	
I_VDDIO	Operating Supply Current for I/O, for all VDD=3.3V			TBD	TBD	mA	
I_VDDO	Operating Supply Current for DDR, for all VDD=1.5V			TBD	TBD	mA	
Pd	Power Dissipation	Vin=Max		TBD	TBD	W	
Ipwdn_VDDCORE	1.06V digital core power down current	Power down all functions		TBD	TBD	mA	
Ipwdn_VDDCORE_CPU	1.31V CA9 digital core power down	Power down all functions		TBD	TBD	mA	

Symbol	Parameter	Test Condition	Min.	Typical	Max.	Unit	Note
	current						
Ipwdn_VDDIO	3.3V I/O digital core power down current	Power down TV DACs		TBD	TBD	mA	
Ipwdn_VDDO	1.5V DDR digital core power down current	Power down DDR3		TBD	TBD	mA	
T_pwd	Total Power Down	PMU Power Down mode			TBD	W	
Llk	Input Leakage		-10		+10	μA	
VOL	Output Voltage Low				0.4	V	
VOH	Output Voltage High		2.4			V	
VIH	Input Voltage High		2.0		5.5	V	
VIL	Input Voltage Low		-0.3		0.8	V	

Table 5-2. DC Characteristics under 60°C

VDDP-VSSP = 3.3V ±10%, Ta = 60°C, Crystal frequency XP_X27IN = 27MHz.

Symbol	Parameter	Test Condition	Min.	Typical	Max.	Unit	Note
I_VDDCORE	Operating Supply Current, for all VDD=1.06V			TBD	TBD	mA	
I_VDDCORE_CPU	Operating Supply Current for CA9, for all VDD=1.31V			TBD	TBD	mA	
I_VDDIO	Operating Supply Current for I/O, for all VDD=3.3V			TBD	TBD	mA	
I_VDDO	Operating Supply Current for DDR, for all VDD=1.5V			TBD	TBD	mA	
Tc	IC Surface Temperature		0		120	°C	
Ta	Operating Environment Temperature		0		60	°C	

Note:

A: As VDDCORE and VDDCORE_CPU core power current are almost TBD and TBD, DC-DC and inductance devices need to be at least TBD for each core power.

B: The IC surface temperature(Tc) should not exceed 120°C when the system operates in a high temperature environment(Ta) within the case. A heat sink may be needed on the IC to control Tc<120°C for different case conditions.

6. AC Characteristics

6.1 Power up Timing Requirement

Signals involved in this sequence are: VDDIO, VDDCORE and C_RST# (cold reset signal). We should follow that the C_RST#(cold reset signal) is always the last signal. The below figure shows that sequence.

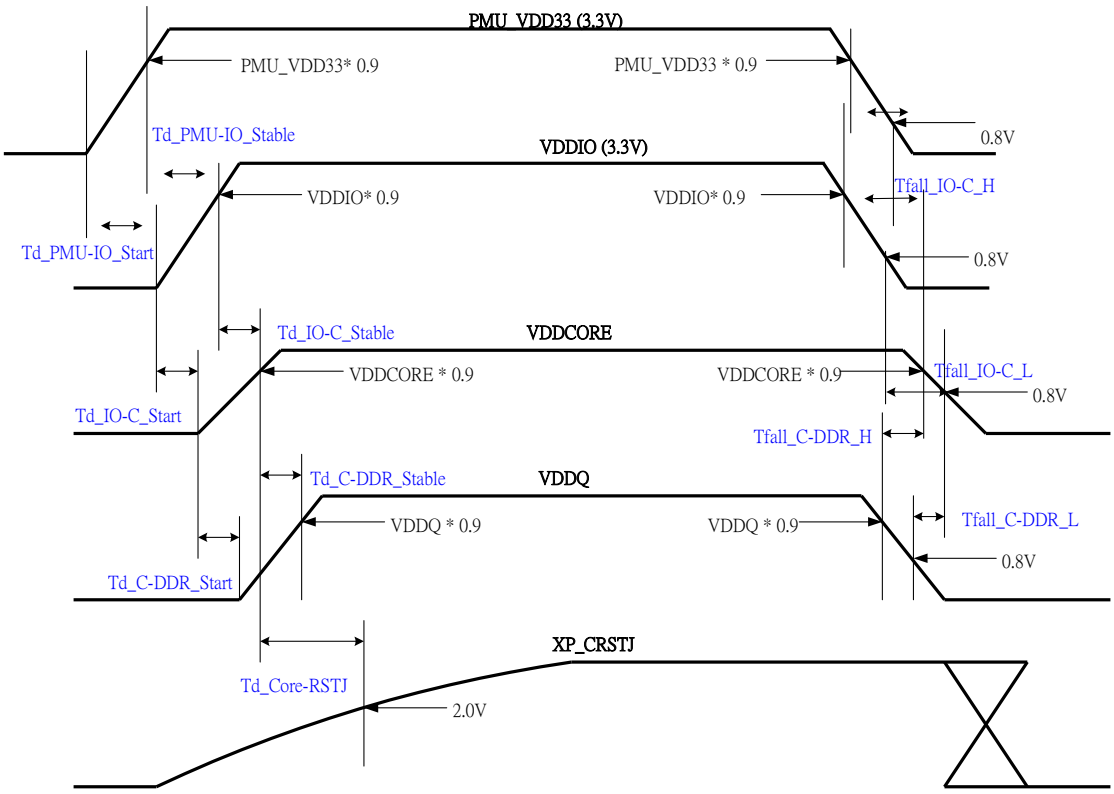


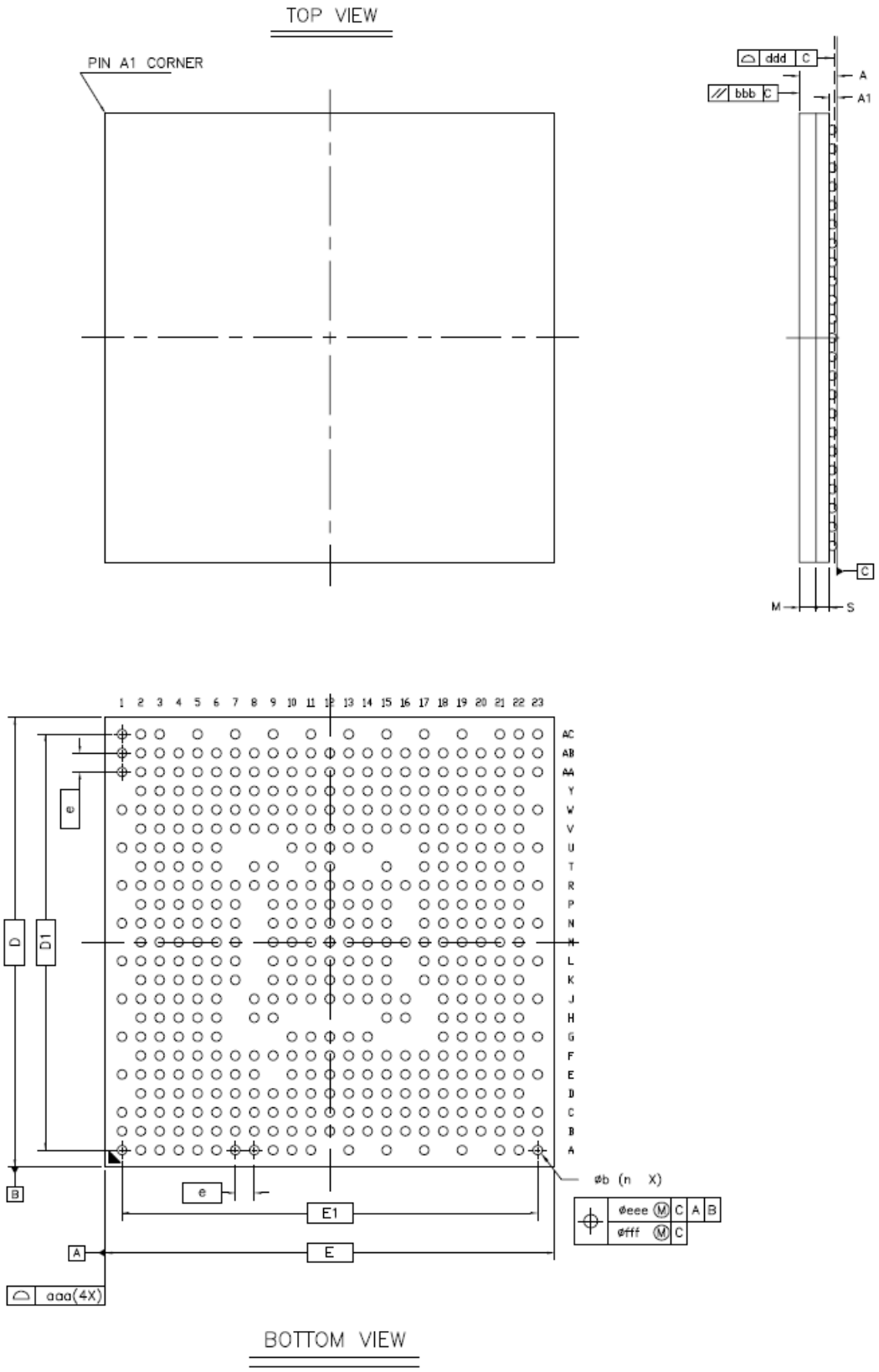
Figure 6-1. Power up and Power down Sequence

Table 6-1. Power up and Power down Sequence Parameters

Name	Description	Value			Unit	Note
		Min.	Typical	Max.		
Td_PMU-IO_Start	Distance from PMU IO power start rise to System IO power start rise	0		70	ms	
Td_PMU-IO_Stable	Distance from PMU IO power stable to System IO power stable	2		70	ms	
Td_IO-C_Start	Distance from IO power start rise to core power start rise	0		N/A	ms	Note 1
Td_IO-C_Stable	Distance from IO power stable to core power stable	0		N/A	ms	
Td_C-DDR_Start	Distance from core power start rise to DDR power start rise	-2		2	ms	
Td_C-DDR_Stable	Distance from core power stable to DDR power stable	-2		2	ms	Note 1
Td_Core-RSTJ	Distance from CPU core power stable to cold reset rise up to 2.0V	5			ms	
Tfall_IO-C_H	Distance from IO power start shut down to core power start shut down	0			ms	
Tfall_IO-C_L	Distance from IO power down to 0.8V to core power down to 0.8V				ms	Note 2

Note1: Actually there is no absolute value about Td_C-DDR_start, Td_C-DDR_stable, Tfall_C-DDR_H and Tfall_C-DDR_L, so it is not required that VDDO must be earlier than VDDCORE at system power-up.
Note 2: There is 8024 to control CA's input/output. VDDIO falling will cause 8024 power down.

7. Package Information



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			SBS LFBGA		
Body Size:	X	E	19.000		
	Y	D	19.000		
Ball Pitch :		e	0.800		
Total Thickness :		A			1.700
Mold Thickness :		M	0.700	Ref.	
Substrate Thickness :		S	0.560	Ref.	
Ball Diameter :			0.400		
Stand Off :		A1	0.270	–	0.370
Ball Width :		b	0.370	–	0.470
Package Edge Tolerance :		aaa	0.150		
Mold Parallelism :		bbb	0.350		
Coplanarity:		ddd	0.200		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.080		
Ball Count :		n	462		
Edge Ball Center to Center :	X	E1	17.600		
	Y	D1	17.600		

8. Order Information

Part No.	Package
M3733	462-pin FBGA

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