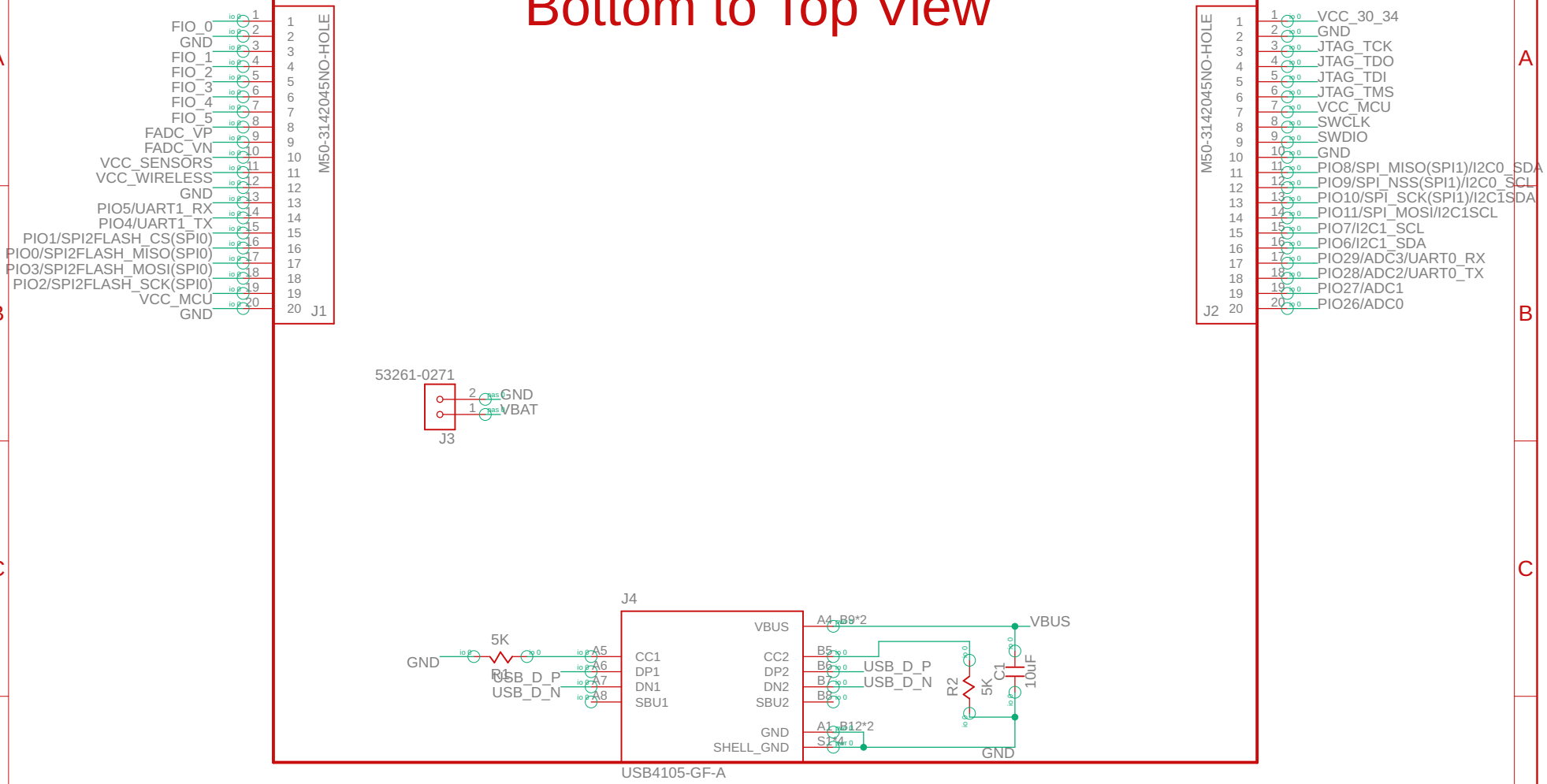
Bottom to Top View



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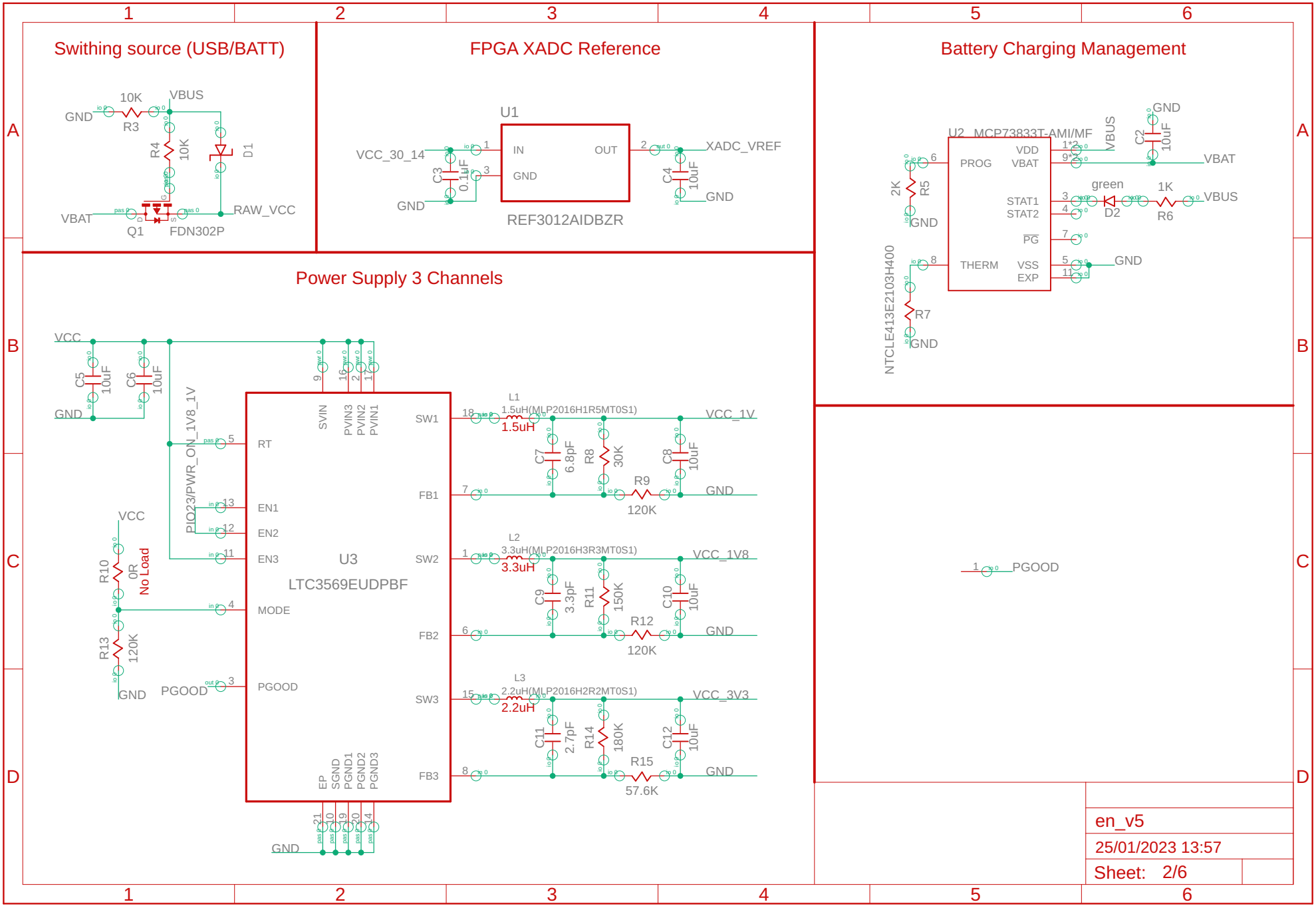
Swithing source (USB/BATT)
10K
R3
VBUS
GND
R4
10K
D1
VBAT
Q1
FDN302P
RAW_VCC
FPGA XADC Reference
U1
VCC_30_14
IN
OUT
XADC_VREF
C3
0.1uF
GND
C4
10uF
GND
REF3012AIDBZR
Battery Charging Management
U2 MCP73833T-AMI/MF
VBUS
C2
10uF
GND
VBAT
PROG
VDD
VBAT
2K
R5
GND
green
1K
R6
VBUS
D2
STAT1
STAT2
PG
THERM
VSS
EXP
GND
NTCLE413E2103H400
R7
GND
Power Supply 3 Channels
VCC
C5
10uF
C6
10uF
GND
PIO23/PWR_ON_1V8_1V
SVIN
PVIN3
PVIN2
PVIN1
RT
EN1
EN2
EN3
MODE
PGOOD
U3
LTC3569EUDPBF
SW1
FB1
SW2
FB2
SW3
FB3
EP
SGND
PGND1
PGND2
PGND3
L1
1.5uH(MLP2016H1R5MT0S1)
1.5uH
C7
6.8pF
R8
30K
C8
10uF
R9
120K
VCC_1V
L2
3.3uH(MLP2016H3R3MT0S1)
3.3uH
C9
3.3pF
R11
150K
C10
10uF
R12
120K
VCC_1V8
L3
2.2uH(MLP2016H2R2MT0S1)
2.2uH
C11
2.7pF
R14
180K
C12
10uF
R15
57.6K
VCC_3V3
R10
0R
No Load
R13
120K
PGOOD
PGOOD
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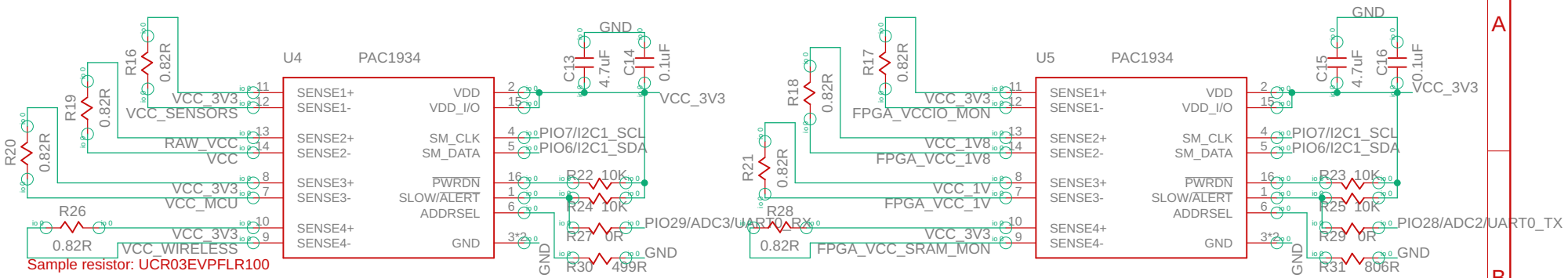
Power/Energy Meter



Sample resistor: UCR03EVPFLR100

The PWDOWN and alert signal are hardly pulled-up to VCC, which means the hardware is set to SLOW mode.
(To disable SLOW mode, you need to enable the alert pin in the software)

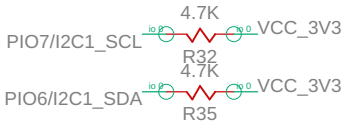
The 0R resistors(R27, R29) to alert can be installed depending on your application. Once it is installed, the ADC2 and ADC should not be used.

Power Control (ON/OFF)

1. PIO23 MUST be set to HIGH before enable the 3.3V Power of the FPGA.
2. Turning PIO21 to LOW will enable the 3.3V power rail to the FPGA including the external SRAM.

To turn off the SRAM entirely, you need to desolder the 100Ohm resistor.

I2C Pullup Resistors



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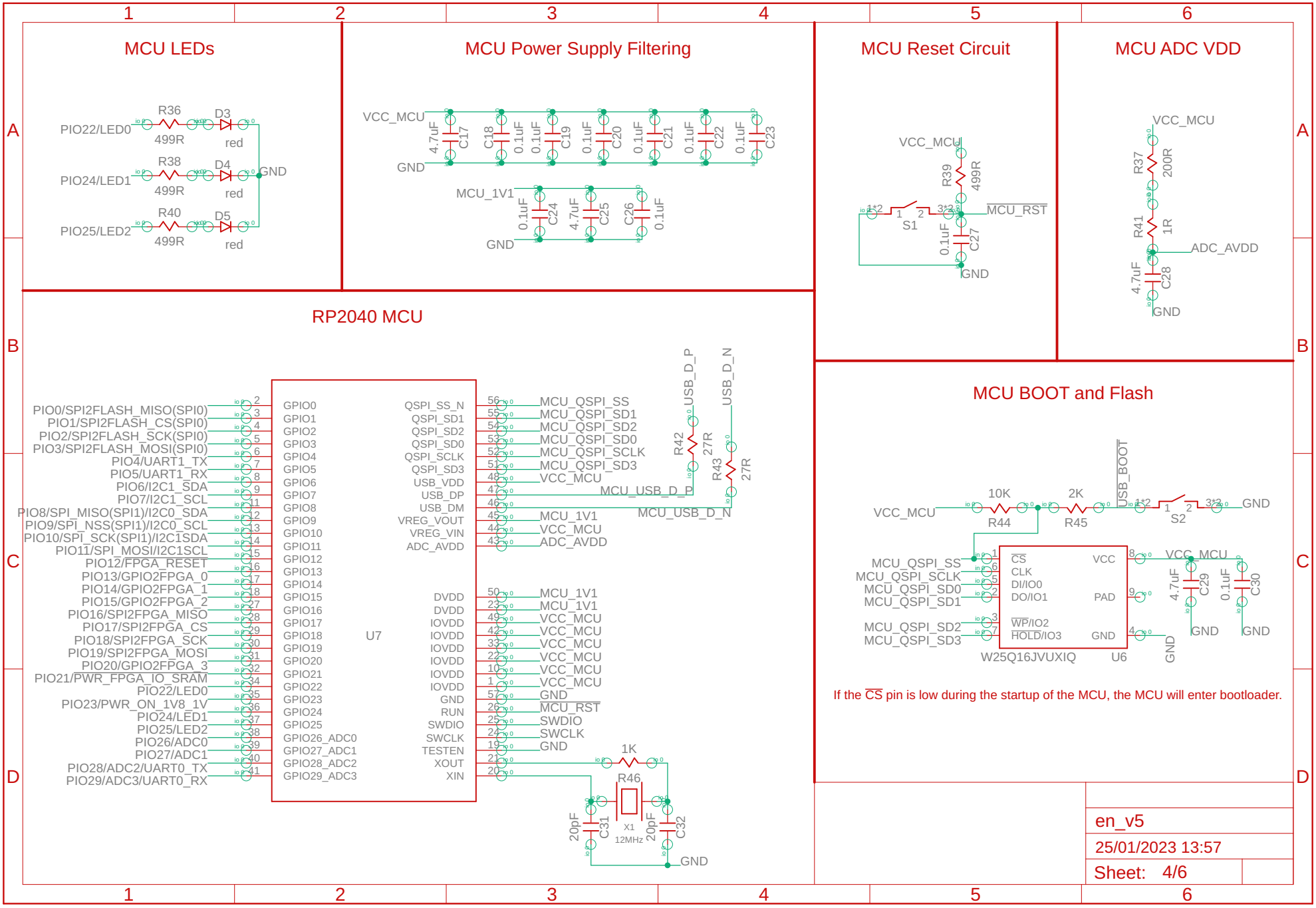
MCU LEDs
PIO22/LED0
R36
499R
D3
red
PIO24/LED1
R38
499R
D4
red
GND
PIO25/LED2
R40
499R
D5
red
MCU Power Supply Filtering
VCC_MCU
4.7uF
C17
C18
0.1uF
C19
C20
C21
C22
C23
GND
MCU_1V1
C24
C25
C26
MCU Reset Circuit
R39
499R
S1
MCU_RST
C27
MCU ADC VDD
R37
200R
R41
1R
ADC_AVDD
C28
RP2040 MCU
U7
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
GPIO25
GPIO26_ADC0
GPIO27_ADC1
GPIO28_ADC2
GPIO29_ADC3
PIO0/SPI2FLASH_MISO(SPI0)
PIO1/SPI2FLASH_CS(SPI0)
PIO2/SPI2FLASH_SCK(SPI0)
PIO3/SPI2FLASH_MOSI(SPI0)
PIO4/UART1_TX
PIO5/UART1_RX
PIO6/I2C1_SDA
PIO7/I2C1_SCL
PIO8/SPI_MISO(SPI1)/I2C0_SDA
PIO9/SPI_NSS(SPI1)/I2C0_SCL
PIO10/SPI_SCK(SPI1)/I2C1SDA
PIO11/SPI_MOSI/I2C1SCL
PIO12/FPGA_RESET
PIO13/GPIO2FPGA_0
PIO14/GPIO2FPGA_1
PIO15/GPIO2FPGA_2
PIO16/SPI2FPGA_MISO
PIO17/SPI2FPGA_CS
PIO18/SPI2FPGA_SCK
PIO19/SPI2FPGA_MOSI
PIO20/GPIO2FPGA_3
PIO21/PWR_FPGA_IO_SRAM
PIO22/LED0
PIO23/PWR_ON_1V8_1V
PIO24/LED1
PIO25/LED2
PIO26/ADC0
PIO27/ADC1
PIO28/ADC2/UART0_TX
PIO29/ADC3/UART0_RX
QSPI_SS_N
QSPI_SD1
QSPI_SD2
QSPI_SD0
QSPI_SCLK
QSPI_SD3
USB_VDD
USB_DP
USB_DM
VREG_VOUT
VREG_VIN
ADC_AVDD
DVDD
IOVDD
GND
RUN
SWDIO
SWCLK
TESTEN
XOUT
XIN
MCU_QSPI_SS
MCU_QSPI_SD1
MCU_QSPI_SD2
MCU_QSPI_SD0
MCU_QSPI_SCLK
MCU_QSPI_SD3
VCC_MCU
MCU_USB_D_P
MCU_USB_D_N
MCU_1V1
ADC_AVDD
R42
27R
R43
27R
USB_D_P
USB_D_N
MCU_RST
SWDIO
SWCLK
1K
R46
X1
12MHz
20pF
C31
20pF
C32
MCU BOOT and Flash
USB_BOOT
10K
R44
2K
R45
S2
CS
CLK
DI/IO0
DO/IO1
WP/IO2
HOLD/IO3
VCC
PAD
GND
W25Q16JVUXIQ
U6
C29
C30
If the CS pin is low during the startup of the MCU, the MCU will enter bootloader.
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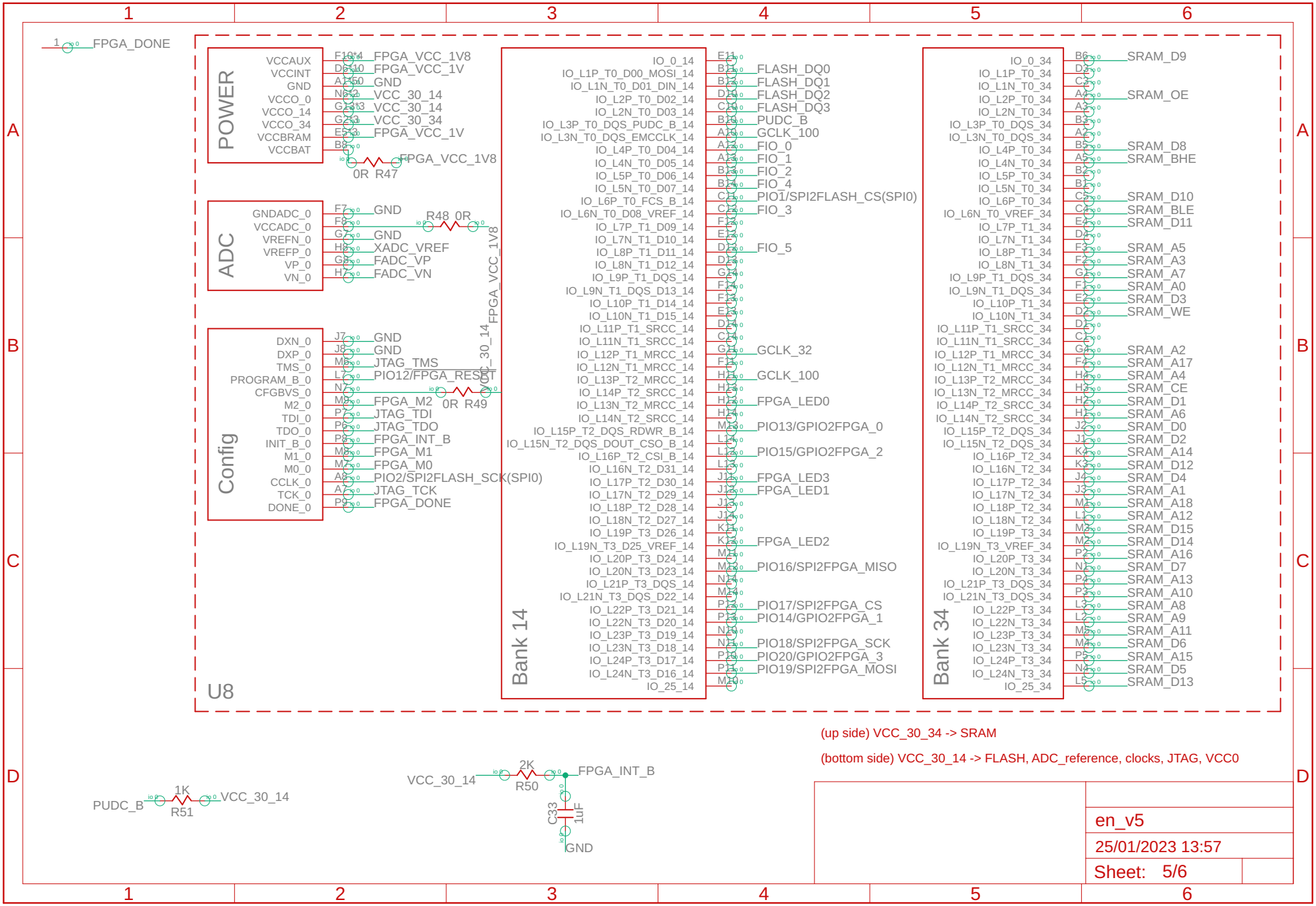
FPGA_DONE
POWER
VCCAUX
VCCINT
GND
VCCO_0
VCCO_14
VCCO_34
VCCBRAM
VCCBAT
FPGA_VCC_1V8
FPGA_VCC_1V
GND
VCC_30_14
VCC_30_14
VCC_30_34
FPGA_VCC_1V
FPGA_VCC_1V8
0R R47
ADC
GNDADC_0
VCCADC_0
VREFN_0
VREFP_0
VP_0
VN_0
GND
R48 0R
GND
XADC_VREF
FADC_VP
FADC_VN
Config
DXN_0
DXP_0
TMS_0
PROGRAM_B_0
CFGBVS_0
M2_0
TDI_0
TDO_0
INIT_B_0
M1_0
M0_0
CCLK_0
TCK_0
DONE_0
GND
GND
JTAG_TMS
PIO12/FPGA_RESET
VCC_30_14
FPGA_M2 0R R49
JTAG_TDI
JTAG_TDO
FPGA_INT_B
FPGA_M1
FPGA_M0
PIO2/SPI2FLASH_SCK(SPI0)
JTAG_TCK
FPGA_DONE
U8
Bank 14
FLASH_DQ0
FLASH_DQ1
FLASH_DQ2
FLASH_DQ3
PUDC_B
GCLK_100
FIO_0
FIO_1
FIO_2
FIO_4
PIO1/SPI2FLASH_CS(SPI0)
FIO_3
FIO_5
GCLK_32
GCLK_100
FPGA_LED0
PIO13/GPIO2FPGA_0
PIO15/GPIO2FPGA_2
FPGA_LED3
FPGA_LED1
FPGA_LED2
PIO16/SPI2FPGA_MISO
PIO17/SPI2FPGA_CS
PIO14/GPIO2FPGA_1
PIO18/SPI2FPGA_SCK
PIO20/GPIO2FPGA_3
PIO19/SPI2FPGA_MOSI
Bank 34
SRAM_D9
SRAM_OE
SRAM_D8
SRAM_BHE
SRAM_D10
SRAM_BLE
SRAM_D11
SRAM_A5
SRAM_A3
SRAM_A7
SRAM_A0
SRAM_D3
SRAM_WE
SRAM_A2
SRAM_A17
SRAM_A4
SRAM_CE
SRAM_D1
SRAM_A6
SRAM_D0
SRAM_D2
SRAM_A14
SRAM_D12
SRAM_D4
SRAM_A1
SRAM_A18
SRAM_A12
SRAM_D15
SRAM_D14
SRAM_A16
SRAM_D7
SRAM_A13
SRAM_A10
SRAM_A8
SRAM_A9
SRAM_A11
SRAM_D6
SRAM_A15
SRAM_D5
SRAM_D13
PUDC_B
1K
R51
VCC_30_14
VCC_30_14
2K
R50
FPGA_INT_B
C33
1uF
GND
(up side) VCC_30_34 -> SRAM
(bottom side) VCC_30_14 -> FLASH, ADC_reference, clocks, JTAG, VCC0
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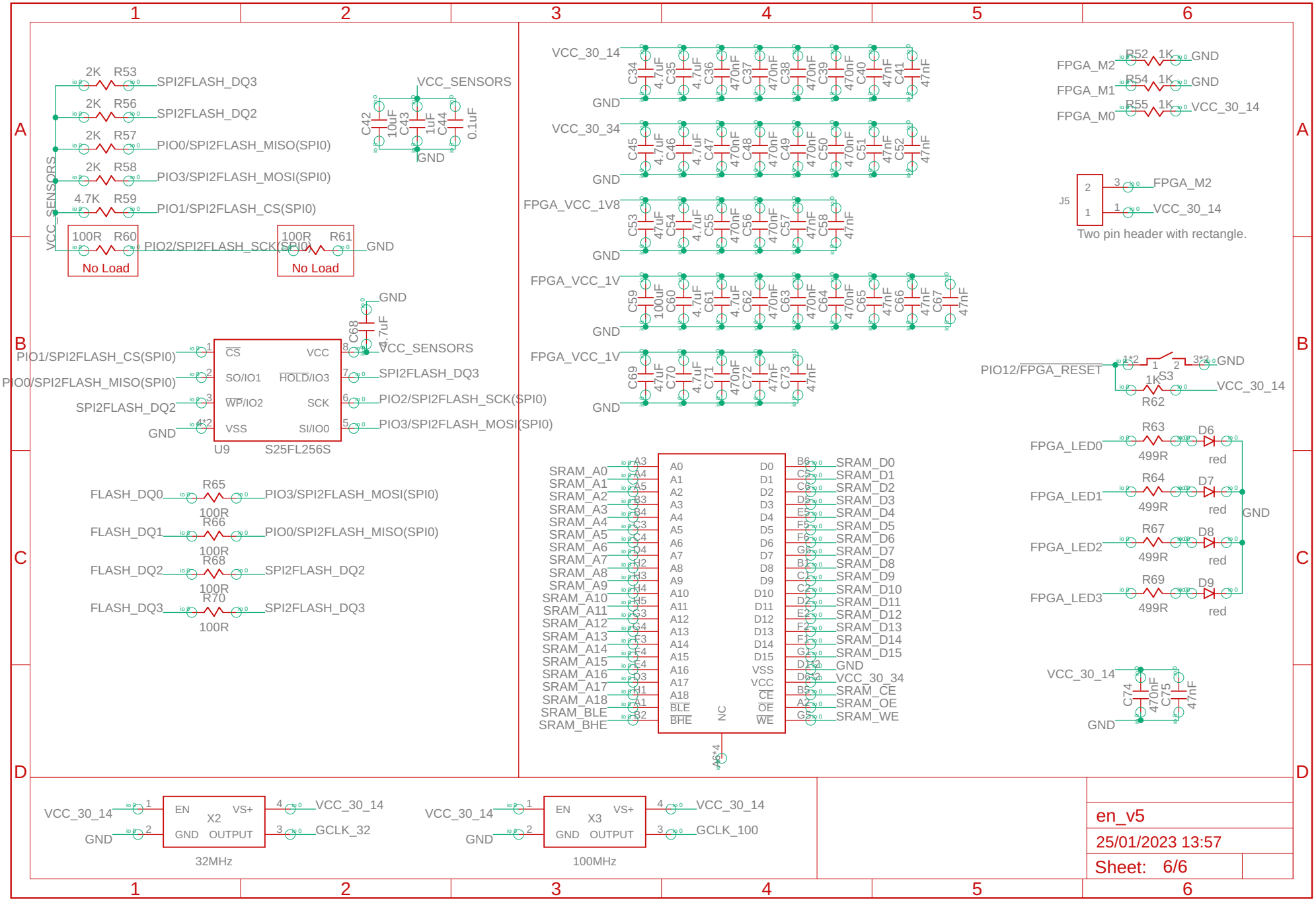
2K R53 SPI2FLASH_DQ3
2K R56 SPI2FLASH_DQ2
2K R57 PIO0/SPI2FLASH_MISO(SPI0)
2K R58 PIO3/SPI2FLASH_MOSI(SPI0)
4.7K R59 PIO1/SPI2FLASH_CS(SPI0)
VCC_SENSORS
100R R60 No Load
PIO2/SPI2FLASH_SCK(SPI0)
100R R61 No Load
GND
C42 10uF C43 1uF C44 0.1uF
VCC_SENSORS
GND
C68 4.7uF
PIO1/SPI2FLASH_CS(SPI0)
PIO0/SPI2FLASH_MISO(SPI0)
SPI2FLASH_DQ2
GND
CS VCC SO/IO1 HOLD/IO3 WP/IO2 SCK VSS SI/IO0
U9 S25FL256S
SPI2FLASH_DQ3
PIO2/SPI2FLASH_SCK(SPI0)
PIO3/SPI2FLASH_MOSI(SPI0)
FLASH_DQ0 R65 100R PIO3/SPI2FLASH_MOSI(SPI0)
FLASH_DQ1 R66 100R PIO0/SPI2FLASH_MISO(SPI0)
FLASH_DQ2 R68 100R SPI2FLASH_DQ2
FLASH_DQ3 R70 100R SPI2FLASH_DQ3
VCC_30_14
C34 4.7uF C35 4.7uF C36 470nF C37 470nF C38 470nF C39 470nF C40 47nF C41 47nF
GND
VCC_30_34
C45 4.7uF C46 4.7uF C47 470nF C48 470nF C49 470nF C50 470nF C51 47nF C52 47nF
GND
FPGA_VCC_1V8
C53 47uF C54 4.7uF C55 470nF C56 470nF C57 47nF C58 47nF
GND
FPGA_VCC_1V
C59 100uF C60 4.7uF C61 4.7uF C62 470nF C63 470nF C64 470nF C65 47nF C66 47nF C67 47nF
GND
FPGA_VCC_1V
C69 47uF C70 4.7uF C71 470nF C72 47nF C73 47nF
GND
SRAM_A0 SRAM_A1 SRAM_A2 SRAM_A3 SRAM_A4 SRAM_A5 SRAM_A6 SRAM_A7 SRAM_A8 SRAM_A9 SRAM_A10 SRAM_A11 SRAM_A12 SRAM_A13 SRAM_A14 SRAM_A15 SRAM_A16 SRAM_A17 SRAM_A18 SRAM_BLE SRAM_BHE
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 BLE BHE NC
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 VSS VCC CE OE WE
SRAM_D0 SRAM_D1 SRAM_D2 SRAM_D3 SRAM_D4 SRAM_D5 SRAM_D6 SRAM_D7 SRAM_D8 SRAM_D9 SRAM_D10 SRAM_D11 SRAM_D12 SRAM_D13 SRAM_D14 SRAM_D15 GND VCC_30_34 SRAM_CE SRAM_OE SRAM_WE
*4
FPGA_M2 R52 1K GND
FPGA_M1 R54 1K GND
FPGA_M0 R55 1K VCC_30_14
J5
FPGA_M2
VCC_30_14
Two pin header with rectangle.
PIO12/FPGA_RESET
S3
GND
R62 1K
VCC_30_14
FPGA_LED0 R63 499R D6 red
FPGA_LED1 R64 499R D7 red
FPGA_LED2 R67 499R D8 red
FPGA_LED3 R69 499R D9 red
GND
VCC_30_14
C74 470nF C75 47nF
GND
VCC_30_14 EN VS+ GND OUTPUT X2 GCLK_32
32MHz
VCC_30_14 EN VS+ GND OUTPUT X3 GCLK_100
100MHz
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