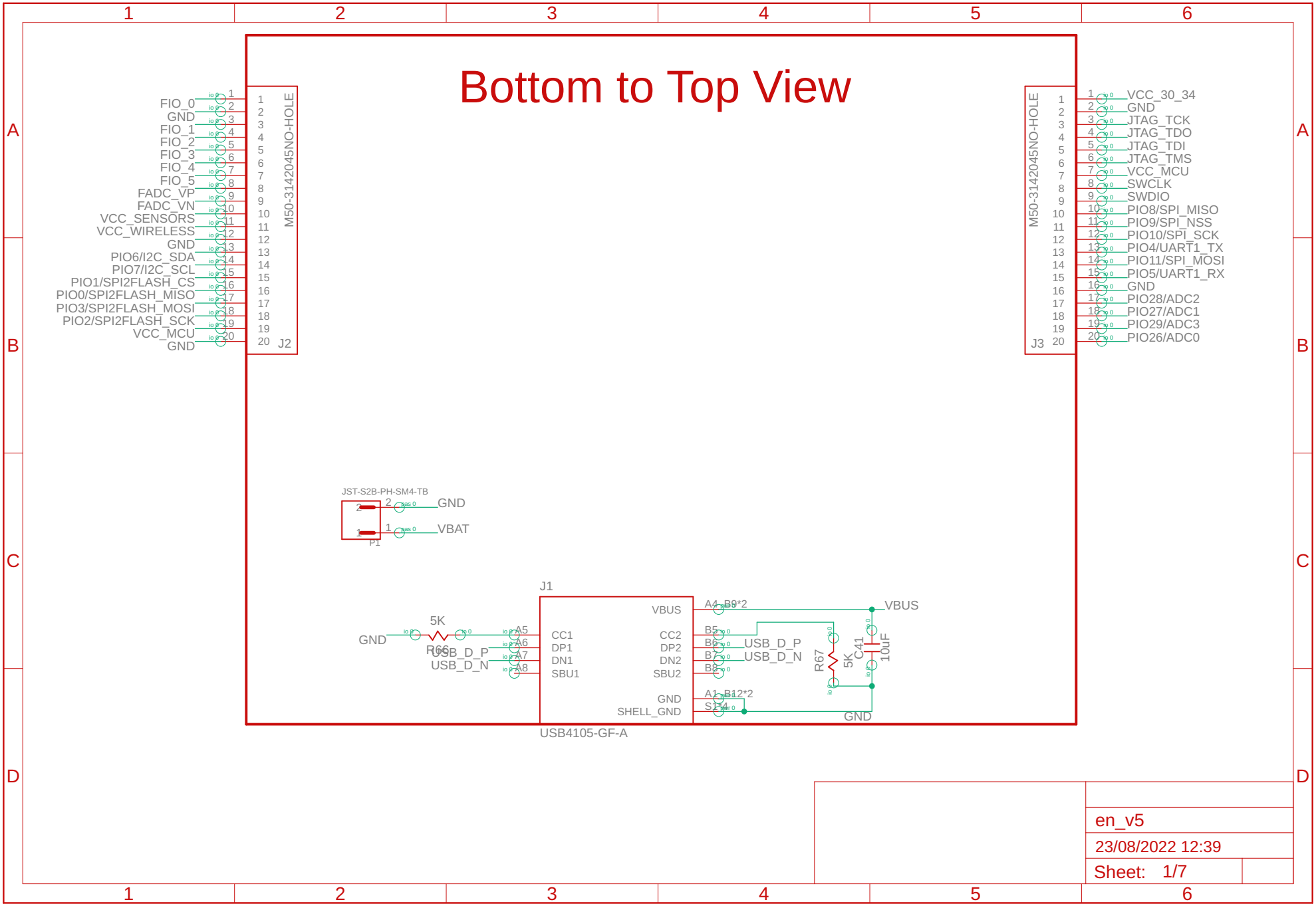
Bottom to Top View
FIO_0
GND
FIO_1
FIO_2
FIO_3
FIO_4
FIO_5
FADC_VP
FADC_VN
VCC_SENSORS
VCC_WIRELESS
GND
PIO6/I2C_SDA
PIO7/I2C_SCL
PIO1/SPI2FLASH_CS
PIO0/SPI2FLASH_MISO
PIO3/SPI2FLASH_MOSI
PIO2/SPI2FLASH_SCK
VCC_MCU
GND
M50-3142045NO-HOLE
J2
M50-3142045NO-HOLE
J3
VCC_30_34
GND
JTAG_TCK
JTAG_TDO
JTAG_TDI
JTAG_TMS
VCC_MCU
SWCLK
SWDIO
PIO8/SPI_MISO
PIO9/SPI_NSS
PIO10/SPI_SCK
PIO4/UART1_TX
PIO11/SPI_MOSI
PIO5/UART1_RX
GND
PIO28/ADC2
PIO27/ADC1
PIO29/ADC3
PIO26/ADC0
JST-S2B-PH-SM4-TB
GND
VBAT
P1
J1
VBUS
CC1
DP1
DN1
SBU1
CC2
DP2
DN2
SBU2
GND
SHELL_GND
A4_B9*2
B5
B6
B7
B8
A1_B12*2
S1-4
5K
R66
USB_D_P
USB_D_N
R67
C41
10uF
VBUS
GND
USB4105-GF-A
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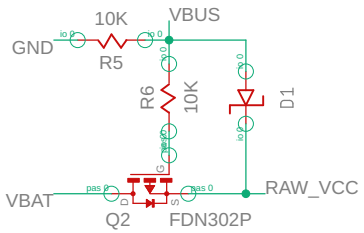
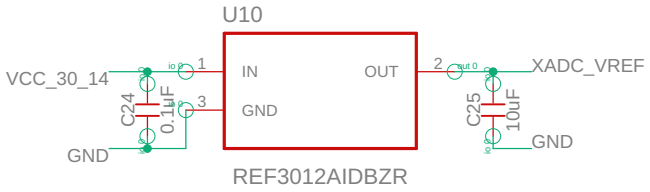
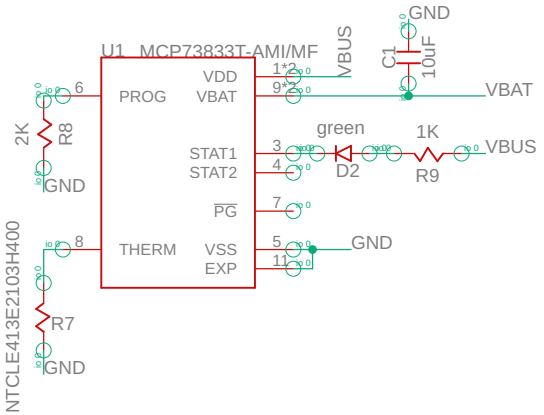
Swithing source (USB/BATT)



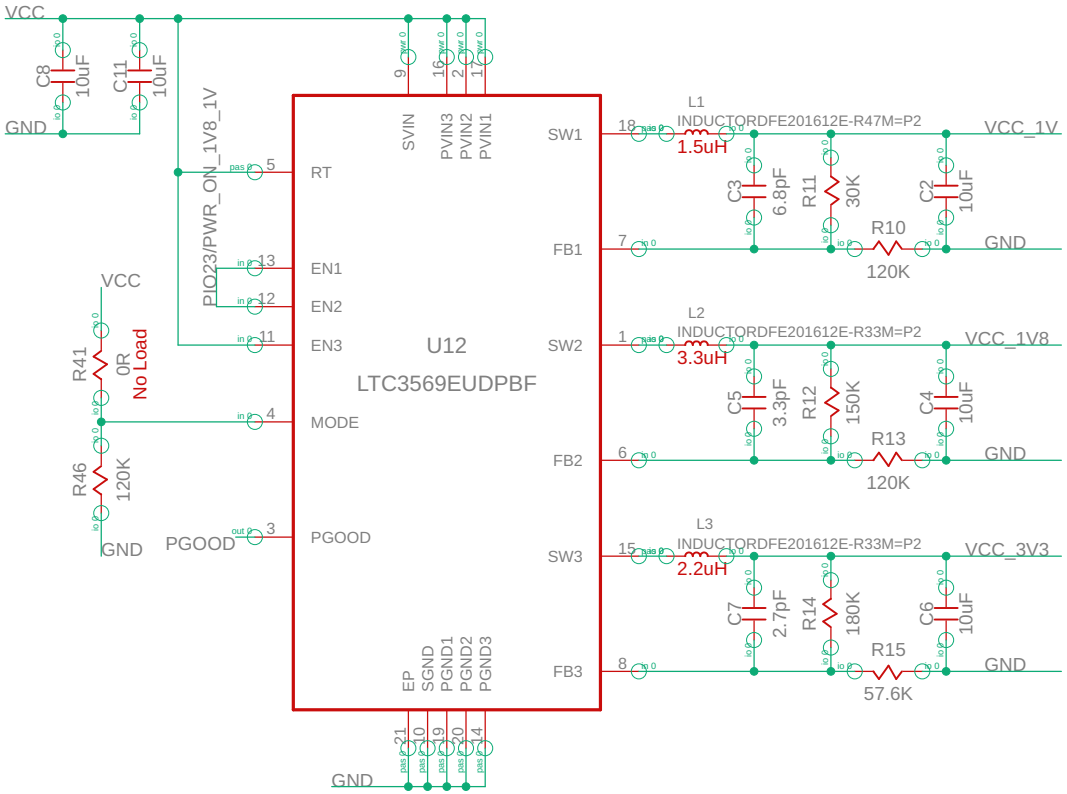
FPGA XADC Reference



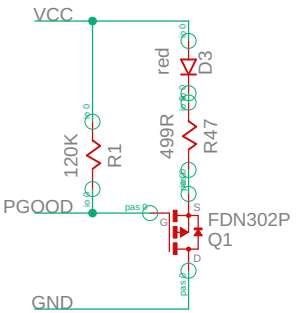
Battery Charging Management



Power Supply 3 Channels



Voltage Regulator PGOOD Indicator



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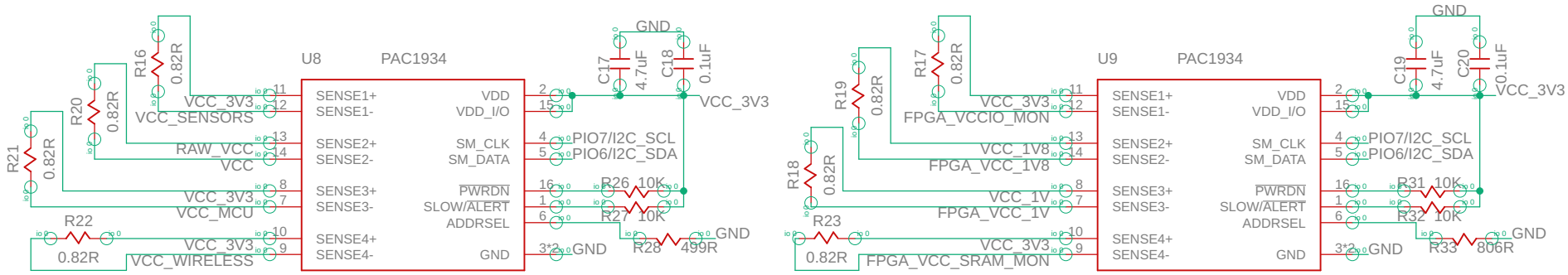
Power/Energy Meter

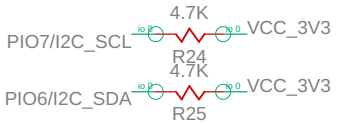


Sample resistor: UCR03EVPFLR100

The PWDOWN and alert signal are hardly pulled-up to VCC

Power Control (ON/OFF)

I2C Pullup Resistors



1. PIO23 MUST be set to HIGH before enable the 3.3V Power of the FPGA.
2. Turning PIO21 to LOW will enable the 3.3V power rail to the FPGA including the external SRAM.

To turn off the SRAM entirely, you need to desolder the 100Ohm resistor.

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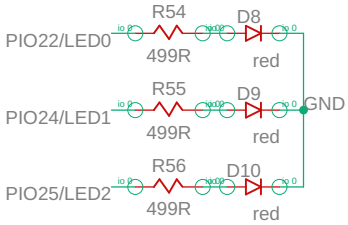
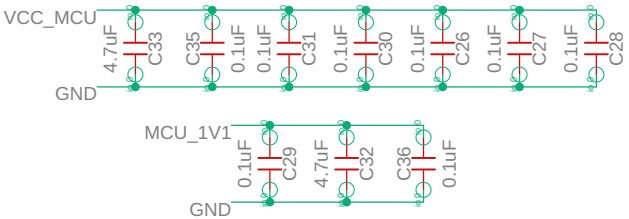
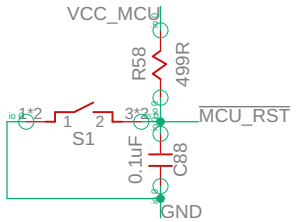
MCU LEDs



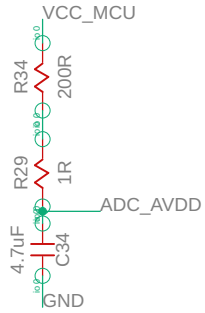
MCU Power Supply Filtering



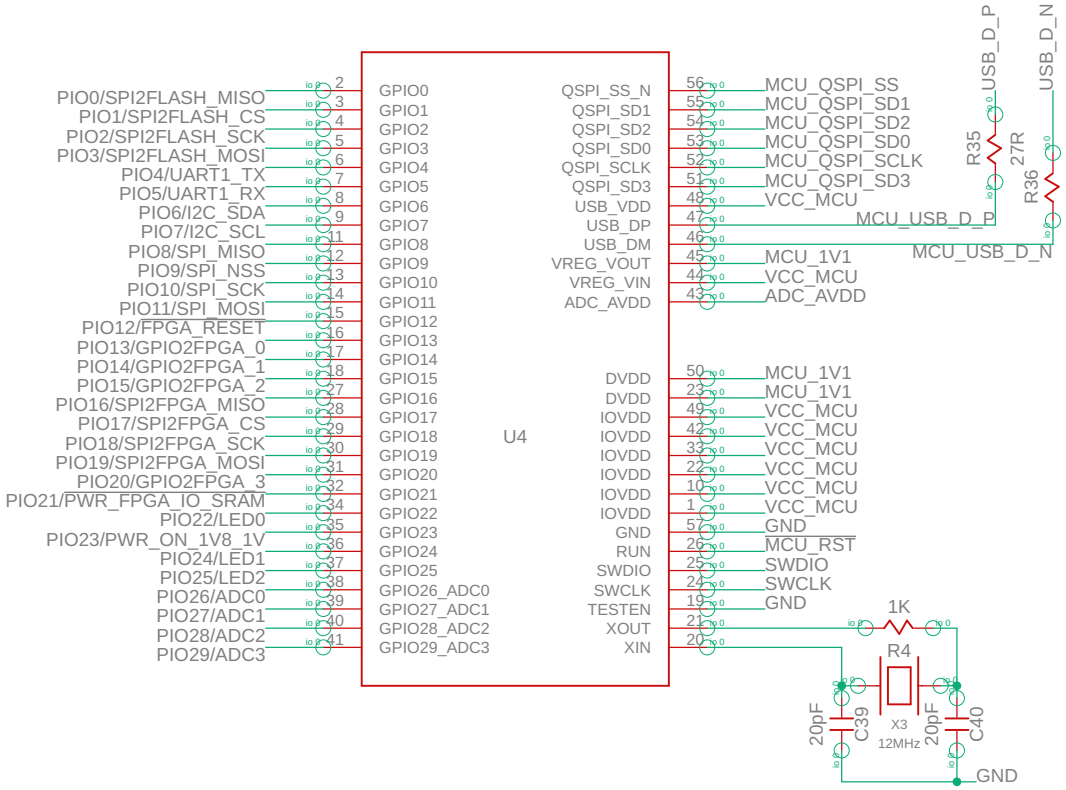
MCU Reset Circuit



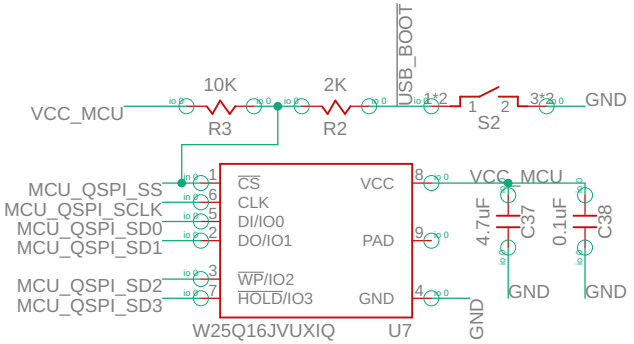
MCU ADC VDD



RP2040 MCU



MCU BOOT and Flash



If the $\overline{CS}$ pin is low during the startup of the MCU, the MCU will enter bootloader.

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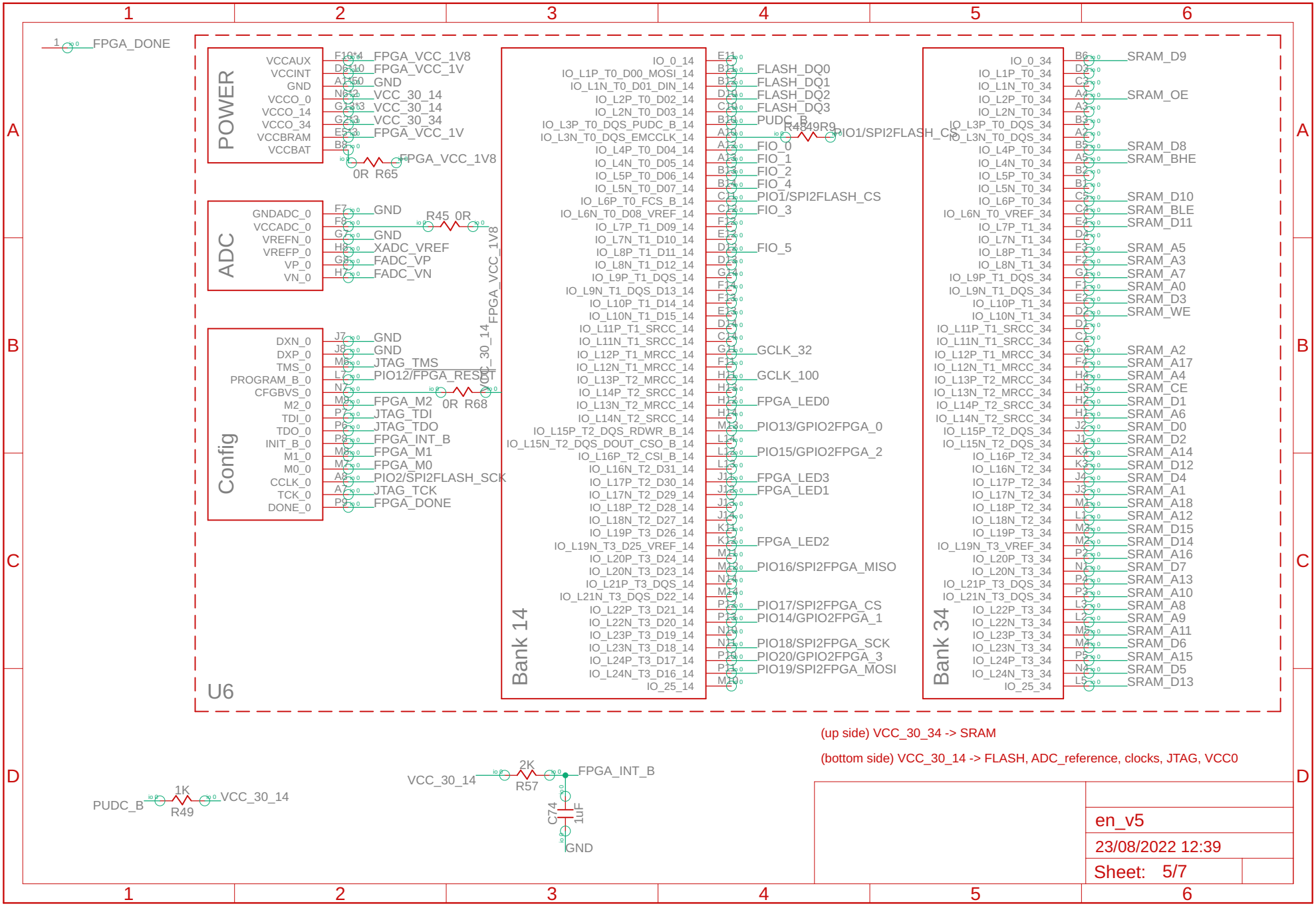
FPGA_DONE
POWER
VCCAUX
VCCINT
GND
VCCO_0
VCCO_14
VCCO_34
VCCBRAM
VCCBAT
FPGA_VCC_1V8
FPGA_VCC_1V
GND
VCC_30_14
VCC_30_14
VCC_30_34
FPGA_VCC_1V
FPGA_VCC_1V8
0R R65
ADC
GNDADC_0
VCCADC_0
VREFN_0
VREFP_0
VP_0
VN_0
GND
R45 0R
GND
XADC_VREF
FADC_VP
FADC_VN
FPGA_VCC_1V8
Config
DXN_0
DXP_0
TMS_0
PROGRAM_B_0
CFGBVS_0
M2_0
TDI_0
TDO_0
INIT_B_0
M1_0
M0_0
CCLK_0
TCK_0
DONE_0
GND
GND
JTAG_TMS
PIO12/FPGA_RESET
VCC_30_14
FPGA_M2 0R R68
JTAG_TDI
JTAG_TDO
FPGA_INT_B
FPGA_M1
FPGA_M0
PIO2/SPI2FLASH_SCK
JTAG_TCK
FPGA_DONE
U6
Bank 14
IO_0_14
IO_L1P_T0_D00_MOSI_14
IO_L1N_T0_D01_DIN_14
IO_L2P_T0_D02_14
IO_L2N_T0_D03_14
IO_L3P_T0_DQS_PUDC_B_14
IO_L3N_T0_DQS_EMCCLK_14
IO_L4P_T0_D04_14
IO_L4N_T0_D05_14
IO_L5P_T0_D06_14
IO_L5N_T0_D07_14
IO_L6P_T0_FCS_B_14
IO_L6N_T0_D08_VREF_14
IO_L7P_T1_D09_14
IO_L7N_T1_D10_14
IO_L8P_T1_D11_14
IO_L8N_T1_D12_14
IO_L9P_T1_DQS_14
IO_L9N_T1_DQS_D13_14
IO_L10P_T1_D14_14
IO_L10N_T1_D15_14
IO_L11P_T1_SRCC_14
IO_L11N_T1_SRCC_14
IO_L12P_T1_MRCC_14
IO_L12N_T1_MRCC_14
IO_L13P_T2_MRCC_14
IO_L14P_T2_SRCC_14
IO_L13N_T2_MRCC_14
IO_L14N_T2_SRCC_14
IO_L15P_T2_DQS_RDWR_B_14
IO_L15N_T2_DQS_DOUT_CSO_B_14
IO_L16P_T2_CSI_B_14
IO_L16N_T2_D31_14
IO_L17P_T2_D30_14
IO_L17N_T2_D29_14
IO_L18P_T2_D28_14
IO_L18N_T2_D27_14
IO_L19P_T3_D26_14
IO_L19N_T3_D25_VREF_14
IO_L20P_T3_D24_14
IO_L20N_T3_D23_14
IO_L21P_T3_DQS_14
IO_L21N_T3_DQS_D22_14
IO_L22P_T3_D21_14
IO_L22N_T3_D20_14
IO_L23P_T3_D19_14
IO_L23N_T3_D18_14
IO_L24P_T3_D17_14
IO_L24N_T3_D16_14
IO_25_14
FLASH_DQ0
FLASH_DQ1
FLASH_DQ2
FLASH_DQ3
PUDC_B
R4849R9
PIO1/SPI2FLASH_CS
FIO_0
FIO_1
FIO_2
FIO_4
PIO1/SPI2FLASH_CS
FIO_3
FIO_5
GCLK_32
GCLK_100
FPGA_LED0
PIO13/GPIO2FPGA_0
PIO15/GPIO2FPGA_2
FPGA_LED3
FPGA_LED1
FPGA_LED2
PIO16/SPI2FPGA_MISO
PIO17/SPI2FPGA_CS
PIO14/GPIO2FPGA_1
PIO18/SPI2FPGA_SCK
PIO20/GPIO2FPGA_3
PIO19/SPI2FPGA_MOSI
Bank 34
IO_0_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
IO_L10N_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L16P_T2_34
IO_L16N_T2_34
IO_L17P_T2_34
IO_L17N_T2_34
IO_L18P_T2_34
IO_L18N_T2_34
IO_L19P_T3_34
IO_L19N_T3_VREF_34
IO_L20P_T3_34
IO_L20N_T3_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L22P_T3_34
IO_L22N_T3_34
IO_L23P_T3_34
IO_L23N_T3_34
IO_L24P_T3_34
IO_L24N_T3_34
IO_25_34
SRAM_D9
SRAM_OE
SRAM_D8
SRAM_BHE
SRAM_D10
SRAM_BLE
SRAM_D11
SRAM_A5
SRAM_A3
SRAM_A7
SRAM_A0
SRAM_D3
SRAM_WE
SRAM_A2
SRAM_A17
SRAM_A4
SRAM_CE
SRAM_D1
SRAM_A6
SRAM_D0
SRAM_D2
SRAM_A14
SRAM_D12
SRAM_D4
SRAM_A1
SRAM_A18
SRAM_A12
SRAM_D15
SRAM_D14
SRAM_A16
SRAM_D7
SRAM_A13
SRAM_A10
SRAM_A8
SRAM_A9
SRAM_A11
SRAM_D6
SRAM_A15
SRAM_D5
SRAM_D13
PUDC_B
1K
R49
VCC_30_14
VCC_30_14
2K
R57
FPGA_INT_B
C74
1uF
GND
(up side) VCC_30_34 -> SRAM
(bottom side) VCC_30_14 -> FLASH, ADC_reference, clocks, JTAG, VCC0
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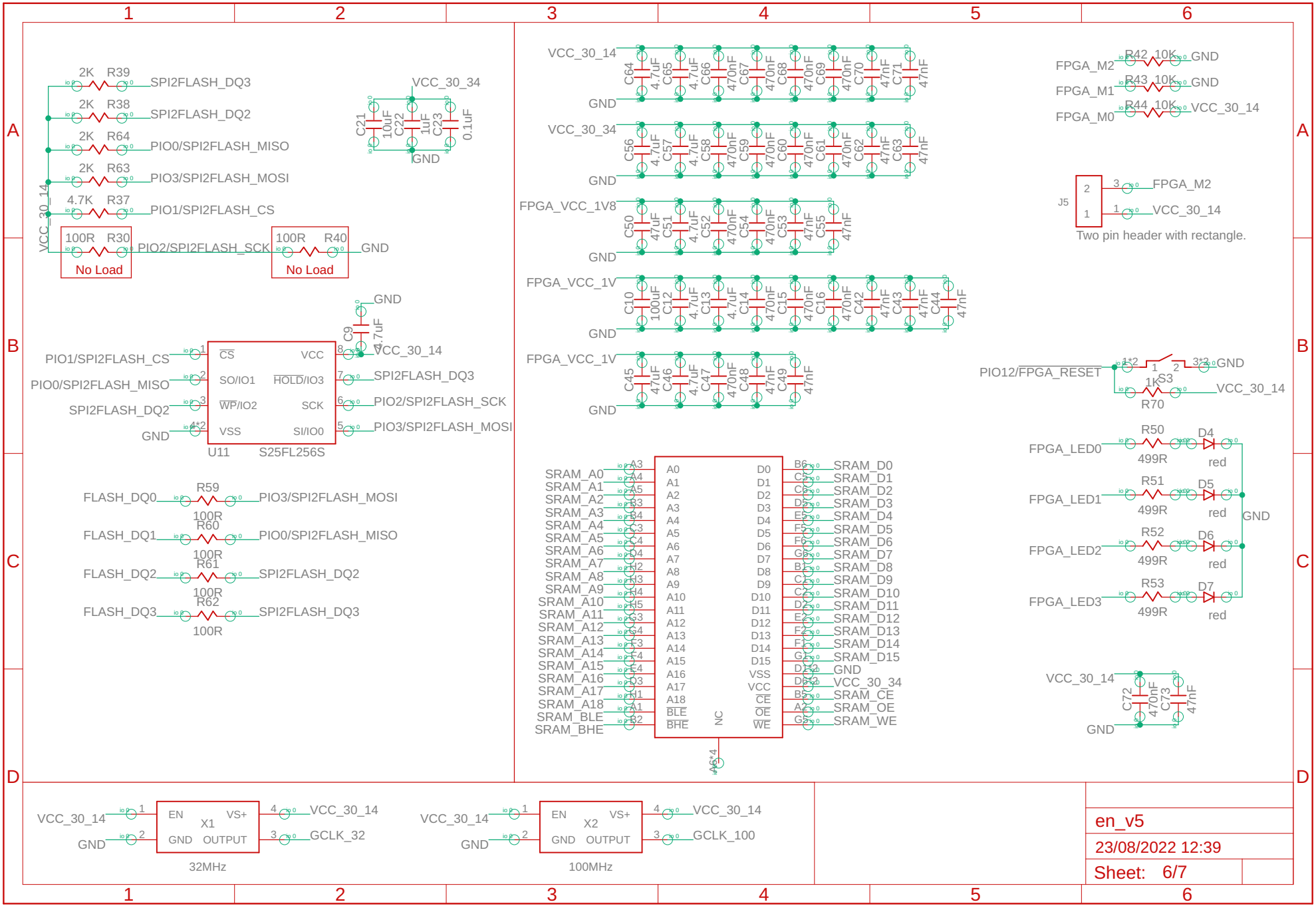
2K R39
SPI2FLASH_DQ3
2K R38
SPI2FLASH_DQ2
2K R64
PIO0/SPI2FLASH_MISO
2K R63
PIO3/SPI2FLASH_MOSI
4.7K R37
PIO1/SPI2FLASH_CS
VCC_30_14
100R R30
No Load
PIO2/SPI2FLASH_SCK
100R R40
No Load
GND
VCC_30_34
C21 10uF
C22 1uF
C23 0.1uF
GND
GND
C9 4.7uF
VCC_30_14
PIO1/SPI2FLASH_CS
PIO0/SPI2FLASH_MISO
SPI2FLASH_DQ2
GND
CS
SO/IO1
WP/IO2
VSS
VCC
HOLD/IO3
SCK
SI/IO0
SPI2FLASH_DQ3
PIO2/SPI2FLASH_SCK
PIO3/SPI2FLASH_MOSI
U11
S25FL256S
FLASH_DQ0
R59 100R
PIO3/SPI2FLASH_MOSI
FLASH_DQ1
R60 100R
PIO0/SPI2FLASH_MISO
FLASH_DQ2
R61 100R
SPI2FLASH_DQ2
FLASH_DQ3
R62 100R
SPI2FLASH_DQ3
VCC_30_14
C64 4.7uF
C65 4.7uF
C66 470nF
C67 470nF
C68 470nF
C69 470nF
C70 47nF
C71 47nF
GND
VCC_30_34
C56 4.7uF
C57 4.7uF
C58 470nF
C59 470nF
C60 470nF
C61 470nF
C62 47nF
C63 47nF
GND
FPGA_VCC_1V8
C50 47uF
C51 4.7uF
C52 470nF
C54 470nF
C53 47nF
C55 47nF
GND
FPGA_VCC_1V
C10 100uF
C12 4.7uF
C13 4.7uF
C14 470nF
C15 470nF
C16 470nF
C42 47nF
C43 47nF
C44 47nF
GND
FPGA_VCC_1V
C45 47uF
C46 4.7uF
C47 470nF
C48 47nF
C49 47nF
GND
SRAM_A0
SRAM_A1
SRAM_A2
SRAM_A3
SRAM_A4
SRAM_A5
SRAM_A6
SRAM_A7
SRAM_A8
SRAM_A9
SRAM_A10
SRAM_A11
SRAM_A12
SRAM_A13
SRAM_A14
SRAM_A15
SRAM_A16
SRAM_A17
SRAM_A18
SRAM_BLE
SRAM_BHE
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 BLE BHE
NC
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 VSS VCC CE OE WE
SRAM_D0
SRAM_D1
SRAM_D2
SRAM_D3
SRAM_D4
SRAM_D5
SRAM_D6
SRAM_D7
SRAM_D8
SRAM_D9
SRAM_D10
SRAM_D11
SRAM_D12
SRAM_D13
SRAM_D14
SRAM_D15
GND
VCC_30_34
SRAM_CE
SRAM_OE
SRAM_WE
A[5:4]
FPGA_M2
R42 10K
GND
FPGA_M1
R43 10K
GND
FPGA_M0
R44 10K
VCC_30_14
J5
FPGA_M2
VCC_30_14
Two pin header with rectangle.
PIO12/FPGA_RESET
S3
1K R70
GND
VCC_30_14
FPGA_LED0
R50 499R
D4 red
FPGA_LED1
R51 499R
D5 red
FPGA_LED2
R52 499R
D6 red
FPGA_LED3
R53 499R
D7 red
GND
VCC_30_14
C72 470nF
C73 47nF
GND
VCC_30_14
GND
EN VS+ GND OUTPUT
X1
VCC_30_14
GCLK_32
32MHz
VCC_30_14
GND
EN VS+ GND OUTPUT
X2
VCC_30_14
GCLK_100
100MHz
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Error 1: The silk print of MCU Rest and boot are switched.
Error 2: the silk print of the date is 2021, should be change to 2022.
Error 3: resistors to M[2:0] should be change to 1K

To optimize: add which I2C that PAC 1934 are connected, answer is I2C1
To optimize: R48 should be removed, then emcclk connect to 100MHz, this versions supports internal clk for configuration with up to 50MHz, QSPI.

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