Pads (104) (103	102	101) (1	00 099	098	097	096 (0	95) (094	4) (093)	092	<u>091</u> ) (0	90 08	9 088	087	086	085 08	4 083	082	081)	080 079	
001																				078
002 Pins 1 d00-	88 rst-	1 1	36 1.17 85 705.1	1 1 1	83 +c		<b>81 80</b> 705.0	1 1	78 708.17	709.ao 7	76 09.ai +	5 74 c +a	713.ai	72 713.ao	1 1	70 7.ao 69 717.		67 a01	-a02 66	077
003 2 d01-	700	1 17	702	702	704	17 5 3 1 70 E	706	707	1 17 700	ao ai 17	710	711	712	ai ao 17	714	17 71 E	716	17 ao ai	-a03 65	076
004 3 d02	/ UU	serdes	/UZ	7 U S	704	SPI	706	7 <b>0</b> 7	async	analog	710	<b>7 L</b> L	L 12	analog	/ 14 L	<b>7 1</b> 5	r / TO	analog	+i 64	075
(005) \ (4 +i)		D		D		D										D		D	617.ao <b>63</b>	074
006	600	601	602	603	604	605	606	607	608	609	610	611	612	<b>61</b> 3	614	615	616	<b>617</b> analog	+c 62	073
007 6 600.17	17	R	L	R	L	R		R		R		R	L	R	L	R	L	Ranarog	617.ai <b>61</b>	072
009 7 500.17	—17 <b>FOO</b>	501	502	EU3	504	505	506	507	508	500	510	5 1 1	512	512	51/	U 515	516	<b>517</b>		071
010 8 d03	1	R	50Z	R	304	303	500	307	308	R	210	3 T T	7	B D L D	214	R	2 TO	R R	517.17 <b>60</b> 417.17 <b>59</b>	
011 9 d04	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	-a04 58	
012—10 d05	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417		
013—11 d06-		R	L	R				R		R		R		R		R	_	R	-a06 56	066
014 12 d07	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	<b>317</b>	-a07 55	065
015 13 d08		R	L	R		2		R		R	310	R	L 312	R	L	R	L	R	-a08 54	064
<b>016 14</b> 300.17		D	D.	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	-a09 53	063
<b>017 15</b> 300.01	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	<b>217</b>	317.17 <b>52</b>	062
018 16 d09	—17																	Г	217.17 <b>51</b>	061
019 17 +c	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	117 117.ao <b>50</b>	060
18 200.17	L	R	L	R	L		L I	R		R		R	L	R	L	R	L	R analog	+c 49	059
021) 19 +i		D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	117.ai <b>48</b>	058
<b>20</b> 100.17	000	001 serdes	002	003 <sub>R</sub>	004	005	006	007 data	008 control	009 address	010	011	012	013	014	<b>015</b>	016	<b>017</b>	+i 47	057
023 024 21 d10								17	9 7	17									-a10 46	056
025 22 d11-			14					d00d17		a00a17							4 -12		-a11 45	054
026	d12 23	d13 d 2	14 25 001.0 26	1 1	+1 28	+C 29	115 30 d1 31		33		08.03 35 35	.01 6 37	a16 38	a15 39	40	+c 41 42	4 a13 43	a12 44		053
027 028	029	030 0	31) 037	2 033	034	035 0	36 037	7 038	039	040 0	41) (04)	2) 043	044	045 (0	046 04	7 048	049	050	051 052	
											$\sim$						049	050	051 052	
IO	17	16	15	14	13	12	11	.  10	0  0	9   0	8 10	)7			04	03	02	01	00	
IO Read Write	PI	N   Rr		: _	13 _   Dv			: .	Jr_ İ	9   <mark>0</mark> Uw   pin		)7  ( pin		05   PIN	04 state	03 PIN		01   PIN		
Read Write	PII PII SR	N   Rr N stat 	e	I Dr	_   Dv     VCO	v   L   D 	B	.w   U	Jr_ İ	Uw   pin   		i pin	06       DAC o	05   PIN   PIN s	tate level	03 PIN PIN	<mark>02</mark>   state	01   PIN	00	
Read Write PIN sta WD	PII   PII   SR   01:	N   Rr N stat   =WEAK =NORMA	PULLDO	/   Dr   	-   Dv VCO )=trist L=inve	v   L   D   tate		.w   U	Jr_ İ	Uw İ		i pin	DAC o -Pi -Wa	05   PIN   PIN s utput n Stat ke Dir	tate level	03 PIN PIN (155	<mark>02</mark>   state	01   PIN	00	
Read Write PIN sta	PII   PII   SR   01:   0:   1:   0:	N   Rr N stat   = <b>WEAK</b>	PULLDO	/   Dr   	-   Dv     VCO  =trist	v   L   D tate rted tate	B	w   U D               	Jr_       	Uw   pin     11=Vd	<b>d</b> (1)	pin   9-bit	DAC o -Pi -Wa -Da -Se	05   PIN   PIN s utput n Stat ke Dir ta Bus rializ	tate level e ection	03 PIN PIN (155	<mark>02</mark>   state xor)	01   PIN   PIN	00	
PIN sta WD DB SR VCO	PII   PII   SR   O:   1:   O:   10:	N   Rr N stat   =WEAK =NORMA =OUTPU =RECEI =OFF	PULLDO L T VE	/   Dr   	VCO )=trist L=inver )=trist L=send	v   L   D tate rted tate	B W	w   U D               	Jr_       	Uw   pin   11=Vd  11=Vs Port	d(1) s cali	pin   9-bit brate	DAC o -Pi -Wa -Da -Se -Vo	05   PIN   PIN s utput n Stat ke Dir ta Bus rializ ltage	tate level ection direction Contro	03 PIN PIN (155	<mark>02</mark>   state xor)	01   PIN   PIN	00	
PIN sta WD DB SR VCO Port A -d-u -d	PII   PII   SR   SR   0:   0:   10:   10:   10:   105   115	N   Rr N stat   =WEAK =NORMA =OUTPU =RECEI =OFF Desc Down Down	PULLDO L T VE	)   Dr 	VCO )=trist L=inver )=trist L=send	v   L   D tate rted tate	B W	w   U D               	Jr_       	Uw   pin   11=Vd  11=Vs Port rd-u rd	d(1) s cali Addres 18 19	pin   9-bit ess D 5 R	DAC o -Pi -Wa -Da -Se -Vo escrip	05   PIN   PIN s utput n Stat ke Dir ta Bus rializ ltage otion Down, Down	tate level ection direction Contro	03 PIN PIN (155 n ction serial	<mark>02</mark>   state xor)	01   PIN   PIN	00	
PIN sta WD DB SR VCO Port A -d-u -d-u -d -dlu -d1-	PII   PII   SR   SR   0:   10:   10:   10:   10:   125   135	N   Rr N stat   =WEAK =NORMA =OUTPU =RECEI =OFF Down Down Down Down	PULLDO L T VE riptic , Up , Left	/   Dr   	VCO )=trist L=inver )=trist L=send )=input	v   L   D tate rted tate	B W	w   U D               	Jr_       	Uw   pin   11=Vd  11=Vd  Port rd-u rd rdlu rdl-	d(1) s cali Addre 18 19 1a 1b	pin   9-bit ess D 5 R 5 R 5 R	DAC o -Pi -Wa -Da -Se -Vo escriptinght, light, light,	05   PIN   PIN s utput n Stat ke Dir ta Bus rializ ltage tion Down, Down, Down, Down,	tate level ection direction cer/Des Contro	03 PIN PIN (155 n ction serial	<mark>02</mark>   state xor)	01   PIN   PIN	00	
PIN sta WD DB SR VCO Port A -d-u -d-u -d1- data u	PII   PII   SR   SR   O:   1:   O:   10:   Address   105   115   125   135   141   145	N   Rr N stat   =WEAK =NORMA =OUTPU =RECEI =OFF Down Down Down Down Up, Up	PULLDO L T VE riptic , Up , Left no har	own och	VCO )=trist L=inver )=trist L=send )=input	v   L   D   tate rted tate	B W	w   U D               	Jr_       	Uw   pin   11=Vd  11=Vd  Port rd-u rd rdlu rdl- ru r	d(1)  s cali Addre 18 19 1a 1b 1c 1d	pin   9-bit 9-bit 5 R 5 R 5 R 5 R	DAC o -Pi -Wa -Da -Se -Vo escriptinght, light, light, light,	05   PIN   PIN s utput n Stat ke Dir ta Bus rializ ltage tion Down, Down, Down, Down, Up	tate level ection direction direction cer/Des Contro	03 PIN PIN (155 n ction serial	<mark>02</mark>   state xor)	01   PIN   PIN	00	
PIN sta WD DB SR VCO Port A -d-u -d-u -d1- data	PII   PII   SR   SR   O:   10:   10:   Address   105   115   125   135   141   145   15d   165	N   Rr N stat   =WEAK =NORMA =OUTPU =RECEI DOWN DOWN DOWN DOWN Up, Up 18-b Left	PULLDO L T VE  riptic , Up  Left no har	own och	VCO )=trist L=inver )=trist L=send )=input	v   L   D   tate rted tate	B W	w   U D               	Jr_       	Uw   pin   11=Vd  11=Vd  11=vd  Port rd-u rd rdlu rdl- ru r r-lu r-l-	d(1)  s cali Addred 18 19 1a 1b 1c 1d 1e 1f	pin   9-bit 9-bit 5 R 5 R 5 R 5 R 5 R	DAC o -Pi -Wa -Da -Se -Vo lescriptinght, light, 5   PIN   PIN s utput n Stat ke Dir ta Bus rializ ltage tion Down, Down, Down, Up Left, Left	tate level ection direction cer/Des Contro Up Left, Left	03 PIN PIN (155 n ction serial olled	02   state xor)	01   PIN   PIN	OO   state		
PIN sta WD DB SR VCO Port A -d-u -d-u -dlu -dl- data u io lu l- address	PII   PII   SR   SR   10:   0:   10:   10:   10:   145   135   141   145   15d   165   175   18-bi	N   Rr N stat =WEAK =NORMA =OUTPU =RECEI =OFF Down Down Down Up, Up 18-b Left Left	PULLDO L T VE  riptic , Up  Left no har it I/C , Up	WN 000000000000000000000000000000000000	VCO )=trist L=inver )=trist L=send )=input	v   L   D   tate rted tate	B W	w   U D               	Jr_       	Uw   pin   11=Vd  11=Vd  11=vd  Port rd-u rd rdlu rdl- ru r r-lu r-l-	d(1)  s cali Addred 18 19 1a 1b 1c 1d 1e 1f ALWA	pin   9-bit 9-bit 5 R 5 R 5 R 5 R 5 R 5 R 5 R 5 R	DAC o  -Pi -Wa -Da -Se -Vo escriptinght, light, 5   PIN   PIN s utput n Stat ke Dir ta Bus rializ ltage tion Down, Down, Down, Up Left, Left port	tate level ection direction direction cer/Des Contro Up Left, Left Up names, ster,	03 PIN PIN (155 n ction serial olled	02   state   xor)	01   PIN   PIN	OO   state		
PIN sta WD DB SR VCO Port A -d-u -d-u -dl- data u io lu l- address data a	PII   PII   SR   SR   te 01:   0:   10:   10:   10:   145   135   141   145   15d   165   175   18-bi:   18-bi:   18-bi:	N   Rr N stat =WEAK =NORMA =OUTPU =RECEI DOWN DOWN DOWN Up, Up 18-b Left t exte	PULLDO L T VE  riptic , Up  it I/C ino har  it I/C rnal a rnal a ral, a	own och och och och och och och och och och	VCO )=trist L=inver )=trist L=send )=input	tate tate tate	10=Vss	w   UD   US (0)	Jr_                 	Uw   pin   11=Vd  11=Vd  11=Vd  Port rd-u rd rdlu rdl- ru r-l- Note: p r t, s	d(1)  s cali Addred 18 19 1a 1b 1c 1d 1e 1f ALWA 10 18 18	pin   9-bit 9-bit ess D 5 R 5 R 5 R 5 R 5 R 5 R 5 R 5 R 5 R 5 R	DAC o  -Pi -Wa -Da -Se -Vo escriptinght, light, light, light, light, light, light light, light l	O5   PIN   PIN s utput n Stat ke Dir ta Bus rializ ltage tion Down, Down, Down, Up Left, Left port regis a stac	tate level e ection direction cer/Des Contro Up Left, Left Up names, ster, tack ck	03 PIN PIN (155  1 ction serial olled  Up  addre 7-bit	O2  state  xor)	01   PIN   PIN	OO   state	
PIN sta WD DB SR VCO Port A -d-u -d-u -dl- data u io lu l- address data	PII   PII   SR   SR   SR   SR   O:   O:   O:   O:   O:   O:   O:   O:	N   Rr N stat   = WEAK = NORMA = OUTPU = RECEI DOWN DOWN DOWN Up, Up 18-b Left t exte t exte t gene t addr	PULLDO L T VE ription , Left no har it I/O , Up rnal a rnal a ral, a rss (w ADD	WN 00  On  Iddress Iddress Iddress Interite	VCO  Detrist  L=inver  L=send  Detrist  Solve  Solv	tate tate tate	10=Vss	w   UD   US (0)	Jr_                 	Uw   pin   11=Vd  11=Vd  11=Vd  11=vd  Port rd-u rd rdlu rdl- ru r-lu r-l- Note: p r t, s io Opcod	d(1)  s cali  Addr  18  19  1a  1b  1c  1d  1e  1f  ALWA  10  18  18  18  18  18	pin   9-bit   ss D R S R S R S R S R S R S R S R S R S R	DAC o  -Pi -Wa -Da -Se -Vo escriptinght, light, light, light, light, light, light, light light, light	O5   PIN   PIN s utput n Stat ke Dir ta Bus rializ ltage tion Down, Down, Down, Up Left, Left port in regis a stat atrol	tate level e ection direct cer/Des Contro  Up Left, Left  Up names, ster, tack ck and St	O3 PIN PIN (155  ction serial olled  Up  addre 7-bit	O2  state  xor)	01   PIN   PIN	OO   state	
PIN sta WD DB SR VCO Port A -d-u -d-u -d1- data u io lu l- address data a b Opcode	PII   PII   SR   SR   OI   OI   OI   OI   OI   OI   OI   O	N   Rr N stat = WEAK = NORMA = OUTPU = RECEI = OFF Down Down Down Up, Up 18-b Left t exte t exte t gene t addr Notes return	PULLDO L T VE ription , Left no har it I/O , Up rnal a rnal a ral, a ers (w ADD	WN OCONTINUE Address Arite Control RESS Control RES Control RESS Control RESS Control RESS Control RESS Control RES Control RESS Control RESS Control RESS Control RESS Control RES Control RESS Control RESS Control RESS Control RESS Control RES Control RESS Control RESS Control RESS Control RESS Control RES Control RESS Control RESS Control RESS Control RESS Control RES Control RESS Control RESS Control RESS Control RESS Control RES Control RESS Control RESS Control RESS Control RESS Control RES Control RESS Control RESS Control RESS Control RESS Control RES	VCO )=trist l=inver )=trist l=send )=input  s bus s, 7-b only) pcodes	tate tate tate tate tate it aut	10=Vss	w   UD   US (0)	Jr_                 	Uw   pin   11=Vd   11=	d(1)  s cali Addr 18 19 1a 1b 1c 1d 1e 1f ALWA 10 18 18 18 18 18	pin   9-bit   5 R R S R S R S R S R S R S R S R S R S	DAC o  -Pi -Wa -Da -Se -Vo escripting the sight, si	O5   PIN   PIN s utput n Stat ke Dir ta Bus rializ ltage tion Down, Down, Down, Up Left, Left port   regis a stat atrol a	tate level ection direction direction cer/Des Contro  Up Left, Left  Up names, ster, tack ck and Ster codes	O3 PIN PIN (155  ction serial olled  Up  addre 7-bit	O2  state  xor)	01   PIN   PIN	OO   state	
PIN sta WD DB SR VCO Port A -d-u -d-u -dlu -dl- data u io lu l- address data a b Opcode ; ex name ; name	PII   PII   SR   SR   O   1   O   1   O   1   O   1   O   1   O   O	N   Rr N stat = WEAK = NORMA = OUTPU = RECEI DOWN DOWN DOWN DOWN Up, Up, 18-b Left t exte t exte t gene t addr Notes return execut jump to	PULLDO L T VE riptio , Left no har it I/O , Up  rnal a ral, a ers (w ADD e via o a re o a re o a re	own occurrence of the control of the	VCO )=trist l=inver )=trist l=send )=input  s bus s, 7-b only) pcodes  p p are l, name l, name	tate rted tate tatus  it aut	10=Vss	w   UD   US (0)	Jr_                 	Uw   pin   11=Vd   11=	d(1)  s cali Addr 18 19 1a 1b 1c 1d 1e 1f ALWA  10 18 18 18 18 18 18 18 18 18 18 18 18 18	pin   9-bit   5 R R R R R R R R R R R R R R R R R R	DAC o  -Pi -Wa -Da -Se -Vo escripting to rest to rescripting to rescription to rescripting to rescription to re	O5   PIN   PIN s utput n Stat ke Dir ta Bus rializ ltage tion Down, Down, Down, Up Left, Left port regis urn s a stat atrol ALU of	tate level ection direction direction direction Up Left, Left Up names, ster, tack ck and Ster codes igned)	O3 PIN PIN (155  ction serial olled  Up  addre 7-bit	O2  state  xor)	01   PIN   PIN	OO   state	
PIN sta WD DB SR VCO Port -d-u -ddlu -dl- datau iolul- address data a b Opcode ; ex name name unext next	PII   PII   SR   SR   O   O   O   O   O   O   O   O   O	N   Rr N stat = WEAK = NORMA = OUTPU = RECEI = OFF Down Down Down Up, Up 18-b Left t extent t extent t extent t extent t addr Notes return execut jump resident	PULLDO L T VE  riptic , Up  , Left no har  it I/O , Up  rnal a ral, a ral, a ers (w  ADD  e via o a re o a re o dec  ≠0 dec  ≠0 dec	WN OCONTRIBUTE OF TEMPORE OF TEMP	VCO )=trist l=inver )=trist l=send )=input  s bus s, 7-b only) pcodes  p p ar l, name l, name l, name l, name	tate rted tate tatus  it aut	10=Vss	w   UD   US (0)	Jr_                 	Uw   pin   11=Vd   11=	d(1)  s cali Addr 18 19 1a 1b 1c 1d 1e 1f ALWA 10 18 18 18 18 18 18 18 18 18 18 18 18 18	pin   9-bit   5   8   5   5   8   5   5   5   5   5	DAC o  -Pi -Wa -Da -Se -Vo escripting to rest	O5   PIN   PIN s utput n Stat ke Dir ta Bus rializ ltage tion Down, Down, Down, Up Left, Left port regis urn s a stat trol ALU or	tate level ection direction direction cer/Des Contro  Up Left, Left  Up names, ster, tack ck and Ster codes  igned) cor)	O3 PIN PIN (155  ction serial olled  Up  addre 7-bit	O2  state  xor)	01   PIN   PIN	OO   state	Muench
PIN sta WD DB SR VCO Port -d-u -ddlu -dl- datau iolul- address data a b Opcode s ex name unext next if -if	PII   PII   SR   SR   SR   SR   SR   SR   SR	N   Rr N stat = WEAK = NORMA = OUTPU = RECEI = OFF Down Down Up 18-b Left t extent t extent t extent t addr Notes return extent jump to jump to	PULLDO L T VE  riptic , Left no har it I/C ral, a ral, a ral, a ral, a ral, a ral, a ral ess (w ADD  e via o a re o a re o dec =0 17=0	WN OCON OCON OCON OCON OCON OCON OCON OC	VCO )=trist  =inver  =send  =input	tate rted tate tate at a tus	B N  10=Vss  01=Vdd	w   UD   US (0)	Jr_                 	Uw   pin   11=Vd   11=	d(1)  s cali Addr 18 19 1a 1b 1c 1d 1e 1f ALWA  10 18 18 18 18 18 18 18 18 11 12 13 14 15 16 17	pin   9-bit   5 R R R R R R R R R R R R R R R R R R	DAC o  -Pi -Wa -Da -Se -Vo escripting to rest to rescripting to rescription to rescripting to rescription to re	O5   PIN   PIN s utput n Stat ke Dir ta Bus rializ ltage tion Down, Down, Down, Up Left, Left port regis urn s a stat trol ALU or	tate level ection direction direction cer/Des Contro  Up Left, Left  Up names, ster, tack ck and Ster codes  igned) cor)	O3 PIN PIN (155  ction serial olled  Up  addre 7-bit	O2  state  xor)	01   PIN   PIN	OO   state	Bill Muench
Read Write  PIN sta WD DB SR VCO Port -d-u -d-u -dl- datau iolul- address data a b Opcode  i ex name name unext next if -if @p @+	PII   PII   SR   SR   Contact   SR   Contact   SR   Contact   SR   Contact   SR   Contact   SR   SR   SR   SR   SR   SR   SR   S	N   Rr N   Stat   WEAK   NORMA   OUTPU   RECET   Down   Down   Up   18-btt   t extent 	PULLDO L T VE  riptic , Left no har it I/C , Up  rnal a ral, a ral, a ral a re o a re	WN OCON OCON OCON OCON OCON OCON OCON OC	VCO )=trist l=inver )=trist l=send )=input  s bus s 7-b only) pcodes p p ar l, name l,	tate tate tate tate tate tate tate tate	B N  10=Vss  01=Vdd	w   UD   US (0)	Jr_                 	Uw   pin   11=Vd   11=	d(1)  s cali  Addr  18  19  1a  1b  1c  1d  1e  1f  ALWA  10  18  18  18  18  19  11  12  13  14  15  16  17  18  19	brate ess D 5 5 7 5 7 7 8 7 8 7 8 8 7 8 8 8 7 8 8 8 8	DAC o  -Pi -Wa -Da -Se -Vo escripting to rest	O5   PIN   PIN s utput n Stat ke Dir ta Bus rializ ltage tion Down, Down, Down, Up Left, Left port regis urn s a stat trol ALU or	tate level ection direction direction cer/Des Contro  Up Left, Left  Up names, ster, tack ck and Ster codes  igned) cor)	O3 PIN PIN (155  ction serial olled  Up  addre 7-bit	O2  state  xor)	01   PIN   PIN	OO   state	ter by Bill Muench
PIN stawD DB SR VCO Port -d-u -ddlu -dl- datau iol- address data a b Opcode  ; ex name name unext next if -if @p @+ @b @	PII   PII   SR   SR   SR   SR   SR   SR   SR	N   Rr N stat = WEAK = NORMA = OFF Down Down Down Down Up 18-b Left t extent t extent t extent t extent t addr Notesreut jump r jump t jump t jump t	PULLDO L T VE riptio , Left no har it I/O rnal a rnal a ral, a ral, a ral ess (w ADD  e via o a re o dec for a re o a	WN OCON OCON OCON OCON OCON OCON OCON OC	VCO )=trist l=inver )=trist l=send )=input  s bus s, 7-b only) pcodes p p ar l, name l, name i r i r i auto- i auto- i auto-	tate tate tate tate tate tate tate tate	B N  10=Vss  01=Vdd	w   UD   US (0)	Jr_                 	Uw   pin   11=Vd   11=	d(1)  s cali Addr 18 19 1a 1b 1c 1d 1e 1f ALWA 10 18 18 18 18 18 18 19 11 12 13 14 15 16 17 18 19 1a 1b	pin   9-bit   9-bit   5	DAC of Pianal Pi	O5   PIN   PIN s utput n Stat ke Dir ta Bus rializ ltage tion Down, Down, Down, Up Left port regis urn se a stat trol ALU or fffff or (x)	tate level ection direction direction cer/Des Contro  Up Left, Left  Up names, ster, tack ck and Ster codes  igned) cor)  cor)	O3 PIN PIN (155  ation serial olled  Up  addre 7-bit	O2  state  xor)	01   PIN   PIN	OO   state	Poster by Bill Muench
PIN sta WD DB SR VCO Port A -d-u -d-u -dlu -dl -datau iolul -data a b Opcode  iname unext next if -if	PII   PII   SR   SR   SR   SR   SR   SR   SR	Rr   Stat   WEAK   NORMA   OUTPU   REF   OFF   Down   Down   Up   State   t extent   t	PULLDO L T VE riptic , Left no har it I/C rnal a rnal a ral, a ral, a ral ess (w ADD  e via e a re o A dec for a re o A de for a re o A de for a re o A de for a re o A de for a re o A de for a re o A de for a re o A de for a re o A de for a re o A de for a re o A de for a re o A de for a re o A de for a re o A de for a re o A de for a re o A de for a re o A de for a re o A de for a re o A de	WN OCON OCON OCON OCON OCON OCON OCON OC	VCO )=trist=	tate tate tate tate tate tate tate tate	B N  10=Vss  01=Vdd  o-incr  ment ment	w   UD   US (0)	Jr_                 	Uw   pin   11=Vd   11=	d(1)  s cali Addr 18 19 1a 1b 1c 1d 1e 1f ALWA 10 18 18 18 18 18 19 11 12 13 14 15 16 17 18 19 1a 1b 1c 1d 1c 1d 1d 1d 1d 1d 1d 1d 1d 1d 1d 1d 1d 1d	brate 9-bit  brate ess D 5 8 5 7 7 8 7 8 7 8 8 7 8 8 7 8 8 8 8 8	DAC of Pine - War - Da - Volescrip Right, Ri	O5   PIN   PIN s utput n Stat ke Dir tage tion Down, Down, Down, Up Left, teft port n regis a stat atrol atrol atrol arregis	tate level e ection direct cer/Des Contro  Up Left, Left  Up names, ster, tack ck and Ster codes  igned) cor)  cor)	O3 PIN PIN (155  ation serial olled  Up  addre 7-bit	O2  state  xor)	01   PIN   PIN	OO   state	Poster by Bill Muench
Read Write PIN sta WD DB SR VCO  Port A-d-u -d-u -dlu -dl-datau iolul- address data a b Opcode  igname  unext next if -if  @p @+ @b @ !p	PII   PII   SR   SR   SR   SR   SR   SR   SR	Rr   Stat   WEAK   NORMA   OUTPU   RECEI   OUTPU   O	PULLDO L T VE  riptic , Left no har it Up  rnal a ral, a ral, a ral ess (w ADD  e via e a re for a	WN OCON OCON OCON OCON OCON OCON OCON OC	VCO )=trist=	tate tate tate tate tate tate tate tate	B N  10=Vss  01=Vdd  o-incr  ment ment ment ment	w   U   U   U   U   U   U   U   U   U	Jr_	Uw pin   11=Vd	d(1)  s cali Addr 18 19 1a 1b 1c 1d 1e 1f ALWA 10 18 18 18 19 11 12 13 14 15 16 17 18 19 11 11 12 13 14 15 16 17 18 19 11 11 12 13 14 15 16 17 18 19 11 11 11 11 11 11 11 11 11 11 11 11	pin   9-bit   9-bit   5	DAC of Pianal Pi	OF PIN Sutput  n Stat ke Direct tion Down, Down, Down, Up  Left port tregis a stat trol ALU or  fffff  or (x)  or regis coregi	tate level ection direction direction direction Up Left, Left Up names, ster, tack ck and Ster codes igned) cor) ister ister	O3 PIN (155  n ction serial olled  Up  addre 7-bit  atus F	O2   state   xor)   izer   Oscill	O1   PIN   PIN   ator	OO   state	Poster by Bill Muench