Lab 1 - Report

California State University Long Beach

College of Computer Engineering and Science

CECS 440: Computer Architecture

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1. Introduction

1.1 Executive Summary

This report will act as a brief summary and demonstration of the results from our project. The goal of this project was to construct a 2-bit Adder from a provided 1-bit Adder and to successfully demonstrate the Adder via the provided testbench, and to document the results via Waveform.

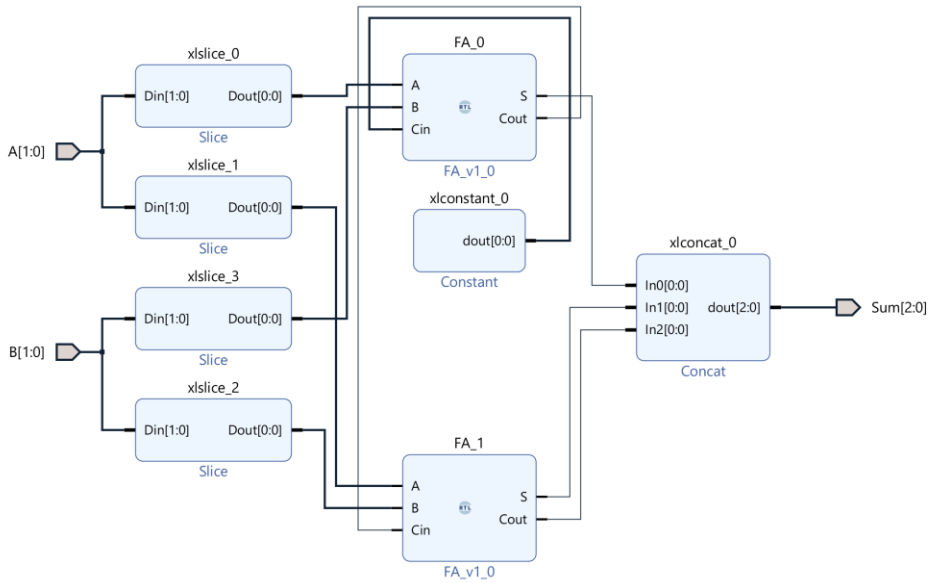
To get the desired result from the 2-bit Adder, we utilized the IP-Integrator to create a block design. The block design utilizes two of the provided Full-Adder files and constructed two slices to allow the two inputs “A” and “B” to access both Full Adders. Additionally, we utilized a Constant of “0” for one of the Adders, and a Concatenator to two Outputs and the Carry-Out from one Full-Adder to create a singular sum.

2. Results

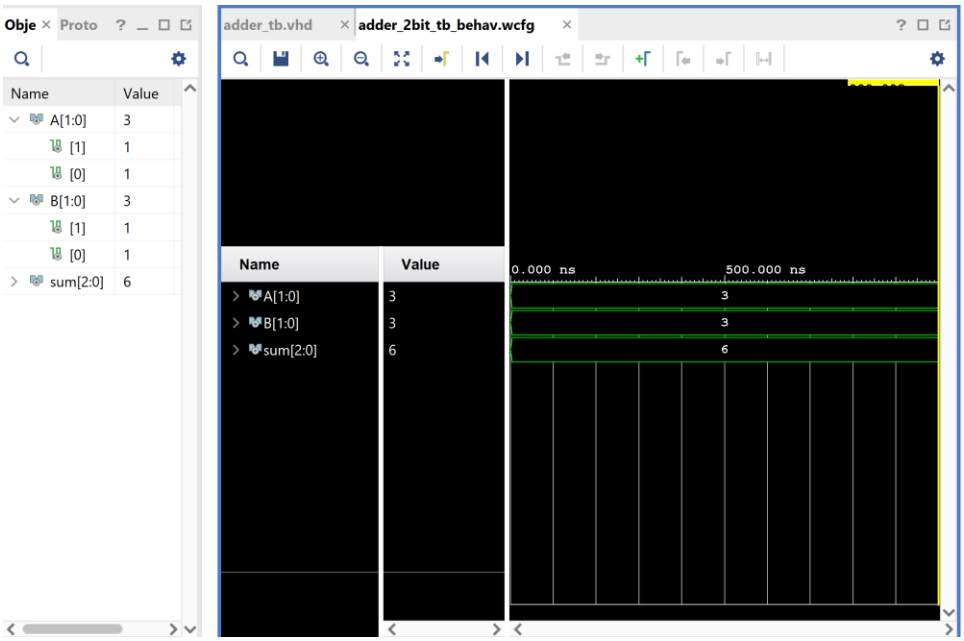
2.1 Waveform Example and IP Design

For this project, we have included the IP-Design and waveform as documentation for our results, as seen below.

Below is the IP-Design for the 2-bit Adder:



Below is the demonstrated waveform for the 2-bit Adder:



2.2 Video Demonstration

For the demonstration of the project, we have recorded a video showing the design, simulation, and results of the project.

Youtube video link: https://youtu.be/anzMAcqFp2g