# UNIVERSAL ISM BAND FSK TRANSCEIVER MODUL

RFM12

RFM12 ist ein kostengünstiges ISM Band Transceiver-Modul mit integriertem PLL. Über die integrierte SPI-Schnittstelle kann das RFM12-Modul komfortabel von einem Microcontroller programmiert und konfiguriert werden.


Features:

- Hervorragendes Preis/Leistungsverhältnis
- keine Abstimmung notwendig
- PLL und Zero-IF Technologie
- Schnelle PLL Abstimmzeit
- Hochauflösende PLL mit 2.5 KHz Schritten
- Hohe Datenrate (bis zu 115.2 kbps mit internen Demodulator，mit externen RC-Filter bis zu 256 kbps)
- Differential-Antennen-Eingang
- Automatische Antennenabstimmung
- Programmierbare TX-Frequenz-Abweichung (von 15 bis 240 KHz)
- Programmierbare Empfänger-Bandbreite (von 67 bis 400 kHz)
- Analoge und digitale Signalstärkeauswertung (ARSSI/DRSSI)
- AFC
- DQD
- Interne Datenfilterung und Clock-Recovery
- RX Synchron-Pattern Erkennung
- SPI-Schnittstelle
- Clock- und Reset-Signal Ausgang für externen Mikrokontroller
- 16 Bit RX Daten FIFO
- Zwei 8 Bit TX Daten Register
- 10MHz Quarz für PLL-Timing
- Wakeup Timer
- 2.2...5.4V- Betriebsspannung
- Niedriger Stromverbrauch
- Standby-Strom weniger als 0.3uA
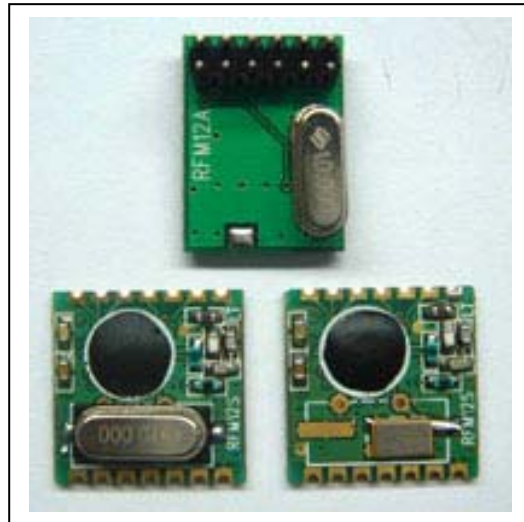
Typische Anwendungen：

• Fernbedienung

• Fernbedienungsempfänger

• Schnurlose Datenübertragung

• Sicherheitssysteme

• Spielzeug

• Reifenluftdruck-Monitoring-System

Pin-Belegung：
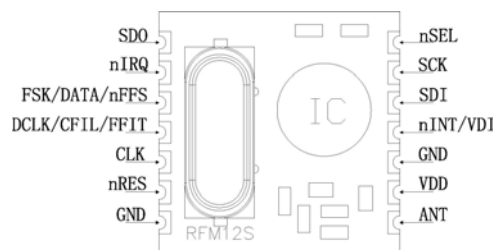
Bezeichnung	Typ	Funktion
nINT/VDI	DI/ DO	Interrupt input (active low)/Valid data indicator
VDD	S	Positive power supply
SDI	DI	SPI data input
SCK	DI	SPI clock input
nSEL	DI	Chip select (active low)
SDO	DO	Serial data output with bus hold
nIRQ	DO	Interrupts request output （active low）
FSK/DATA/nFFS	DI/DO/DI	Transmit FSK data input/ Received data output (FIFO not used)/ FIFO select
DCLK/CFIL/FFIT	DO/AIO/DO	Clock output (no FIFO)/ external filter capacitor(analog mode)/ FIFO interrupts(active high)when FIFO level set to 1, FIFO empty interruption can be achieved
CLK	DO	Clock output for external microcontroller
nRES	DIO	Reset output （active low）
GND	S	Power ground

Electrical Parameter：

Maximum（not at working mode）

symbol	parameter	minimum	maximum	Unit
V_{dd}	Positive power supply	-0.5	6.0	V
V_{in}	All pin input level	-0.5	Vdd+0.5	V
I_{in}	Input current except power	-25	25	mA
ESD	Human body model		1000	V
T_{st}	Storage temperature	-55	125	℃
T_{ld}	Soldering temperature(10s)		260	℃

Recommended working range

symbol	parameter	minimum	maximum	Unit
V_{dd}	Positive power supply	2.2	5.4	V
T_{op}	Working temperature	-40	85	℃

DC characteristic

symbol	parameter	Remark	minimum	typical	maximum	Unit
$I_{dd\_TX\_0}$	Supply current (TX mode, P_{out} = 0dBm)	433MHz band		13		mA
$I_{dd\_TX\_PMAX}$	Supply current (TX mode, P_{out} = P_{max})	433MHz band		21		mA
I_{dd_RX}	Supply current (RX mode)	433MHz band		10		mA
I_x	Stand by current	Crystal and base band on		3．0	3．5	mA
I_{pd}	Sleep mode current	All blocks off		0.3		uA
I_{lb}	Low battery detection			0.5		uA
V_{lb}	Low battery step	0.1V per step	2.2		5.3	V
V_{lba}	Low battery detection accuracy			75		mV
V_{il}	Low level input				$0.3*V_{dd}$	V
V_{ih}	High level input		$0.7*V_{dd}$			V
I_{il}	Leakage current	V_{il}=0V	-1		1	uA
I_{ih}	Leakage current	V_{ih}=V_{dd}, V_{dd}=5.4V	-1		1	uA
V_{ol}	Low level output	I_{ol}=2mA			0.4	V
V_{oh}	High level output	I_{oh}=-2mA	V_{dd}-0.4			V

AC characteristic

symbol	parameter	remark	min	typical	max	Unit
f_{ref}	PLL frequency		8	10	12	MHz
f_{LO}	frequency (10MHz crystal used)	433 MHz band, 2.5KHz step	430.24		439.75	MHz

BW	Receiver bandwidth	1	60	67	75	KHz
		2	120	134	150	
		3	180	200	225	
		4	240	270	300	
		5	300	350	375	
		6	360	400	450	
t_{lock}	PLL lock time	After 10MHz step hopping, frequency error <10 kHz		20		us
BR	Data rate	With internal digital demodulator	0.6		115.2	kbps
BR_A	Data rate	With external RC filter			256	kbps
P_{min}	sensitivity	BW=134KHz,BR=1.2kbps		-102	-96	dBm
AFC_{range}	AFC working range	df_{FSK} FSK deviation in the received signal		0.8* df_{FSK}		
RS_A	RSSI accuracy			±5		dB
RS_R	RSSI range			46		dB
C_{ARSSI}	ARSSI filter			1		nF
RS_{STEP}	RSSI programmable step			6		dB
RS_{RESP}	DRSSI response time	RSSI output high after valid , CARRSI=5nF		500		us

AC characteristic(Transmitter)

symbol	parameter	remark	min	typical	max	Unit
P_{max}	Available output power with optimal antenna impedance	433MHZ band		8		dbm
P_{out}	Typical output power	Selectable in 3 dB steps	P_{max}-21		P_{max}	dbm

C_o	Output capacitance (set by the automatic antenna tuning circuit)			2	2.6	3.2	pf
Q_o	Quality factor of the output capacitance			13	15	17	
L_{out}	Output phase noise	100 kHz from carrier 1 MHz from carrier				-75 -85	dbc/HZ
BR	FSK bit rate					256	kbps
df_{fsk}	FSK frequency deviation	Programmable in 15 kHz steps		15		240	kHZ

AC characteristic(Turn-on/Turnaround timings)

symbol	parameter	remark	min	typical	max	Unit
T_{st}	Crystal oscillator startup time	Crystal ESR < 100			5	ms
$T_{tx\_rx\_XTAL\_ON}$	Transmitter - Receiver turnover time	Synthesizer off, crystal oscillator on		450		us
$T_{rx\_tx\_XTAL\_ON}$	Receiver - Transmitter turnover time	Synthesizer off, crystal oscillator on		350		us
$T_{tx\_rx\_SYNT\_ON}$	Transmitter - Receiver turnover time	Synthesizer on, crystal oscillator on		425		us
$T_{rx\_tx\_SYNT\_ON}$	Receiver - Transmitter turnover time	Synthesizer on, crystal oscillator on		300		us
C_{xl}	Crystal load capacitance	Programmable in 0.5 pF steps, tolerance+/- 10%	8.5		16	pf
t_{POR}	Internal POR timeout	After V_{dd} has reached 90% of final value			100	ms
t_{PBt}	Wake-up timer clock period	Calibrated every 30 seconds	0.96		1.05	ms
$C_{in, D}$	Digital input apacitance				2	pf
$t_{r, f}$	Digital output rise/fall time	15pF pure capacitive load			10	ns

Mechanical Dimension

（units in mm）

SMD PACKAGE（S1）
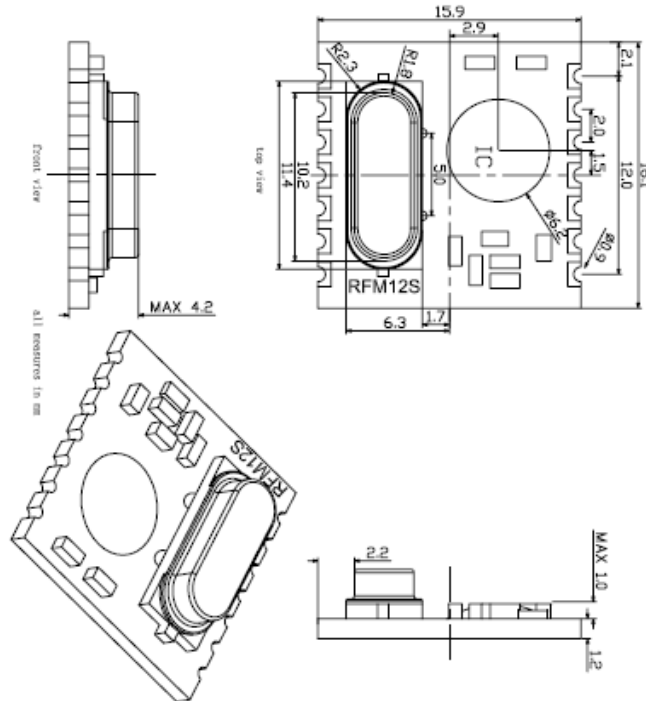
Module Model Definition

model=module-operation band

RFM12 – 433-D/S

module type   operation band   Package

example：1，RFM12 module at 433MHz band, SMD : RFM12-433-S。

RF12 programming guide

1. Brief description

RF12 is a low cost FSK transceiver IC witch integrated all RF functions in a single chip. It only need a MCU, a crystal, a decouple capacitor and antenna to build a hi reliable FSK transceiver system.

RF12 supports a command interface to setup frequency, deviation, output power and also data rate. No need any hardware adjustment when using in frequency-hopping applications

RF12 can be used in applications such as remote control toys, wireless alarm, wireless sensor, wireless keyboard/mouse, home-automation and wireless data collection.

2. Commands

1. Timing diagram
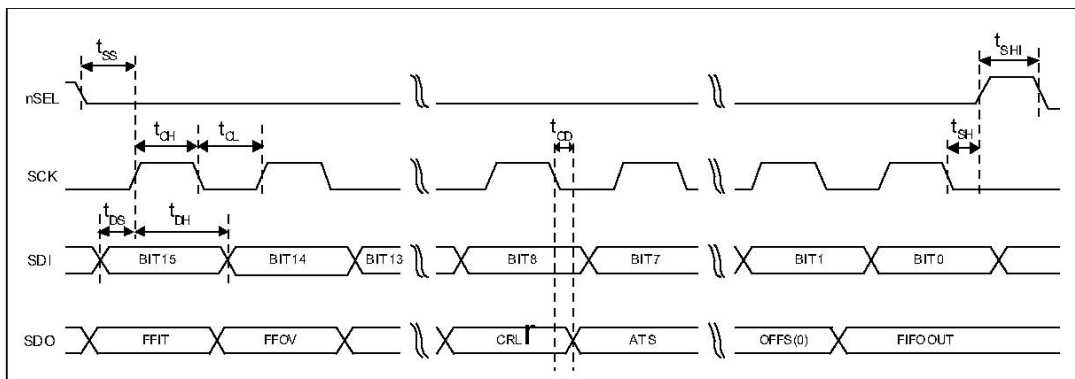
2. Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	0	0	0	0	0	el	ef	0	1	x3	x2	x1	x0	8008h

e l: Enable TX register
e f: Enable RX FIFO buffer

x3..x0: select crystal load capacitor

x3	x2	x1	x0	load capacitor [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
……		……		
1	1	1	0	15.5
1	1	1	1	16.0

3. Power Management Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	0	0	0	1	0	er	ebb	et	es	ex	eb	ew	dc	8208h

er： Enable receiver

ebb： Enable base band block

et： Enable transmitter

es： Enable synthesizer

ex： Enable crystal oscillator

eb： Enable low battery detector

ew： Enable wake-up timer

dc： Disable clock output of CLK pin

4. Frequency Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A680h

f11..f0: Set operation frequency:

433band: Fc=430+F*0.0025 MHz

Fc is carrier frequency and F is the frequency parameter. 36≤F≤3903

5. Data Rate Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	cs	r6	r5	r4	r3	r2	r1	r0	C623h

r6..r0: Set data rate:

BR=10000000/29/（R+1）/（1+cs*7）

6. Receiver Control Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	p20	d1	d0	i2	i1	i0	g1	g0	r2	r1	r0	9080h

p20: select function of pin20

p20	
0	External interrupt in
1	VDI output

i2..i0:select baseband bandwidth

i2	i1	i0	Baseband Bandwidth [kHz]
0	0	0	reserved
0	0	1	400
0	1	0	340
0	1	1	270
1	0	0	200
1	0	1	134
1	1	0	67
1	1	1	reserved

d1..d0: select VDI response time

d1	d0	Response
0	0	Fast
0	1	Medium
1	0	Slow
1	1	Always on

g1..g0: select LNA gain

g1	g0	LNA gain (dBm)
0	0	0
0	1	-6
1	0	-14
1	1	-20

r2..r0: select DRSSI threshold

r2	r1	r0	RSSIsetth [dBm]
0	0	0	-103
0	0	1	-97
0	1	0	-91
0	1	1	-85
1	0	0	-79
1	0	1	-73
1	1	0	-67
1	0	1	-61

The actual DRSSI threshold is related to LNA setup:

$$RSSI_{th} = RSSI_{setth} + G_{LNA.}$$

7．**Data Filter Command**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	al	ml	1	s	1	f2	f1	f0	C22Ch

al: Enable clock recovery auto-lock

ml: Enable clock recovery fast mode

s1..s0: select data filter type

s1	s0	Filter type
0	0	OOK
0	1	Digital filter
1	0	reserved

f1..f0: Set DQD threshold

8．**Output and FIFO mode Command**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	f3	f2	f1	f0	0	al	ff	dr	CA80h

f3..f0: Set FIFO interrupt level

al: select FIFO fill start condition

al	
0	Sync-word
1	Always

ff: Enable FIFO fill

dr：   Disable hi sensitivity reset mode

9．**Receiver FIFO Read Command**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	B000h

This command is used to read FIFO data when FFIT interrupt generated. FIFO data output starts at 8th SCK period.

10.   **AFC Command**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	a1	a0	rl1	rl0	st	fi	oe	en	C4F7h

a1..a0: select AFC auto-mode：

a1	a0	
0	0	Controlled by MCU
0	1	Run once at power on
1	0	Keep offset when VDI hi
1	1	Keeps independently from VDI

rl1..rl0: select range limit

r1	r0	range（fres）
0	0	No restriction
0	1	+15/-16
1	0	+7/-8
1	1	+3-4

st: st goes hi will store offset into output register

fi: Enable AFC hi accuracy mode

oe: Enable AFC output register

en: Enable AFC funcition

11.   **AFC Command**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	1	1	0	0	mp	m3	m2	m1	m0	0	p2	p1	p0	9800h

m: select modulation polarity

m2..m0: select frequency deviation:

m3	m2	m1	m0	frequency deviation [kHz]
0	0	0	0	15
0	0	0	1	30
0	0	1	0	45
0	0	1	1	60
0	1	0	0	75
0	1	0	1	90
0	1	1	0	105
0	1	1	1	120
1	0	0	0	135

1	0	0	1	150
1	0	1	0	165
1	0	1	1	180
1	1	0	0	195
1	1	0	1	210
1	1	1	0	225
1	1	1	1	240

p2..p0: select output power

p2	p1	p0	Output power[dBm]
0	0	0	0
0	0	1	-3
0	1	0	-6
0	1	1	-9
1	0	0	-12
1	0	1	-15
1	1	0	-18
1	0	1	-21

12. Transmitter Register Write Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	1	0	0	0	t7	t6	t5	t4	t3	t2	t1	t0	B8AAh

This command is use to write a data byte to RF12 and then RF12 transmit it

13. Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up period is determined by:

$$T_{wake-up} = M * 2^R \ [ms]$$

For continual operation, bit 'et' must be cleared and set

14. 低占空比命令（Low Duty-Cycle Command）

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	d6	d5	d4	d3	d2	d1	d0	en	C8OEh

d6..d0: Set duty cycle

D.C. = (D * 2 +1) / M *100%

en：Enable low duty cycle mode

15. Low Battery Detector and Microcontroller Clock Divider Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	d2	d1	d0	v4	v3	v2	v1	v0	C000h

d2..d0: select frequency of CLK pin

d2	d1	d0	Clock frequency[MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

CLK signal is derive form crystal oscillator and it can be applied to MCU clock in to save a second crystal.

If not used, please set bit "dc" to disable CLK output

To integrate the load capacitor internal can not only save cost, but also adjust reference frequency by software

v4..v0: Set threshold voltage of Low battery detector：
Vlb=2.2+V*0.1 [V]

16. Status Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-

This command starts with a 0 and be used to read internal status register