	ADDRESS	OFFSET	NAME	VALUE	NOTES
BASE	0x50200000	-	BASE ADDRESS		
CTRL	0x50200000	0x000	PIO CONTROL REGISTER	0x00000001	Enable SM0
FSTAT	0x50200004	0x004	FIFO STATUS REGISTER	0x0f010f01	
FDEBUG	0x50200008	0x008	FIFO DEBUG REGISTER	0x00000000	
FLEVEL	0x5020000c	0x00c	FIFO LEVELS	0x00000000	
TXF0	0x50200010	0x010	DIRECT WRITE ACCESS TO TX FIFO	0x000000ff	Direct write access to the TX FIFO for this state machine. Each write pushes one word to the FIFO. Attempting to write to a full FIFO has no effect on the FIFO state or contents, and sets the sticky FDEBUG_TXOVER error flag for this FIFO
RXF0	0x50200020	0x020	DIRECT READ ACCESS TO RX FIFO	0x00000000	Direct read access to the RX FIFO for this state machine. Each read pops one word from the FIFO. Attempting to read from an empty FIFO has no effect on the FIFO state, and sets the sticky FDEBUG_RXUNDER error flag for this FIFO. The data returned to the system on a read from an empty FIFO is undefined
INSTR_MEM0	0x50200048	0x048	WRITE ONLY ACCESS TO INSTRUCTION MEMORY LOCATION 0	0x00000000	Write-only access to instruction memory location N
...	...	...	...	...	...
INSTR_MEM31	0x502000x4	0x0c4	WRITE ONLY ACCESS TO INSTRUCTION MEMORY LOCATION 31	0x00000000	Write-only access to instruction memory location N
SM0_CLKDIV	0x502000c8	0x0c8	CLOCK DIVISOR REGISTER	0x000fa000	Clock divisor register for state machine N Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)
SM0_EXECCTRL	0x502000cc	0x0cc	EXECUTION/BEHAVIORAL SETTINGS	0x00000000	AS Side bit is enabled and default setting
SM0_SHIFTCTRL	0x502000d0	0x0d0	CONTROL OF INPUT/OUTPUT SHIFT REGISTERS	0x00000000	Default Values
SM0_ADDR	0x502000d4	0x0d4	CURRENT INSTRUCTION ADDRESS	0x00000000	Default Values
SM0_INSTR	0x502000d8	0x0d8	READ/WRITE TO SEE OR EXECUTE AN INSTRUCTION	0x00006221	instruction value get from ws2812.pio.h
SM0_PINCTRL	0x502000dc	0x0dc	STATE MACHINE PIN CONTROL	0x20003000	Side set number is 0