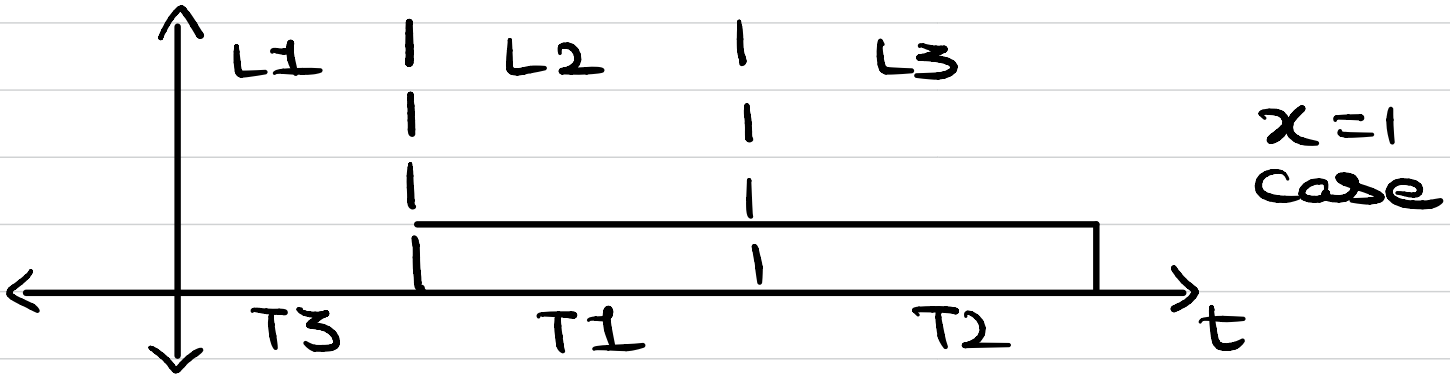
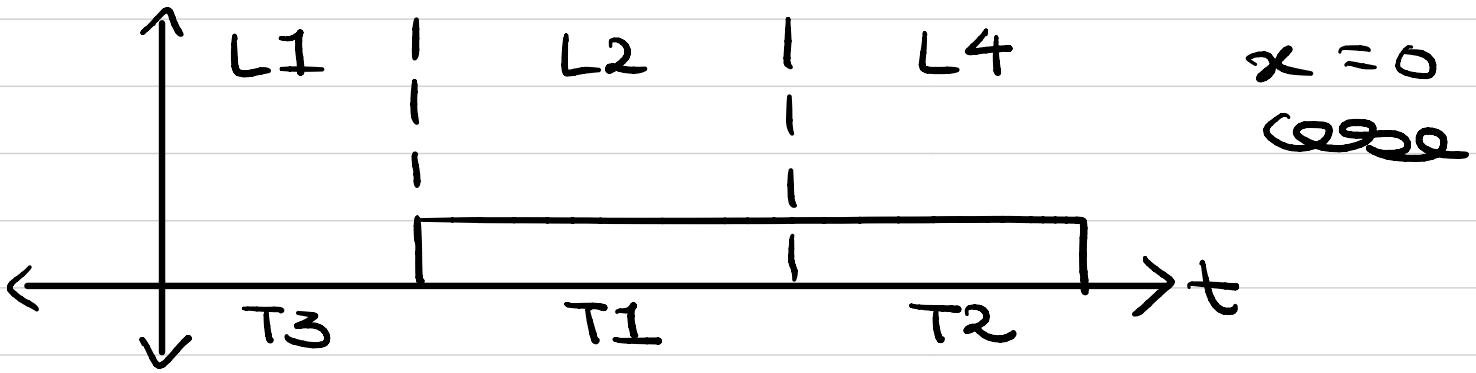
Paper Modelling of Code

BitLoop :-

```
L1   out x , 1          side 0 [T3-1]
L2   Jmp !x do_zero     side 1 [T1-1]
     Do_one
L3   Jmp Bitloop        side 1 [T2-1]
     Do_zero
L4   NOP                side 0 [T2-1]
```





Current Instruction	Data in FIFO	SM Stalled?	Delay Cycles Left	Value of OSR	SMX	LED State
L1	Yes	No	2	0x	1	0
L2	Yes	No	1	0x	1	1
L3	Yes	No	4	0x	1	1
L1	Yes	No	2	0x	1	0