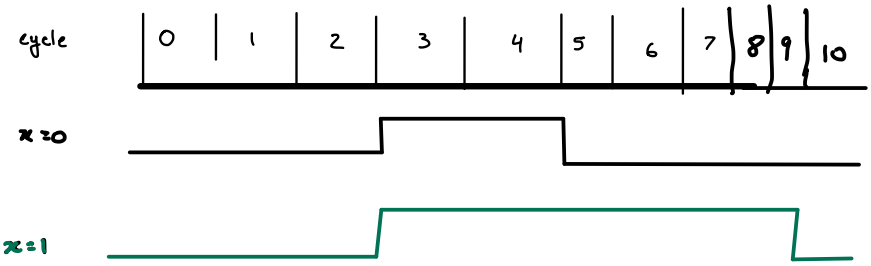
```
.wrap_target
bitloop:
    L1 out x, 1  side 0 [T3 - 1]
    L2 jmp !x do_zero  side 1 [T1 - 1]
do_one:
    L3 jmp bitloop  side 1 [T2 - 1]
do_zero:
    L4 nop  side 0 [T2 - 1]
.wrap
```

$T_1 = 2$, $T_2 = 5$, $T_3 = 3$

Assume x = 0

Assume x = 1

GPIO



cycle	0		1		2		3		4		5		6		7	
CLK	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Current Instruction	L1		L2		L4 / L3		L1		Repeat →							
Data in FIFO?	N		Y		N Y		N		Repeat →							
SM Stalled?	Y		N		Y N		Y		Repeat →							
Delay cycle	3		2		5 5		3		Repeat →							
OSR	x → 0		0 1		0 1		x → 0		Repeat →							
X	0		0 1		0 1		0		Repeat →							
GPIO	0		1		0 1		0		Repeat →							
									Repeat →							