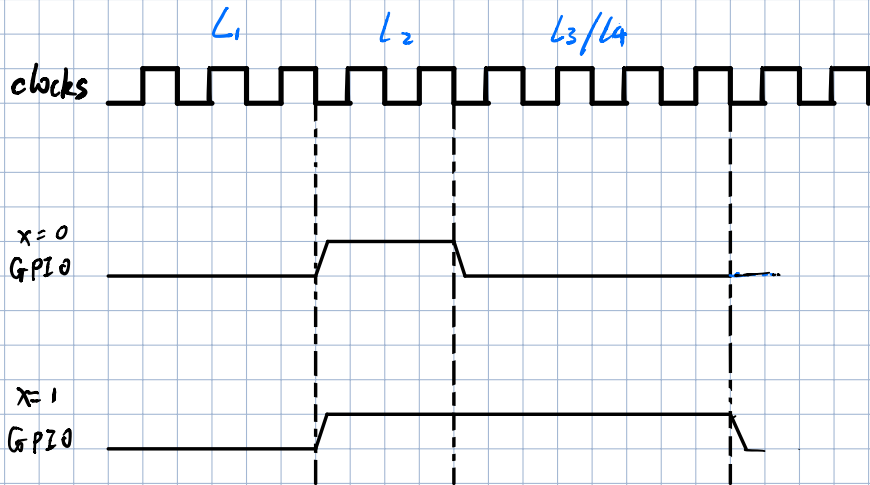


```

Wrap-target
bitloop:
L1: outb x, 1      side 0 [T3-1];
L2: jmp !x do-zero side 1 [T2-1];
do-zero:
L3: jmp bitloop   side 1 [T2-1];
do-zero:
L4: nop          side 0 [T2-1];
... wrap:

```

$T_1 = 2; T_2 = 5; T_3 = 3$



Current instr

Data in FIFO

SM stall

Delays left

OSR value

$x=0$

LED state

$x=1$

LED state