| | ADDRESS | OFFSET | NAME |
|---|---|---|---|
| PIO0_BASE | 0x50200000 | NA | Base |
| CTRL | 0x50200000 | 0x000 | |
| FSTAT | 0x50200004 | 0x004 | |
| FDEBUG | 0x50200008 | 0x008 | |
| FLEVEL | 0x5020000c | 0x00c | |
| TXF0 | 0x50200010 | 0x010 | |
| TXF1 | 0x50200014 | 0x014 | |
| TXF2 | 0x50200018 | 0x018 | |
| TXF3 | 0x5020001c | 0x01c | |
| RXF0 | 0x50200020 | 0x020 | |
| RXF1 | 0x50200024 | 0x024 | |
| RXF2 | 0x50200028 | 0x028 | |
| RXF3 | 0x5020002c | 0x02c | |
| IRQ | 0x50200030 | 0x030 | |
| IRQ_FORCE | 0x50200034 | 0x034 | |
| INPUT_SYNC_BYPASS | 0x50200038 | 0x038 | |
| DBG_PADOUT | 0x5020003c | 0x03c | |
| DBG_PADOE | 0x50200040 | 0x040 | |
| DBG_CFGINFO | 0x50200044 | 0x044 | |
| INSTR_MEM0 | 0x50200048 | 0x048 | |
| INSTR_MEM1 | 0x5020004c | 0x04c | |
| INSTR_MEM2 | 0x50200050 | 0x050 | |
| INSTR_MEM3 | 0x50200054 | 0x054 | |
| INSTR_MEM4 | 0x50200058 | 0x058 | |
| INSTR_MEM5 | 0x5020005c | 0x05c | |
| INSTR_MEM6 | 0x50200060 | 0x060 | |
| INSTR_MEM7 | 0x50200064 | 0x064 | |
| INSTR_MEM8 | 0x50200068 | 0x068 | |
| INSTR_MEM9 | 0x5020006c | 0x06c | |
| INSTR_MEM10 | 0x50200070 | 0x070 | |
| INSTR_MEM11 | 0x50200074 | 0x074 | |
| INSTR_MEM12 | 0x50200078 | 0x078 | |
| INSTR_MEM13 | 0x5020007c | 0x07c | |
| INSTR_MEM14 | 0x50200080 | 0x080 | |
| INSTR_MEM15 | 0x50200084 | 0x084 | |
| INSTR_MEM16 | 0x50200088 | 0x088 | |
| INSTR_MEM17 | 0x5020008c | 0x08c | |
| INSTR_MEM18 | 0x50200090 | 0x090 | |
| INSTR_MEM19 | 0x50200094 | 0x094 | |
| INSTR_MEM20 | 0x50200098 | 0x098 | |
| INSTR_MEM21 | 0x5020009c | 0x09c | |
| INSTR_MEM22 | 0x502000a0 | 0x0a0 | |
| INSTR_MEM23 | 0x502000a4 | 0x0a4 | |
| INSTR_MEM24 | 0x502000a8 | 0x0a8 | |

| | | |
|---|---|---|
| INSTR_MEM25 | 0x502000ac | 0x0ac |
| INSTR_MEM26 | 0x502000b0 | 0x0b0 |
| INSTR_MEM27 | 0x502000b4 | 0x0b4 |
| INSTR_MEM28 | 0x502000b8 | 0x0b8 |
| INSTR_MEM29 | 0x502000bc | 0x0bc |
| INSTR_MEM30 | 0x502000c0 | 0x0c0 |
| INSTR_MEM31 | 0x502000c4 | 0x0c4 |
| SM0_CLKDIV | 0x502000c8 | 0x0c8 |
| SM0_EXECCTRL | 0x502000cc | 0x0cc |
| SM0_SHIFTCTRL | 0x502000d0 | 0x0d0 |
| SM0_ADDR | 0x502000d4 | 0x0d4 |
| SM0_INSTR | 0x502000d8 | 0x0d8 |
| SM0_PINCTRL | 0x502000dc | 0x0dc |
| SM1_CLKDIV | 0x502000e0 | 0x0e0 |
| SM1_EXECCTRL | 0x502000e4 | 0x0e4 |
| SM1_SHIFTCTRL | 0x502000e8 | 0x0e8 |
| SM1_ADDR | 0x502000ec | 0x0ec |
| SM1_INSTR | 0x502000f0 | 0x0f0 |
| SM1_PINCTRL | 0x502000f4 | 0x0f4 |
| SM2_CLKDIV | 0x502000f8 | 0x0f8 |
| SM2_EXECCTRL | 0x502000fc | 0x0fc |
| SM2_SHIFTCTRL | 0x50200100 | 0x100 |
| SM2_ADDR | 0x50200104 | 0x104 |
| SM2_INSTR | 0x50200108 | 0x108 |
| SM2_PINCTRL | 0x5020010c | 0x10c |
| SM3_CLKDIV | 0x50200110 | 0x110 |
| SM3_EXECCTRL | 0x50200114 | 0x114 |
| SM3_SHIFTTCTRL | 0x50100118 | 0x118 |
| SM3_ADDR | 0x5020011c | 0x11c |
| SM3_INSTR | 0x50200120 | 0x120 |
| SM3_PINCTRL | 0x50200124 | 0x124 |
| INTR | 0x50200128 | 0x128 |
| IEQ0_INTE | 0x5020012c | 0x12c |
| IEQ0_INTF | 0x50200130 | 0x130 |
| IRQ0_INTS | 0x50200134 | 0x134 |
| IEQ1_INTE | 0x50200138 | 0x138 |
| IEQ1_INTF | 0x5020013c | 0x13c |
| IEQ1_INTS | 0x50200140 | 0x140 |

VALUE

reserved,0x0,0x0,0x0
reserved, 0,0,0,1
reserved, 0,reserved,0,reserved,0,reserved,0
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0
0
0
0
1
0
0
0
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reserved,0
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reserved,0

reserved,0
reserved,0
reserved,0
reserved,0
reserved,0
reserved,0
reserved,0
0,0,reserved
0(25-bit),reserved,0(5-bit)
0(16-bit), reserved
reserved,0(5-bit)
reserved,0
0
0,0,reserved
0(25-bit),reserved,0(5-bit)
0(16-bit), reserved
0(16-bit), reserved
reserved,0
0
0,0,reserved
0(25-bit),reserved,0(5-bit)
0(16-bit), reserved
0(16-bit), reserved
reserved,0
0
0,0,reserved
0(25-bit),reserved,0(5-bit)
0(16-bit), reserved
0(16-bit), reserved
reserved,0
0
reserved,0,0,0,1,0,0,0,0,0,0,0,0
reserved, 0,0,0,1,0,0,0,0,0,0,0,0
reserved, 0,0,0,1,0,0,0,0,0,0,0,0
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reserved, 0,0,0,1,0,0,0,0,0,0,0,0
reserved, 0,0,0,1,0,0,0,0,0,0,0,0
reserved, 0,0,0,1,0,0,0,0,0,0,0,0

Notes

No reset
RX FIFO FULL
no overflow, underflow
RX0 is high
pio_sm_put_blocking
no transmit
no transmit
no transmit
RX0 high
No use
NO use
NO use
no clear
no force
no bypass, default
GPIO 11 and 12 used
GPIO 11 and 12 used
4 SM per PIO
write not enabled
write not enabled
write not enabled
write not enabled
write not enabled
write not enabled
write not enabled
write not enabled
write not enabled
write not enabled
write not enabled
write not enabled
write not enabled
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write not enabled
write not enabled
write not enabled

write not enabled
write not enabled
write not enabled
write not enabled
write not enabled
write not enabled
write not enabled
    65536 freq
  None applied
  None applied
       SM0
  no read/write
no in/out effect
    65536 freq
  None Applied
  None Applied
       SM0
  no read/write
no in/out effect
    65536 freq
  None applied
  None applied
       SM0
  no read/write
no in/out effect
      65536
  None applied
  None applied
       SM0
  no read/write
no in/out effect
     SM0 use
     SM0 use
     SM0 use
     SM0 use
     SM0 use
     SM0 use
     SM0 use