

.wrap-target

bitloop:

out x, 1 side 0 [T₃-1]

jmp !x do-zero side 1 [T₁-1]

do-one:

jmp bitloop side 1 [T₂-1]

do-zero:

nop side 0 [T₂-1]

Label 0

Label 1

L 1

L 2

Label 2

L 3

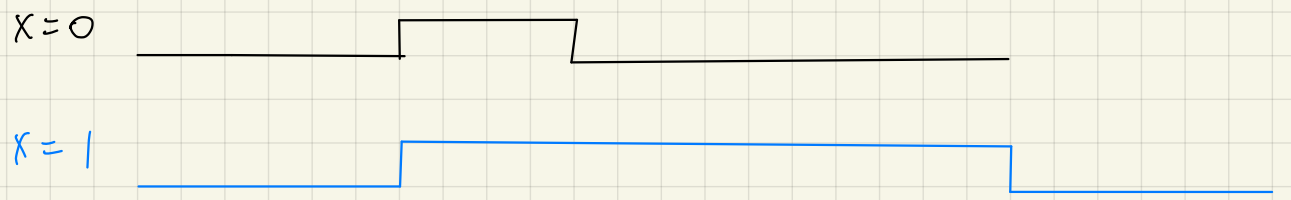
Label 3

L 4

T₁ = 2
T₂ = 5
T₃ = 3
Assume x = 0
Assume x = 1

GPIO:

cycle | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |



.wrap

cycle	0	1	2	3	4	5	6	7	
CLK	1	0	1	0	1	0	1	0	1
current instruction	L1	L2	L4/L3	L1	Repeat cycle 1 → 3				
Data in FIFO?	N	Y	NY	N	Repeat Cycle 1 → 3				
SM stalled?	Y	N	YN	Y	Repeat cycle 1 → 3				
Delay cycle	3	2	55	3	Repeat Cycle 1 → 3				
OSR	x → 0	01	01	x → 0	Repeat Cycle 1 → 3				
X	0	01	01	0	Repeat Cycle 1 → 3				
LED pin (GPIO)	0	1	01	0	Repeat Cycle 1 → 3				