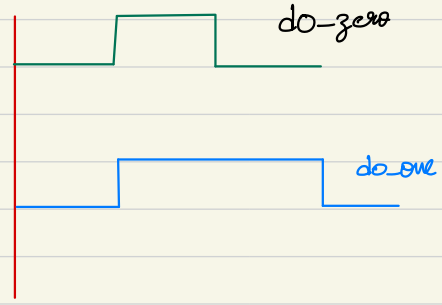


• wrap_target

```

littloop:
L1 out  x, 1 side 0 [T3-1];
L2 jmp  !x do-zero side 1 [T1-1];
do_one:
L3 jmp  littloop side 1 [T2-1];
d1_zero:
L4 nop   side 0 [T2-1];
  
```

• wrap



cycle	0	1	2
Current Instruction	L1	L2	L3
FIFO	1	1	1
SM-STALL	0	0	0
Delay cycles left	3	2	5
OSR	0	0	0
LED	0	1	0