	ADDRESS	OFFSET	NAME	VALUE	Notes
BASE	0x50200000		PIO0_BASE		Init PIO0
CTRL	0x50200000	0x000	CLKDIV_RESTART SM_RESRART SM_ENABLE	0x00000001	PIO control register PIO = 0 SM = 0
FSTAT	0x50200004	0x004	TXEMPTY TXFULL RXEMPTY RXFULL	0x0f000f01	FIFO status register Tx FIFO is empty Rx FIFO is empty
FDEBUG	0x50200008	0x008	TXSTALL TXOVER RXUNDER RXSTALL	0x00000000	FIFO debug register
FLEVEL	0x5020000c	0x00c	RX3 TX3 RX2 TX2 RX1 TX1 RX0 TX0	0x00000000	FIFO level Init RX and TX
TXF0	0x50200010	0x010	TXF0	0x00000000	TX FIFO for SM0
TXF1	0x50200014	0x014	TXF1	0x00000000	TX FIFO for SM1
TXF2	0x50200018	0x018	TXF2	0x00000000	TX FIFO for SM2
TXF3	0x5020001c	0x01c	TXF3	0x00000000	TX FIFO for SM3
RXF0	0x50200020	0x020	RXF0	0x00c8a2c8	32 bits GRB color
RXF1	0x50200024	0x024	RXF1	0x00c8a2c8	32 bits GRB color
RXF2	0x50200028	0x028	RXF2	0x00c8a2c8	32 bits GRB color
RXF3	0x5020002c	0x02c	RXF3	0x00c8a2c8	32 bits GRB color
INSTR_MEM0	0x50200030	0x030	INSTR_MEM0	0x00000000	Write-only Reset state
INSTR_MEMn	...	...	INSTR_MEMn	...	Mem0-Mem31 = 0
INSTR_MEM31	0x502000c4	0x0c4	INSTR_MEM31	0x00000000	Write-only Reset state
SM0_CLKDIV	0x502000c8	0x0c8	INT FRAV	0x000fa000	Clock divisor register for state machine 0 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)
SM0_EXECCTRL	0x502000cc	0x0cc	EXEC_STALLED SIDE_EN SIDE_PINDIR JMP_PIN OUT_EN_SEL INLINE_OUT_EN OUT_STICKY WRAP_TOP WRAP_BOTTOM STATUS_SEL STATUS_N	0x00017a00	Execution/behavioural settings for state machine 0
SM0_SHIFTCRTL	0x502000d0	0x0d0	FJOIN_RX FJION_TX PULL_THRESH PUSH_THRESH OUT_SHIFTDIR IN_SHIFTDIR AUTOPULL AUTOPUSH	0x40060000	Control behaviour of the input/output shift registers for state machine 0
SM0_ADDR	0x502000d4	0x0d4		0x00000014	Current instruction address for state machine 0
SM0_INSTR	0x502000d8	0x0d8		0x00006221	Read the instruction currently addressed by state machine
SM0_PINCTRL	0x502000dc	0x0dc	SIDESET_COUNT SET_COUNT OUT_COUNT IN_BASE SIDESET_BASE SET_BASE OUT_BASE	0x20003000	State machine pin control 0
SM1_CLKDIV	0x50200000	0x0e0	INT FRAV	0x00010000	Clock divisor register for state machine 1 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)
SM1_EXECCTRL	0x5020000	0x0e4	EXEC_STALLED SIDE_EN SIDE_PINDIR JMP_PIN OUT_EN_SEL INLINE_OUT_EN OUT_STICKY WRAP_TOP WRAP_BOTTOM STATUS_SEL STATUS_N	0x0001f000	Execution/behavioural settings for state machine 1
SM1_SHIFTCTRL	0x50200000	0x0e8	FJOIN_RX FJION_TX PULL_THRESH PUSH_THRESH OUT_SHIFTDIR IN_SHIFTDIR AUTOPULL AUTOPUSH	0x000c000	Control behaviour of the input/output shift registers for state machine 1
SM1_ADDR	0x50200ec	0x0ec	SM1_ADDR	0x0000000	Current instruction address for state machine 1
SM1_INSTR	0x50200f0	0x0f0	SM1_INSTR	0x0000fcfe	Read the instruction currently addressed by state machine
SM1_PINCTRL	0x50200f4	0x0f4	SIDESET_COUNT SET_COUNT OUT_COUNT IN_BASE SIDESET_BASE SET_BASE OUT_BASE	0x00000000	State machine pin control 0
SM2_CLKDIV	0x50200f8	0x0f8	INT FRAV	0x00010000	Clock divisor register for state machine 2 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)
SM2_EXECCTRL	0x50200fc	0x0fc	EXEC_STALLED SIDE_EN SIDE_PINDIR JMP_PIN OUT_EN_SEL INLINE_OUT_EN OUT_STICKY WRAP_TOP WRAP_BOTTOM STATUS_SEL STATUS_N	0x0001f000	Execution/behavioural settings for state machine 2
SM2_SHIFTCTRL	0x5020100	0x100	FJOIN_RX FJION_TX PULL_THRESH PUSH_THRESH OUT_SHIFTDIR IN_SHIFTDIR AUTOPULL AUTOPUSH	0x000c0000	Control behaviour of the input/output shift registers for state machine 2
SM2_ADDR	0x5020104	0x104	SM2_ADDR	0x00000000	Current instruction address for state machine 2
SM2_INSTR	0x5020108	0x108	SM2_INSTR	0x0000fcfe	Read the instruction currently addressed by state machine
SM2_PINCTRL	0x502010c	0x10c	SIDESET_COUNT SET_COUNT OUT_COUNT IN_BASE SIDESET_BASE SET_BASE OUT_BASE	0x14000000	State machine pin control 2
SM3_CLKDIV	0x5020110	0x110	INT FRAV	0x00010000	Clock divisor register for state machine 3 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)
SM3_EXECCTRL	0x50200114	0x114	EXEC_STALLED SIDE_EN SIDE_PINDIR JMP_PIN OUT_EN_SEL INLINE_OUT_EN OUT_STICKY WRAP_TOP WRAP_BOTTOM STATUS_SEL STATUS_N	0x0001f000	Execution/behavioural settings for state machine 3
SM3_SHIFTCTRL	0x50200118	0x118	FJOIN_RX FJION_TX PULL_THRESH PUSH_THRESH OUT_SHIFTDIR IN_SHIFTDIR AUTOPULL AUTOPUSH	0x000c0000	Control behaviour of the input/output shift registers for state machine 3
SM3_ADDR	0x5020011c	0x11c	SM3_ADDR	0x00000000	Current instruction address for state machine 3
SM3_INSTR	0x50200120	0x120	SM3_INSTR	0x0000fcfe	Read the instruction currently addressed by state machine
SM3_PINCTRL	0x50200124	0x124	SIDESET_COUNT SET_COUNT OUT_COUNT IN_BASE SIDESET_BASE SET_BASE OUT_BASE	0x14000000	State machine pin control 3