* IS_RGBW = false

```
bitloop:
L0 out x, 1  side 0 [T3-1]      1, 2, 3, 4, 5, 13
L1 jmp !X do_zero  side 1 [T1-1]  6, 7
do_one:
L2 jmp bitloop  side 0 [T2-1]   8, 9, 10, 11, 12
do_zero:
L3 nop          side 0 [T2-1]
```

	T1	T2	3	4	5	6	7	8	9	10	11	12	13
current instruction	L0	L0	L0	L0	L0	L1	L1	L2	L2	L2	L2	L2	L0
data in FIFO?	N	Y	N	N	N	N	N	N	N	N	N	N	N
SM stalled?	Y	Y	N	N	N	N	N	N	N	N	N	N	N
delay cycles remain	—	—	2	1	0	1	0	4	3	2	1	0	2
OSR value?	0x0	0x0	*	△	→								□
x scratch register val?	—	—	1	1	1	1	1	1	1	1	1	1	1
OUTPUT Pin state	0	0	0	0	0	1	1	1	1	1	1	1	0

OSR changes below →

* OSR value: 0x DEBEAD 00

△ 0x BD7D 5A 00

□ 0x 7AFA B4 00