	ADDRESS	OFFSET	NAME	VALUE	notes	SET 0X0000FF
BASE	0x50200000		PIO0_BASE		PIO1 address: 0x50300000	
CTRL	50200000	0x000	PIO control register	0x00000001	PIO control register. SM_ENABLE, SM_RESTART and CLKDIV_RESTART is rest to 0x0.	
FSTAT	50200004	0x00000004	FIFO status register	0x0f000f01	FIFO status register. The first four bits of RXFULL and TXFULL are 0. (pio_fifo_join）	0x0f000f01
FDEBUG	50200008	0x00000008	FIFO debug register	0x00000000	FIFO debug register. The first four bits to be RXSTALL, RXUNDER and TXOVER and TXSTALL are all 0 after resetting.	0x01000e00
FLEVEL	5020000c	0x0000000c	FIFO levels	0x00000000	FIFO levels All of bits of this register is resetted to 0 after the offsetting, no reserved bits for this register.	0x00000000
TXF0	50200010	0x00000010	TX FIFO for SM0	0x00000000	Direct write access to the TX FIFO for this state machine. Each write pushes one word to the FIFO. Attempting to write to a full FIFO has no effect on the FIFO state or contents, and sets the sticky FDEBUG_TXOVER error flag for this FIFO. All of bits of this register is rested to 0 after the offsetting and there is no reserved bits in the register, additionally, there are no message being printed out.	0x00000000
TXF1	50200014	0x00000014	TX FIFO for SM1	0x00000000	Direct write access to the TX FIFO for this state machine. Eachwrite pushes one word to the FIFO. Attempting to write to a fullFIFO has no effect on the FIFO state or contents, and sets thesticky FDEBUG_TXOVER error flag for this FIFO.	0x00000000
TXF2	50200018	0x00000018	TX FIFO for SM2	0x00000000	Direct write access to the TX FIFO for this state machine. Eachwrite pushes one word to the FIFO. Attempting to write to a fullFIFO has no effect on the FIFO state or contents, and sets thesticky FDEBUG_TXOVER error flag for this FIFO.	0x00000000
TXF3	5020001c	0x0000001c	TX FIFO for SM3	0x00000000	Direct write access to the TX FIFO for this state machine. Eachwrite pushes one word to the FIFO. Attempting to write to a fullFIFO has no effect on the FIFO state or contents, and sets thesticky FDEBUG_TXOVER error flag for this FIFO.	0x00000000
RXF0	50200020	0x00000020	RX FIFO for SM0	0x963f69b2	Direct read access to the RX FIFO for this state machine. Each read pops one word from the FIFO. Attempting to read from an empty FIFO has no effect on the FIFO state, and sets the sticky FDEBUG_RXUNDER error flag for this FIFO. The data returned to the system on a read from an empty FIFO is undefined. The rule for setting the value is basically the same as TXFn	0x14fea89d
RXF1	50200024	0x00000024	RX FIFO for SM1	0x245a3d99	Direct read access to the RX FIFO for this state machine. Eachread pops one word from the FIFO. Attempting to read from anempty FIFO has no effect on the FIFO state, and sets the sticky FDEBUG_RXUNDER error flag for this FIFO. The data returned tothe system on a read from an empty FIFO is undefined.	0x0db36757
RXF2	50200028	0x00000028	RX FIFO for SM2	0xadf83d99	Direct read access to the RX FIFO for this state machine. Eachread pops one word from the FIFO. Attempting to read from anempty FIFO has no effect on the FIFO state, and sets the sticky FDEBUG_RXUNDER error flag for this FIFO. The data returned tothe system on a read from an empty FIFO is undefined.	0xb3060127
RXF3	5020002c	0x0000002c	RX FIFO for SM3	0xa8fc7caf	Direct read access to the RX FIFO for this state machine. Eachread pops one word from the FIFO. Attempting to read from anempty FIFO has no effect on the FIFO state, and sets the sticky FDEBUG_RXUNDER error flag for this FIFO. The data returned tothe system on a read from an empty FIFO is undefined.	oxb8250d8e
INSTR_MEM0	50200030	0x00000030		0x00000000	Write-only access to instruction memory location 0. The first half of this registe is resetted to 0 with the second half being the reserved ones.	0x00000000
INSTR_MEMn	50200030+4n	0x48+4n		0x00000000	Write-only access to instruction memory location n, from ws2812.pio.h header filer	0x00000000
INSTR_MEM31	502000c4	0x000000c4	Instruction memory location 31	0x00000000	Write-only access to instruction memory location 31, instruction memory register is a 32 bit value.	0x00000000
SM0_CLKDIV	50200c8	0x000000c8	Clock divisor register for SM0	0x000fa000	Clock divisor register for state machine n. Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256). The frist 8 bits are reserved ones with the FRAC is reseted to 0. The last 4 bits of the INT is reseted to vaue 1.	0x000fa000
SM0_EXECCTRL	502000cc	0x0cc	Execution settings for state machine N	0x00017a00	Execution/behavioural settings for state machine n. The 5 to 6 bits are reserved ones and the 12 to 16 bits are offset to 0x1f, the rest of the bits are being reseted to 0.	0x00013800
SM0_SHIFTCRTL	502000d0	0x0d0	Control behaviour of the input/output shift	0x40060000	Control behaviour of the input/output shift registers for state machine 0. The first half of the register' bits are the reserved ones with the 18, 19 bits reset to 1.	0x40060000
SM0_ADDR	502000d4	0x0d4		0x00000014	Current instruction address of state machine 0. The first four bits are resetd to 0 with the rest bits of it are reserved.	0x00000010
SM0_INSTR	502000d8	0x0d8		0x00006221	Read to see the instruction currently addressed by state machine0’s program counterWrite to execute	0x00006221
SM0_PINCTRL	502000dc	0x0dc	State Machine Pin Control	0x20003000	State machine pin control 0. Since only the 26 to 28 bits are offset to 0x5(101)	0x20003000
SM1_CLKDIV	50200e0	0x0e0		0x00010000	Clock divisor register for state machine 1 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)	0x00010000

SM1_EXECCTRL	50200e4	0x0e4		0x0001f000	Execution/behavioural settings for state machine 1	0x0001f000	
SM1_SHIFTCTRL	50200e8	0x0e8		0x000c000	Control behaviour of the input/output shift registers for state machine 1	0x000c0000	
SM1_ADDR	50200ec	0x0ec		0x0000000	Current instruction address of state machine 1	0x0000000	
SM1_INSTR	50200f0	0x0f0		0x0000fcfe	Read to see the instruction currently addressed by state machine 1's program counter Write to execute an instruction immediately (including jumps) and then resume execution.	0x00007df3	
SM1_PINCTRL	50200f4	0x0f4		0x00000000	State machine pin control	0x00000000	
SM2_CLKDIV	50200f8	0x0f8		0x00010000	Clock divisor register for state machine 2 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)	0x00010000	
SM2_EXECCTRL	50200fc	0x0fc		0x0001f000	Execution/behavioural settings for state machine 2	0x0001f000	
SM2_SHIFTCTRL	5020100	0x100		0x000c0000	Control behaviour of the input/output shift registers for state machine 2	0x000c0000	
SM2_ADDR	5020104	0x104		0x00000000	Current instruction address of state machine 2	0x00000000	
SM2_INSTR	5020108	0x108		0x0000fcfe	Read to see the instruction currently addressed by state machine 2's program counter Write to execute an instruction immediately (including jumps) and then resume execution.	0x00007df3	
SM2_PINCTRL	502010c	0x10c		0x14000000	State machine pin control	0x14000000	
SM3_CLKDIV	5020110	0x110		0x00010000	Clock divisor register for state machine 3 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)	0x00010000	
SM3_EXECCTRL	5020114	0x114		0x0001f000	Execution/behavioural settings for state machine 3	0x0001f000	
SM3_SHIFTCTRL	5020118	0x118		0x000c0000	Control behaviour of the input/output shift registers for state machine 3	0x000c0000	
SM3_ADDR	502011c	0x11c		0x00000000	Current instruction address of state machine 3	0x00000000	
SM3_INSTR	5020120	0x120		0x0000fcfe	Read to see the instruction currently addressed by state machine 3's program counter Write to execute an instruction immediately (including jumps) and then resume execution.	0x00007df3	
SM3_PINCTRL	5020124	0x124		0x14000000	State machine pin control	0x14000000	