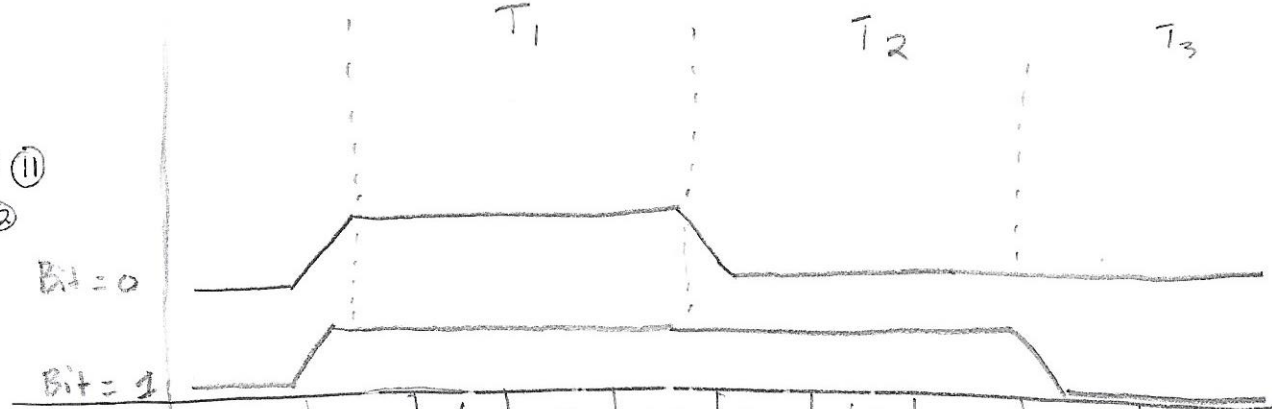
```
L1 .wrap_target
L2 Bitloop ⑤ ⑯
L3 out x, 1  side 0 [T3-1]  ① ⑥ ⑪
L4 jmp !x do_zero side 1 [T1-1]  ② ⑦ ⑫
L5 do_one: ③ ⑧
L6 jmp bitloop side 1 [T2-1] ④ ⑨
L7 do_zero ⑬
L8 nop  side 0 [T2-1] ⑭
L9 .wrap ⑮
```



Clock	1	4	6	7	12	13	16	18	19	24	25	28	30
Current instr	L3	L4	L5	L6	L2	L3	L4	L5	L6	L2	L3	L4	L7
FIFO data	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Sm stalled	N	N	Y	N	Y	N	N	Y	N	Y	N	N	Y
~~delay~~ cycles before next step	2	1	0	4	0	2	1	0	4	0	2	1	0
OSR value	1	1	1	1	0	0	0	0	0	0	0	0	0
Sm x value	1	1	1	1	1	1	1	1	1	1	0	0	0
Led state	0	1	1	1	1	1	1	1	1	1	0	0	0

Bit 1 | Bit 2 | Bit 3

Color: 110 110 1000 1000 1111 0000

First bit

For first 3 bits 110

$T_1 = 2 \quad T_2 = 5 \quad T_3 = 3$