	Address	Offset	Name	Value	Notes
BASE	0x50200000 0x50300000	Null	PIO0 PIO1	Null	Initialize with pio0
CTRL	0x50200000	0x000	PIO control register	00000000	SM_ENABLE, SM_RESTART, and CLKDIV_RESTART is rest to 0x0.
FSTAT	0x50200004	0x004	FIFO status register	0f000f01	TX Full,RX empty
FDEBUG	0x50200008	0x008	FIFO debug register	01000e00	SM0 TX FIFO taken
FLEVEL	0x5020000c	0x00c	FIFO levels	00000000	All of bits of this register is rested to 0 after offsetting.
TXF0 TXF1 TFX2 TFX3	0x50200010 0x50200014 0x50200018 0x5020001c	0x010 0x014 0x018 0x01c	TX FIFO	00000000	All of bits of this register is rested to 0 after offsetting, and no reserved bits in this register.
RXF0 RXF1 RXF2 RXF3	0x50200020 0x50200024 0x50200028 0x5020002c	0x020 0x024 0x028 0x02c	RX FIFO	00000ff00 a9572ec5 ebb3cbda 6d37b798	
INSTR_MEM0	0x50200048	0x048	Instruction memory 0	00000000	
INSTR_MEM31	0x502000c4	0x0c4	Instruction memory 31	00000000	Similarly, as INSTR_MEM0

SM0_CLKDIV	0x502000c8	0x0c8	Clock divisors register for state machine 0	000fa000	
SM0_EXECCTRL	0x502000cc	0x0cc	Execution/behavioral settings for state machine 0	0000b400	
SM0_SHIFTCTRL	0x502000d0	0x0d8	Shift registers for state machine 0	40060000	Use RX FIFO as TX, output left, auto pull
SM0_ADDR	0x502000d4	0x0d4	Current instruction addresses of state machine 0	00000008	Current instruction address (0x1c)
SM0_INSTR	0x502000d8	0x0d8	Instruction registers for state machine 0	00006221	
SM0_PINCTRL	0x502000dc	0x0dc	State machine pin control 0	20000800	Side set 1