Given 7,=2 72=5 73=3 SM main loop . Wrep_target bit-loop: side 0 [73-1] (Li) out X. 1 (L2) jmp !x do_zero Side 1 [7, -1] do_one (L3) jmp bitloop Side | [72-1] do_zero Sde 0 [72-1] (14) nop wrap Follow the loop, we will have Date =0 Date = 1 72 instructions (Repeat) clock 5 **/**0 Date 1 T3 = 3 Ti=2 cycle come SM stalled n n n GPIO Date in FLFO? η SM X 1/0