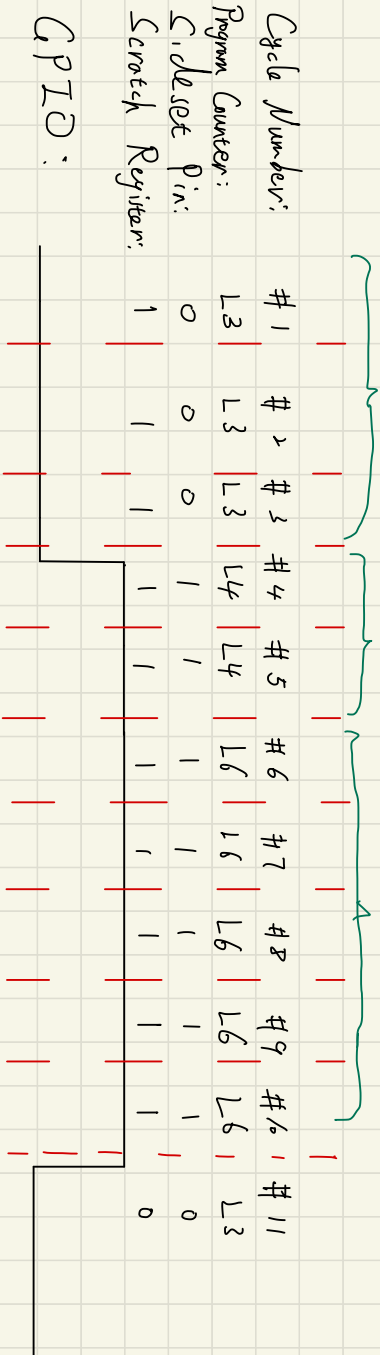


$T_3 = 3$ cycles $T_1 = 2$ cycles $T_1 = 5$ cycles.



Label Instruction: #808080 := [1000]08080

L1: left shift OR den 1 bit. Most Significant Bit was popped out (1)

Explanation: Since the bit is zero, this output voltage is a so-called "short-positive" pulse which is recognized as "0" by the vnsr12 module.

```

18 1 1 wrap target
19 1 bitloop:
20 1 1 out x, 1
21 1 4 jmp ix do_zero side 1 [11 - 1] ; Branch on the bit we shifted out. Positive pulse
22 1 6 do_one:
23 1 6 jmp bitloop
24 1 1 do_zero:
25 1 8 nop
26 1 3 wrap
  
```