SM Cycle Count	0	1	2	3	SM Cycle Count	0	1	2	3
SM CLK					FDEBUG [27:24] STALL EMPTY TX FIFO				
GPIO 12					FDEBUG [3:0] STALL FULL RX FIFO				
WS2812 Serial Input V					TX FIFO [31:0]				
WS2812 V					RX FIFO [31:0]				
APDS-9969 V					OSR (0 full)				
WS2812 Luminance					Instruction	Waiting	Recieve Signal	Out From FIFO	Transmit
FSTAT [27:24] TX FIFO EMPTY									
FSTAT [19:16] TX FIFO FULL									
FSTAT [11:8] RX FIFO EMPTY									
FSTAT [3:0] RX FIFO FULL									