```
L1  .wrap_target
L2  bitloop:
L3    out x, 1   side 0 [T3-1];
L4    jmp !x do_zero side 1 [T1-1];
L5  do_one:
L6    jmp bitloop side 1 [T2-1];
L7  do_zero:
L8    nop side 0 [T2-1];
L9  .wrap
```

x=1

	T1	T2	T3	T4
INSN	L3	L4	L6	L3
Data?	N	Y	Y	N
Stalled?	Y	N	N	Y
Delay Cycles	3	2	5	3
OSR	0	1	1	0
SM "X"	0	1	1	0
LED State	0	1	1	0

...

x=0

	T1	T2	T3
INSN	L3	L4	L8
Data?	N	N	N
Stalled?	Y	N	Y
Delay cycle	3	2	5
OSR	0	0	0
SM "X"	0	0	0
LED State	0	0	0